Silicon NPN Power Transistors 2SD1496

DESCRIPTION

·With TO-3PN package
·High voltage ,high reliability
·Wide area of safe operation

APPLICATIONS

·High voltage power switching TV horizontal deflection output applications

PINNING

PIN	DESCRIPTION
1	Base
2	Collector;connected to mounting base
3	Emitter

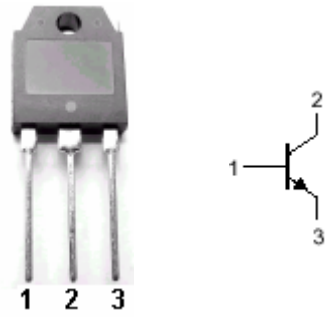

Fig.1 simplified outline (TO-3PN) and symbol

Absolute maximum ratings (Ta=25□)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	1500	V
V_{CEO}	Collector-emitter voltage	Open base	600	V
V_{EBO}	Emitter-base voltage	Open collector	6	V
I_C	Collector current		5	A
$I_{C(surge)}$	Collector surge current		16	A
P_C	Collector power dissipation	T_C=25□	50	W
T_j	Junction temperature		150	□
T_{stg}	Storage temperature		-45~150	□

Silicon NPN Power Transistors 2SD1496

CHARACTERISTICS

Tj=25□ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{(BR)EBO}$	Emitter-base breakdown voltage	I_E=10mA; I_C=0	6			V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage	I_C=10mA; R_{BE}=∞	600			V
V_{CEsat}	Collector-emitter saturation voltage	I_C=4.5A; I_B=1.2A			5.0	V
V_{BEsat}	Base-emitter saturation voltage	I_C=4.5A; I_B=1.2A			1.5	V
I_{CEX}	Collector cut-off current	V_{CE}=1500V; V_{BE}=1.5V			1.0	mA
I_{EBO}	Emitter cut-off current	V_{EB}=6V; I_C=0			1.0	mA
h_{FE}	DC current gain	I_C=0.3A ; V_{CE}=5V	10		30	
t_f	Fall time	I_C=3A;I_{B1}=0.7A, I_{B2}=-2.7A; L_B=0			2.3	μs

PACKAGE OUTLINE

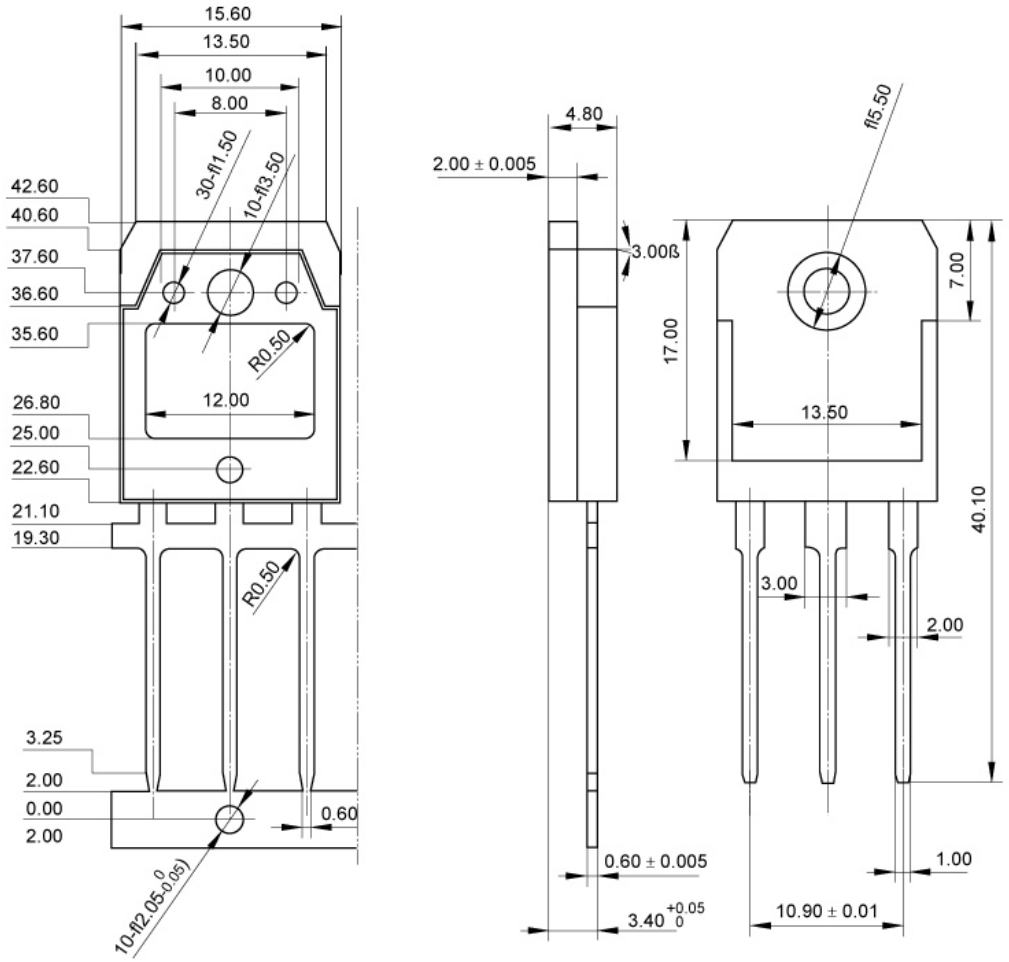

Fig.2 outline dimensions (unindicated tolerance:±0.10 mm)