

To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

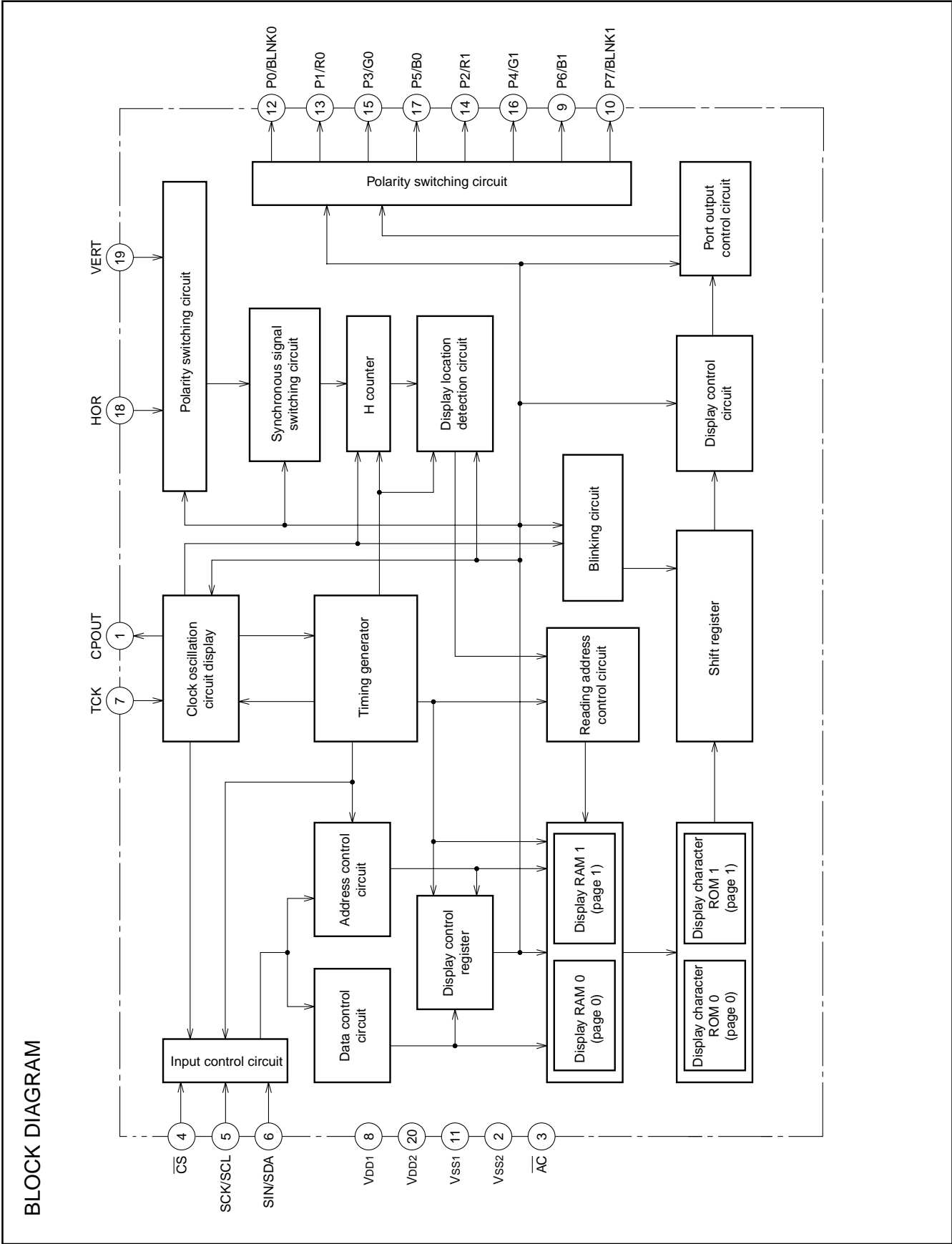
The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

PIN DESCRIPTION

Pin Number	Symbol	Pin name	Input/Output	Function
1	CPOUT	Filter output	Output	Filter output. Connect loop filter to this pin.
2	VSS2	Earthing pin	–	Connect to GND.
3	\overline{AC}	Auto-clear input	Input	When "L", this pin resets the internal IC circuit. Hysteresis input. Built-in pull-up resistor.
4	\overline{CS}	Chip select input	Input	<at the 16-bit serial communication> Chip select pin. Set this pin to "L" level at serial data transfer. Hysteresis input. Built-in pull-up resistor.
				<at the I ² C-BUS serial communication> Set this pin to "H" level.
5	SCK/SCL	Clock input	Input	<at the 16-bit serial communication> SIN pin serial data is taken in when SCK rises at \overline{CS} pin "L" level. Hysteresis input.
				<at the I ² C-BUS serial communication> SDA pin serial data is taken in synchronized with SCL.
6	SIN/SDA	Data input	Input	<at the 16-bit serial communication> This is the pin for serial input of display control register and display RAM data. Hysteresis input.
		Data I/O	I/O	<at the I ² C-BUS serial communication> Hysteresis input. This is the pin for serial input of display control register and display RAM data. Also this pin output acknowledge signal.
7	TCK	External clock	Input	This is the pin for external clock input.
8	VDD1	Power pin	–	Please connect to +5V with the power pin.
9	P6/B1	Port P6 output	Output	This pin can be toggled between port pin output and B1 signal output.
10	P7/BLNK1	Port P7 output	Output	This pin can be toggled between port pin output and BLNK1 signal output.
11	VSS1	Earthing pin	–	Please connect to GND using circuit earthing pin.
12	P0/BLNK0	Port P0 output	Output	This pin can be toggled between port pin output and BLNK0 signal output.
13	P1/R0	Port P1 output	Output	This pin can be toggled between port pin output and R0 signal output.
14	P2/R1	Port P2 output	Output	This pin can be toggled between port pin output and R1 signal output.
15	P3/G0	Port P3 output	Output	This pin can be toggled between port pin output and G0 signal output.
16	P4/G1	Port P4 output	Output	This pin can be toggled between port pin output and G1 signal output.
17	P5/B0	Port P5 output	Output	This pin can be toggled between port pin output and B0 signal output.
18	HOR	Horizontal synchronous signal input	Input	This pin inputs the horizontal synchronous signal. Hysteresis input.
19	VERT	Vertical synchronous signal input	Input	This pin inputs the vertical synchronous signal. Hysteresis input.
20	VDD2	Power pin	–	Please connect to +5V with the power pin.



MEMORY CONSTITUTION

Address 000₁₆ to 11F₁₆ are assigned to the display RAM, address 120₁₆ to 128₁₆ are assigned to the display control registers. The internal circuit is reset and all display control registers (address 120₁₆ to 128₁₆) are set to "0" when the \overline{AC} pin level is "L". And then, RAM is not erased and be undefined. This memory is consisted of 2

pages : page 0 memory and page 1 memory (their addresses are common), page controlled by DAF bit of each address when writing data. For detail, see "Data input". Memory constitution is shown in Figure 1 and 2.

Addresses	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
000 ₁₆	0	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0
001 ₁₆	0	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0
⋮	⋮	Background coloring			Blinking	Character color			Character code							
11E ₁₆	0	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0
11F ₁₆	0	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0
120 ₁₆	0	EXCK0	DISV2	DIVS1	DIVS0	DIV10	DIV9	DIV8	DIV7	DIV6	DIV5	DIV4	DIV3	DIV2	DIV1	DIV0
121 ₁₆	0	RSEL0	PTD7	PTD6	PTD5	PTD4	PTD3	PTD2	PTD1	PTD0	PTC5	PTC4	PTC3	PTC2	PTC1	PTC0
122 ₁₆	0	RSEL1	SPACE2	SPACE1	SPACE0	HP10	HP9	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0
123 ₁₆	0	EXCK1	TEST3	TEST2	TEST1	TEST0	VP9	VP8	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
124 ₁₆	0	TEST9	PTC67	TEST4	DSP11	DSP10	DSP9	DSP8	DSP7	DSP6	DSP5	DSP4	DSP3	DSP2	DSP1	DSP0
125 ₁₆	0	TEST10	VSZ1H1	VSZ1H0	VSZ1L1	VSZ1L0	V1SZ1	V1SZ0	LIN9	LIN8	LIN7	LIN6	LIN5	LIN4	LIN3	LIN2
126 ₁₆	0	POPUP	VSZ2H1	VSZ2H0	VSZ2L1	VSZ2L0	V18SZ1	V18SZ0	LIN17	LIN16	LIN15	LIN14	LIN13	LIN12	LIN11	LIN10
127 ₁₆	0	MODE0	TEST12	HSZ20	TEST11	HSZ10	BETA14	TEST8	TEST7	TEST6	FB	FG	FR	RB	RG	RR
128 ₁₆	0	MODE1	BLINK2	BLINK1	BLINK0	DSPON	STOP	RAMERS	SYAD	BLK1	BLK0	POLH	POLV	VMASK	B/F	BCOL

Fig. 1 Memory constitution (page 0 memory)

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

Addresses	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
000 ₁₆	1	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0
001 ₁₆	1	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0
⋮	⋮	Background coloring			Blinking	Character color			Character code							
11E ₁₆	1	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0
11F ₁₆	1	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0
120 ₁₆	1	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
121 ₁₆	1	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
122 ₁₆	1	–	SPACE2	SPACE1	SPACE0	HP10	HP9	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0
123 ₁₆	1	–	TEST3	VJT	TEST1	TEST0	VP9	VP8	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
124 ₁₆	1	–	–	TEST4	DSP11	DSP10	DSP9	DSP8	DSP7	DSP6	DSP5	DSP4	DSP3	DSP2	DSP1	DSP0
125 ₁₆	1	–	VSZ1H1	VSZ1H0	VSZ1L1	VSZ1L0	V1SZ1	V1SZ0	LIN9	LIN8	LIN7	LIN6	LIN5	LIN4	LIN3	LIN2
126 ₁₆	1	–	VSZ2H1	VSZ2H0	VSZ2L1	VSZ2L0	V18SZ1	V18SZ0	LIN17	LIN16	LIN15	LIN14	LIN13	LIN12	LIN11	LIN10
127 ₁₆	1	–	TEST12	HSZ20	TEST11	HSZ10	BETA14	TEST8	TEST7	TEST6	FB	FG	FR	RB	RG	RR
128 ₁₆	1	–	BLINK2	BLINK1	BLINK0	DSPON	TEST13	RAMERS	SYAD	BLK1	BLK0	–	–	–	–	BCOL

Fig. 2 Memory constitution (page 1 memory)

Note: Page 0 and page 1 registers are found in their respective pages. For example, HP10 to HP0 of the page 0 memory sets the horizontal display start position of page 0, whereas HP10 to HP0 (same register name) of the page 1 memory sets the horizontal display start position of page 1. Also, registers common to both page 0 and page 1 are found only in the page 0 memory. For example, PTC0 is the control register of the P0 pin and is found only in the page 0 memory.

SCREEN CONSTITUTION

The screen lines and rows are determined from each address of the display RAM (page 0 and page 1 are common). The screen constitution is shown in Figure 3.

Row Line	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	000 ₁₆	001 ₁₆	002 ₁₆	003 ₁₆	004 ₁₆	005 ₁₆	006 ₁₆	007 ₁₆	008 ₁₆	009 ₁₆	00A ₁₆	00B ₁₆	00C ₁₆	00D ₁₆	00E ₁₆	00F ₁₆	010 ₁₆	011 ₁₆	012 ₁₆	013 ₁₆	014 ₁₆	015 ₁₆	016 ₁₆	017 ₁₆
2	018 ₁₆	019 ₁₆	01A ₁₆	01B ₁₆	01C ₁₆	01D ₁₆	01E ₁₆	01F ₁₆	020 ₁₆	021 ₁₆	022 ₁₆	023 ₁₆	024 ₁₆	025 ₁₆	026 ₁₆	027 ₁₆	028 ₁₆	029 ₁₆	02A ₁₆	02B ₁₆	02C ₁₆	02D ₁₆	02E ₁₆	02F ₁₆
3	030 ₁₆	031 ₁₆	032 ₁₆	033 ₁₆	034 ₁₆	035 ₁₆	036 ₁₆	037 ₁₆	038 ₁₆	039 ₁₆	03A ₁₆	03B ₁₆	03C ₁₆	03D ₁₆	03E ₁₆	03F ₁₆	040 ₁₆	041 ₁₆	042 ₁₆	043 ₁₆	044 ₁₆	045 ₁₆	046 ₁₆	047 ₁₆
4	048 ₁₆	049 ₁₆	04A ₁₆	04B ₁₆	04C ₁₆	04D ₁₆	04E ₁₆	04F ₁₆	050 ₁₆	051 ₁₆	052 ₁₆	053 ₁₆	054 ₁₆	055 ₁₆	056 ₁₆	057 ₁₆	058 ₁₆	059 ₁₆	05A ₁₆	05B ₁₆	05C ₁₆	05D ₁₆	05E ₁₆	05F ₁₆
5	060 ₁₆	061 ₁₆	062 ₁₆	063 ₁₆	064 ₁₆	065 ₁₆	066 ₁₆	067 ₁₆	068 ₁₆	069 ₁₆	06A ₁₆	06B ₁₆	06C ₁₆	06D ₁₆	06E ₁₆	06F ₁₆	070 ₁₆	071 ₁₆	072 ₁₆	073 ₁₆	074 ₁₆	075 ₁₆	076 ₁₆	077 ₁₆
6	078 ₁₆	079 ₁₆	07A ₁₆	07B ₁₆	07C ₁₆	07D ₁₆	07E ₁₆	07F ₁₆	080 ₁₆	081 ₁₆	082 ₁₆	083 ₁₆	084 ₁₆	085 ₁₆	086 ₁₆	087 ₁₆	088 ₁₆	089 ₁₆	08A ₁₆	08B ₁₆	08C ₁₆	08D ₁₆	08E ₁₆	08F ₁₆
7	090 ₁₆	091 ₁₆	092 ₁₆	093 ₁₆	094 ₁₆	095 ₁₆	096 ₁₆	097 ₁₆	098 ₁₆	099 ₁₆	09A ₁₆	09B ₁₆	09C ₁₆	09D ₁₆	09E ₁₆	09F ₁₆	0A0 ₁₆	0A1 ₁₆	0A2 ₁₆	0A3 ₁₆	0A4 ₁₆	0A5 ₁₆	0A6 ₁₆	0A7 ₁₆
8	0A8 ₁₆	0A9 ₁₆	0AA ₁₆	0AB ₁₆	0AC ₁₆	0AD ₁₆	0AE ₁₆	0AF ₁₆	0B0 ₁₆	0B1 ₁₆	0B2 ₁₆	0B3 ₁₆	0B4 ₁₆	0B5 ₁₆	0B6 ₁₆	0B7 ₁₆	0B8 ₁₆	0B9 ₁₆	0BA ₁₆	0BB ₁₆	0BC ₁₆	0BD ₁₆	0BE ₁₆	0BF ₁₆
9	0C0 ₁₆	0C1 ₁₆	0C2 ₁₆	0C3 ₁₆	0C4 ₁₆	0C5 ₁₆	0C6 ₁₆	0C7 ₁₆	0C8 ₁₆	0C9 ₁₆	0CA ₁₆	0CB ₁₆	0CC ₁₆	0CD ₁₆	0CE ₁₆	0CF ₁₆	0D0 ₁₆	0D1 ₁₆	0D2 ₁₆	0D3 ₁₆	0D4 ₁₆	0D5 ₁₆	0D6 ₁₆	0D7 ₁₆
10	0D8 ₁₆	0D9 ₁₆	0DA ₁₆	0DB ₁₆	0DC ₁₆	0DD ₁₆	0DE ₁₆	0DF ₁₆	0E0 ₁₆	0E1 ₁₆	0E2 ₁₆	0E3 ₁₆	0E4 ₁₆	0E5 ₁₆	0E6 ₁₆	0E7 ₁₆	0E8 ₁₆	0E9 ₁₆	0EA ₁₆	0EB ₁₆	0EC ₁₆	0ED ₁₆	0EE ₁₆	0EF ₁₆
11	0F0 ₁₆	0F1 ₁₆	0F2 ₁₆	0F3 ₁₆	0F4 ₁₆	0F5 ₁₆	0F6 ₁₆	0F7 ₁₆	0F8 ₁₆	0F9 ₁₆	0FA ₁₆	0FB ₁₆	0FC ₁₆	0FD ₁₆	0FE ₁₆	0FF ₁₆	100 ₁₆	101 ₁₆	102 ₁₆	103 ₁₆	104 ₁₆	105 ₁₆	106 ₁₆	107 ₁₆
12	108 ₁₆	109 ₁₆	10A ₁₆	10B ₁₆	10C ₁₆	10D ₁₆	10E ₁₆	10F ₁₆	110 ₁₆	111 ₁₆	112 ₁₆	113 ₁₆	114 ₁₆	115 ₁₆	116 ₁₆	117 ₁₆	118 ₁₆	119 ₁₆	11A ₁₆	11B ₁₆	11C ₁₆	11D ₁₆	11E ₁₆	11F ₁₆

* The hexadecimal numbers in the boxes show the display RAM address.

Fig. 3 Screen constitution

DISPLAY RAM

Address 000₁₆ to 11F₁₆

DA	Register	Contents		Remarks																																				
		Status	Function																																					
0	C0	0	Set the displayed ROM character code. To write data into page 0 (Note 2), select the data from the ROM characters (256 types) for page 0 and set the character code. To write data into page 1, do the same from the ROM characters (256 types) for page 1.	Set display character																																				
		1																																						
1	C1	0																																						
		1																																						
2	C2	0																																						
		1																																						
3	C3	0																																						
		1																																						
4	C4	0																																						
		1																																						
5	C5	0																																						
		1																																						
6	C6	0																																						
		1																																						
7	C7	0																																						
		1																																						
8	R	0	<table border="1"> <thead> <tr> <th>B</th> <th>G</th> <th>R</th> <th>Color</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>Red</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>Green</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>Yellow</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>Blue</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>Magenta</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>Cyan</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>White</td></tr> </tbody> </table>	B	G	R	Color	0	0	0	Black	0	0	1	Red	0	1	0	Green	0	1	1	Yellow	1	0	0	Blue	1	0	1	Magenta	1	1	0	Cyan	1	1	1	White	Set character color (character unit)
		B		G	R	Color																																		
0	0	0		Black																																				
0	0	1		Red																																				
0	1	0		Green																																				
0	1	1		Yellow																																				
1	0	0		Blue																																				
1	0	1		Magenta																																				
1	1	0		Cyan																																				
1	1	1		White																																				
1																																								
9	G	0																																						
		1																																						
A	B	0																																						
		1																																						
B	BLINK	0		Do not blink.	Set blinking See register BLINK2 to BLINK0 (address 128 ₁₆)																																			
		1	Blinking																																					
C	BR	0	<table border="1"> <thead> <tr> <th>BB</th> <th>BG</th> <th>BR</th> <th>Color</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>Red</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>Green</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>Yellow</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>Blue</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>Magenta</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>Cyan</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>White</td></tr> </tbody> </table>	BB	BG	BR	Color	0	0	0	Black	0	0	1	Red	0	1	0	Green	0	1	1	Yellow	1	0	0	Blue	1	0	1	Magenta	1	1	0	Cyan	1	1	1	White	Set character background (character unit)
		BB		BG	BR	Color																																		
0	0	0		Black																																				
0	0	1		Red																																				
0	1	0		Green																																				
0	1	1		Yellow																																				
1	0	0		Blue																																				
1	0	1		Magenta																																				
1	1	0		Cyan																																				
1	1	1		White																																				
1																																								
D	BG	0																																						
		1																																						
E	BB	0																																						
		1																																						

Notes 1. The display RAM is undefined state at the AC pin.

2. The display RAM consists of 2 pages, page 0 and page 1 (common address). The page in which data is written is controlled by the DAF bit. When set to "0", data is written into page 0, whereas when set to "1", data is written into page 1.

REGISTERS DESCRIPTION

(1) Address 120₁₆

DA	Register	Contents		Remarks															
		Status	Function																
0	DIV0 (Note 3)	0	Set division value (multiply value) of horizontal oscillation frequency. $N1 = \sum_{n=0}^{10} (DIVn \times 2^n)$ N1 : division value (multiply value)	Set display frequency by division value (multiply value) setting. For details, see REGISTER SUPPLEMENTARY DESCRIPTION (1). Also, set the display frequency range by registers DIVS0, DIVS1(address 120 ₁₆), RSEL0(address 121 ₁₆) and RSEL1(address 122 ₁₆) in accordance with the display frequency. Any of this settings above is required only when EXCK1 = 0, EXCK0 = 1 and EXCK1 = 1, EXCK0 = 1.															
		1																	
		2																	
		3																	
		4																	
		5																	
		6																	
		7																	
		8																	
		9																	
		A																	
B	DIVS0 (Note 3)	0	For setting, see REGISTER SUPPLEMENTARY DESCRIPTION (2).	Set display frequency range.															
		1																	
C	DIVS1 (Note 3)	0																	
		1																	
D	DISV2 (Note 3)	0																	
		1																	
E	EXCK0 (Note 3)	0	<table border="1"> <thead> <tr> <th>EXCK1</th> <th>EXCK0</th> <th>Display clock input</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>External clock mode 1</td> </tr> <tr> <td>0</td> <td>1</td> <td>Internal clock mode</td> </tr> <tr> <td>1</td> <td>0</td> <td>Do not set</td> </tr> <tr> <td>1</td> <td>1</td> <td>External clock mode 2</td> </tr> </tbody> </table>	EXCK1	EXCK0	Display clock input	0	0	External clock mode 1	0	1	Internal clock mode	1	0	Do not set	1	1	External clock mode 2	Display clock setting See REGISTER SUPPLEMENTARY DESCRIPTION (1) EXCK1 : address123 ₁₆
		EXCK1		EXCK0	Display clock input														
		0		0	External clock mode 1														
		0		1	Internal clock mode														
		1		0	Do not set														
1	1	External clock mode 2																	
1																			

- Notes 1. The mark ○ around the status value means the reset status by the "L" level is input to $\bar{A}C$ pin.
 2. The page in which data is written is controlled by the DAF bit. When set to "0", data is written into page 0, whereas when set to "1", data is written into page 1.
 3. Registers marked with (Note 3) are found only in page 0, therefore the register value does not change when the DAF bit is set to "1".

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(2) Address 12116

DA	Register	Contents		Remarks
		Status	Function	
0	PTC0 (Note 3)	⓪	P0 output (port P0).	P0 pin output control.
		1	BLNK0 output.	
1	PTC1 (Note 3)	⓪	P1 output (port P1).	P1 pin output control.
		1	R0 signal output.	
2	PTC2 (Note 3)	⓪	P2 output (port P2).	P2 pin output control.
		1	R1 signal output.	
3	PTC3 (Note 3)	⓪	P3 output (port P3).	P3 pin output control.
		1	G0 signal output.	
4	PTC4 (Note 3)	⓪	P4 output (port P4).	P4 pin output control.
		1	G1 signal output.	
5	PTC5 (Note 3)	⓪	P5 output (port P5).	P5 pin output control.
		1	B0 signal output.	
6	PTD0 (Note 3)	⓪	"L" output or negative polarity output (BLNK0 output).	P0 pin data control.
		1	"H" output or positive polarity output (BLNK0 output).	
7	PTD1 (Note 3)	⓪	"L" output or negative polarity output (R0 signal output).	P1 pin data control.
		1	"H" output or positive polarity output (R0 signal output).	
8	PTD2 (Note 3)	⓪	"L" output or negative polarity output (R1 signal output).	P2 pin data control.
		1	"H" output or positive polarity output (R1 signal output).	
9	PTD3 (Note 3)	⓪	"L" output or negative polarity output (G0 signal output).	P3 pin data control.
		1	"H" output or positive polarity output (G0 signal output).	
A	PTD4 (Note 3)	⓪	"L" output or negative polarity output (G1 signal output).	P4 pin data control.
		1	"H" output or positive polarity output (G1 signal output).	
B	PTD5 (Note 3)	⓪	"L" output or negative polarity output (B0 signal output).	P5 pin data control.
		1	"H" output or positive polarity output (B0 signal output).	
C	PTD6 (Note 3)	⓪	"L" output or negative polarity output (B1 signal output).	P6 pin data control.
		1	"H" output or positive polarity output (B1 signal output).	
D	PTD7 (Note 3)	⓪	"L" output or negative polarity output (BLNK1 signal output).	P7 pin data control.
		1	"H" output or positive polarity output (BLNK1 signal output).	
E	RSEL0 (Note 3)	⓪	For setting, see REGISTER SUPPLYMENTARY DESCRIPTION (2).	Set display frequency range.
		1		

Notes 1. The mark ⓪ around the status value means the reset status by the "L" level is input to AC pin.

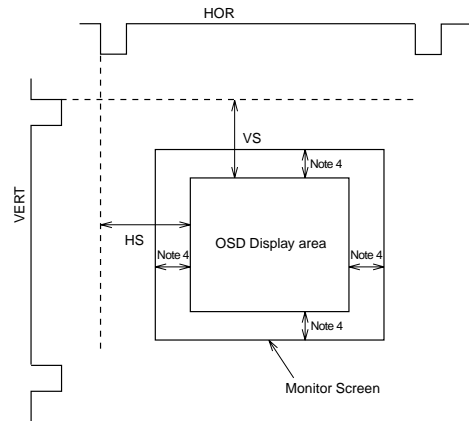
2. The page in which data is written is controlled by the DAF bit. When set to "0", data is written into page 0, whereas when set to "1", data is written into page 1.

3. Registers marked with (Note 3) are found only in page 0, therefore the register value does not change when the DAF bit is set to "1".

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(3) Address 122₁₆

DA	Register	Contents		Remarks																																							
		Status	Function																																								
0	HP0	0	If HS is the horizontal display start location, $HS = T \times \left(\sum_{n=0}^{10} 2^n HP_n + 6 \right)$	Horizontal display start location is specified using the 11 bits from HP10 to HP0. HP10 to HP0 = (00000000000 ₂) and (00000100111 ₂) setting is forbidden.																																							
		1																																									
1	HP1	0	T : Period of display frequency 2007 settings are possible.																																								
		1																																									
2	HP2	0																																									
		1																																									
3	HP3	0																																									
		1																																									
4	HP4	0																																									
		1																																									
5	HP5	0																																									
		1																																									
6	HP6	0																																									
		1																																									
7	HP7	0																																									
		1																																									
8	HP8	0																																									
		1																																									
9	HP9	0																																									
		1																																									
A	HP10	0																																									
		1																																									
B	SPACE0	0	<table border="1"> <thead> <tr> <th colspan="3">SPACE</th> <th rowspan="2">Number of Lines and Space <(S) represents space></th> </tr> <tr> <th>2</th> <th>1</th> <th>0</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>12</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1 (S) 10 (S) 1</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>2 (S) 8 (S) 2</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>3 (S) 6 (S) 3</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>4 (S) 4 (S) 4</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>5 (S) 2 (S) 5</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>6 (S) 6</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>6 (S)(S) 6</td> </tr> </tbody> </table> (S) represents one line worth of space	SPACE			Number of Lines and Space <(S) represents space>	2	1	0	0	0	0	12	0	0	1	1 (S) 10 (S) 1	0	1	0	2 (S) 8 (S) 2	0	1	1	3 (S) 6 (S) 3	1	0	0	4 (S) 4 (S) 4	1	0	1	5 (S) 2 (S) 5	1	1	0	6 (S) 6	1	1	1	6 (S)(S) 6	Leave one line worth of space in the vertical direction. For example, 6 (S) 6 indicates two sets of 6 lines with a line of spaces between lines 6 and 7. A line is 18 × N horizontal scan lines. N is determined by the character size in the vertical direction
		SPACE			Number of Lines and Space <(S) represents space>																																						
2	1	0																																									
0	0	0	12																																								
0	0	1	1 (S) 10 (S) 1																																								
0	1	0	2 (S) 8 (S) 2																																								
0	1	1	3 (S) 6 (S) 3																																								
1	0	0	4 (S) 4 (S) 4																																								
1	0	1	5 (S) 2 (S) 5																																								
1	1	0	6 (S) 6																																								
1	1	1	6 (S)(S) 6																																								
1																																											
C	SPACE1	0																																									
		1																																									
D	SPACE2	0																																									
		1																																									
E	RSEL1 (Note 3)	0	For setting, see REGISTER SUPPLEMENTARY DESCRIPTION (2).	Set display frequency range.																																							
		1																																									

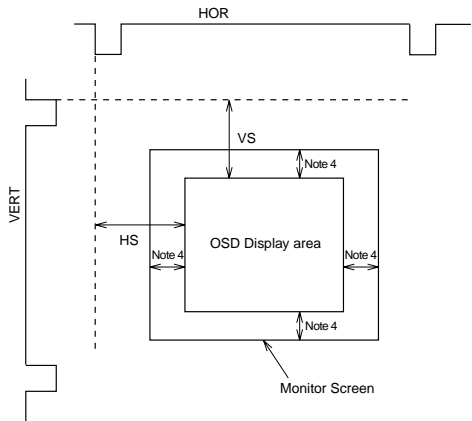


- Notes 1. The mark ○ around the status value means the reset status by the "L" level is input to AC pin.
 2. The page in which data is written is controlled by the DAF bit. When set to "0", data is written into page 0, whereas when set to "1", data is written into page 1.
 3. Registers marked with (Note 3) are found only in page 0, therefore the register value does not change when the DAF bit is set to "1".
 4. Set up the horizontal and vertical display start location so that display range may not exceed it.
 Set the character code "FF₁₆" (blank without background) for the display RAM of the part which the display range exceeds.

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(4) Address 123₁₆

DA	Register	Contents		Remarks
		Status	Function	
0	VP0	0	If VS is the vertical display start location,	The vertical start location is specified using the 10 bits from VP9 to VP0. VP9 to VP0 = (0000000002) setting is forbidden.
		1	$VS = H \times \sum_{n=0}^9 2^n VP_n$	
1	VP1	0	H: Cycle with the horizontal synchronizing pulse	
		1	1023 settings are possible.	
2	VP2	0		
		1		
3	VP3	0		
		1		
4	VP4	0		
		1		
5	VP5	0		
		1		
6	VP6	0		
		1		
7	VP7	0		
		1		
8	VP8	0		
		1		
9	VP9	0		
		1		
A	TEST0	0	It should be fixed to "0".	
		1	Can not be used.	
B	TEST1	0	It should be fixed to "0".	
		1	Can not be used.	
C	VJT	0	It should be fixed to "0".	
		1	Can not be used.	
D	TEST3	0	It should be fixed to "0".	
		1	Can not be used.	
E	EXCK1 (Note 3)	0	For setting, see Register EXCK0 (address 120 ₁₆).	Display clock setting
		1		



HS* (shown left) shows horizontal display start location that is register B/F (address 128₁₆) = 0 is set.

- Notes 1. The mark ○ around the status value means the reset status by the "L" level is input to \bar{AC} pin.
 2. The page in which data is written is controlled by the DAF bit. When set to "0", data is written into page 0, whereas when set to "1", data is written into page 1.
 3. Registers marked with (Note 3) are found only in page 0, therefore the register value does not change when the DAF bit is set to "1".
 4. Set up the horizontal and vertical display start location so that display range may not exceed it.
 Set the character code "FF₁₆" (blank without background) for the display RAM of the part which the display range exceeds.

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(5) Address 124₁₆

DA	Register	Contents		Remarks																				
		Status	Function																					
0	DSP0	0	The display mode (blanking mode) for line n on the display screen is set line-by-line, using DSPn (n = 0 to 11).	Sets the display mode of line 1.																				
		1																						
1	DSP1	0	The display mode is determined by the combination of registers BLK1 and BLK0 (address 128 ₁₆). Settings are given below.	Sets the display mode of line 2.																				
		1																						
2	DSP2	0	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>BLK1</th> <th>BLK0</th> <th>DSPn="0"</th> <th>DSPn="1"</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Matrix-outline border</td> <td>Matrix-outline</td> </tr> <tr> <td>0</td> <td>1</td> <td>Character</td> <td>Border</td> </tr> <tr> <td>1</td> <td>0</td> <td>Border</td> <td>Matrix-outline</td> </tr> <tr> <td>1</td> <td>1</td> <td>Matrix-outline</td> <td>Character</td> </tr> </tbody> </table>	BLK1	BLK0	DSPn="0"	DSPn="1"	0	0	Matrix-outline border	Matrix-outline	0	1	Character	Border	1	0	Border	Matrix-outline	1	1	Matrix-outline	Character	Sets the display mode of line 3.
BLK1	BLK0	DSPn="0"		DSPn="1"																				
0	0	Matrix-outline border	Matrix-outline																					
0	1	Character	Border																					
1	0	Border	Matrix-outline																					
1	1	Matrix-outline	Character																					
		1																						
3	DSP3	0	(At register BCOL = "0")	Sets the display mode of line 4.																				
		1																						
4	DSP4	0	For detail, see DISPLAY FORM1(1).	Sets the display mode of line 5.																				
		1																						
5	DSP5	0		Sets the display mode of line 6.																				
		1																						
6	DSP6	0		Sets the display mode of line 7.																				
		1																						
7	DSP7	0		Sets the display mode of line 8.																				
		1																						
8	DSP8	0		Sets the display mode of line 9.																				
		1																						
9	DSP9	0		Sets the display mode of line 10.																				
		1																						
A	DSP10 (Note 3)	0		Sets the display mode of line 11.																				
		1																						
B	DSP11 (Note 3)	0		Sets the display mode of line 12.																				
		1																						
C	TEST4	0	It should be fixed to "0".																					
		1	Can not be used.																					
D	PTC67 (Note 3)	0	P6 output (port P6) and P7 output (port P7).	P6 pin and P7 pin output control.																				
		1	B1 output and BLNK output.																					
E	TEST9 (Note 3)	0	Set to "0" in internal clock mode.																					
		1	Set to "1" in external clock mode.																					

Notes 1. The mark ○ around the status value means the reset status by the "L" level is input to AC pin.

2. The page in which data is written is controlled by the DAF bit. When set to "0", data is written into page 0, whereas when set to "1", data is written into page 1.

3. Registers marked with (Note 3) are found only in page 0, therefore the register value does not change when the DAF bit is set to "1".

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(6) Address 125₁₆

DA	Register	Contents		Remarks
		Status	Function	
0	LIN2	0	The vertical dot size for line n in the character dot lines (18 vertical lines) is set using LINn (n = 2 to 17).	Character size setting in the vertical direction for the 2nd line.
		1		
1	LIN3	0	Dot size can be selected between 2 types for each dot line. For dot size, see the below registers. Line 1 and lines 2 to 12 can be set independent of one another.	Character size setting in the vertical direction for the 3rd line.
		1		
2	LIN4	0		Character size setting in the vertical direction for the 4th line.
		1		
3	LIN5	0		Character size setting in the vertical direction for the 5th line.
		1		
4	LIN6	0		Character size setting in the vertical direction for the 6th line.
		1		
5	LIN7	0		Character size setting in the vertical direction for the 7th line.
		1		
6	LIN8	0		Character size setting in the vertical direction for the 8th line.
		1		
7	LIN9	0		Character size setting in the vertical direction for the 9th line.
		1		
8	V1SZ0	0	H: Cycle with the horizontal synchronizing pulse	Character size setting in the vertical direction for the 1st line. (display monitor 1 to 12 line)
		1		
9	V1SZ1	0		
		1		
A	VSZ1L0	0	H: Cycle with the horizontal synchronizing pulse	Character size setting in the vertical direction (display monitor 1 line) at "0" state in register LIN2 to LIN17 (address 125 ₁₆ , 126 ₁₆).
		1		
B	VSZ1L1	0		
		1		
C	VSZ1H0	0	H: Cycle with the horizontal synchronizing pulse	Character size setting in the vertical direction (display monitor 1 line) at "1" state in register LIN2 to LIN17 (address 125 ₁₆ , 126 ₁₆).
		1		
D	VSZ1H1	0		
		1		
E	TEST10 (Note 3)	0	It should be fixed to "0".	
		1	Can not be used.	

	LINn = "0"	LINn = "1"
1st line	Refer to VSZ1L0 and VSZ1L1	Refer to VSZ1H0 and VSZ1H1
2nd to 12th line	Refer to VSZ2L0 and VSZ2L1	Refer to VSZ2H0 and VSZ2H1

V1SZ1	V1SZ0	Vertical direction size
0	0	1H/dot
0	1	2H/dot
1	0	3H/dot
1	1	4H/dot

VSZ1L1	VSZ1L0	Vertical direction size
0	0	1H/dot
0	1	2H/dot
1	0	3H/dot
1	1	4H/dot

VSZ1H1	VSZ1H0	Vertical direction size
0	0	1H/dot
0	1	2H/dot
1	0	3H/dot
1	1	4H/dot

- Notes 1. The mark ○ around the status value means the reset status by the "L" level is input to AC pin.
 2. The page in which data is written is controlled by the DAF bit. When set to "0", data is written into page 0, whereas when set to "1", data is written into page 1.
 3. Registers marked with (Note 3) are found only in page 0, therefore the register value does not change when the DAF bit is set to "1".

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(7) Address 126₁₆

DA	Register	Contents		Remarks															
		Status	Function																
0	LIN10	⓪	The vertical dot size for line n in the character dot lines (18 vertical lines) is set using LINn (n = 2 to 17).	Character size setting in the vertical direction for the 10th line.															
		1																	
1	LIN11	⓪	Dot size can be selected between 2 types for each dot line.	Character size setting in the vertical direction for the 11th line.															
		1																	
2	LIN12	⓪	For dot size, see the below registers. Line 1 and lines 2 to 12 can be set independent of one another.	Character size setting in the vertical direction for the 12th line.															
		1																	
3	LIN13	⓪	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th></th> <th>LINn = "0"</th> <th>LINn = "1"</th> </tr> </thead> <tbody> <tr> <td>1st line</td> <td>Refer to VSZ1L0 and VSZ1L1</td> <td>Refer to VSZ1H0 and VSZ1H1</td> </tr> <tr> <td>2nd to 12th line</td> <td>Refer to VSZ2L0 and VSZ2L1</td> <td>Refer to VSZ2H0 and VSZ2H1</td> </tr> </tbody> </table>		LINn = "0"	LINn = "1"	1st line	Refer to VSZ1L0 and VSZ1L1	Refer to VSZ1H0 and VSZ1H1	2nd to 12th line	Refer to VSZ2L0 and VSZ2L1	Refer to VSZ2H0 and VSZ2H1	Character size setting in the vertical direction for the 13th line.						
				LINn = "0"	LINn = "1"														
1st line	Refer to VSZ1L0 and VSZ1L1	Refer to VSZ1H0 and VSZ1H1																	
2nd to 12th line	Refer to VSZ2L0 and VSZ2L1	Refer to VSZ2H0 and VSZ2H1																	
1																			
4	LIN14	⓪		Character size setting in the vertical direction for the 14th line.															
		1																	
5	LIN15	⓪		Character size setting in the vertical direction for the 15th line.															
		1																	
6	LIN16	⓪		Character size setting in the vertical direction for the 16th line.															
		1																	
7	LIN17	⓪		Character size setting in the vertical direction for the 17th line.															
		1																	
8	V18SZ0	⓪	H: Cycle with the horizontal synchronizing pulse	Character size setting in the vertical direction for the 18th line. (display monitor 1 to 12 line)															
		1																	
9	V18SZ1	⓪	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>V18SZ1</th> <th>V18SZ0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table>	V18SZ1	V18SZ0	Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot	1	1	4H/dot	
		V18SZ1		V18SZ0	Vertical direction size														
0	0	1H/dot																	
0	1	2H/dot																	
1	0	3H/dot																	
1	1	4H/dot																	
1																			
A	VSZ2L0	⓪	H: Cycle with the horizontal synchronizing pulse	Character size setting in the vertical direction (display monitor for 2 to 12 line) at "0" state in register LIN2 to LIN17 (address 125 ₁₆ , 126 ₁₆).															
		1																	
B	VSZ2L1	⓪	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>VSZ2L1</th> <th>VSZ2L0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table>	VSZ2L1	VSZ2L0	Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot	1	1	4H/dot	
		VSZ2L1		VSZ2L0	Vertical direction size														
0	0	1H/dot																	
0	1	2H/dot																	
1	0	3H/dot																	
1	1	4H/dot																	
1																			
C	VSZ2H0	⓪	H: Cycle with the horizontal synchronizing pulse	Character size setting in the vertical direction (display monitor for 2 to 12 line) at "0" state in register LIN2 to LIN17 (address 125 ₁₆ , 126 ₁₆).															
		1																	
D	VSZ2H1	⓪	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>VSZ2H1</th> <th>VSZ2H0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table>	VSZ2H1	VSZ2H0	Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot	1	1	4H/dot	
		VSZ2H1		VSZ2H0	Vertical direction size														
0	0	1H/dot																	
0	1	2H/dot																	
1	0	3H/dot																	
1	1	4H/dot																	
1																			
E	POPUP (Note 3)	⓪	Page 1 priority display	Sets the priority page for when 2 pages are displayed at the same time. The setting is effective only when the standard display mode is set as MODE0 = "0" , MODE1 = "0". See "DISPLAY FORM 2" .															
		1	Page 0 priority display																

- Notes 1. The mark ⓪ around the status value means the reset status by the "L" level is input to $\bar{A}C$ pin.
2. The page in which data is written is controlled by the DAF bit. When set to "0", data is written into page 0, whereas when set to "1", data is written into page 1.
3. Registers marked with (Note 3) are found only in page 0, therefore the register value does not change when the DAF bit is set to "1".

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(8) Address 127₁₆

DA	Register	Contents				Remarks																																				
		Status	Function																																							
0	RR	⓪	<table border="1"> <thead> <tr> <th>RB</th> <th>RG</th> <th>RR</th> <th>Color</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Black</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Red</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>Green</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Yellow</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>Blue</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>Magenta</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>Cyan</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>White</td> </tr> </tbody> </table>			RB	RG	RR	Color	0	0	0	Black	0	0	1	Red	0	1	0	Green	0	1	1	Yellow	1	0	0	Blue	1	0	1	Magenta	1	1	0	Cyan	1	1	1	White	Sets the raster color of all blankings.
		RB	RG	RR	Color																																					
0	0	0	Black																																							
0	0	1	Red																																							
0	1	0	Green																																							
0	1	1	Yellow																																							
1	0	0	Blue																																							
1	0	1	Magenta																																							
1	1	0	Cyan																																							
1	1	1	White																																							
1																																										
1	RG	⓪	<table border="1"> <thead> <tr> <th>FB</th> <th>FG</th> <th>FR</th> <th>Color</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Black</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Red</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>Green</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Yellow</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>Blue</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>Magenta</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>Cyan</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>White</td> </tr> </tbody> </table>			FB	FG	FR	Color	0	0	0	Black	0	0	1	Red	0	1	0	Green	0	1	1	Yellow	1	0	0	Blue	1	0	1	Magenta	1	1	0	Cyan	1	1	1	White	Sets the blanking color of the Border size, or the shadow size.
		FB	FG	FR	Color																																					
0	0	0	Black																																							
0	0	1	Red																																							
0	1	0	Green																																							
0	1	1	Yellow																																							
1	0	0	Blue																																							
1	0	1	Magenta																																							
1	1	0	Cyan																																							
1	1	1	White																																							
1																																										
2	RB	⓪																																								
		1																																								
3	FR	⓪																																								
		1																																								
4	FG	⓪																																								
		1																																								
5	FB	⓪																																								
		1																																								
6	TEST6	⓪	It should be fixed to "0".																																							
		1	Can not be used.																																							
7	TEST7	⓪	It should be fixed to "0".																																							
		1	Can not be used.																																							
8	TEST8	⓪	It should be fixed to "0".																																							
		1	Can not be used.																																							
9	BETA14	⓪	Matrix-outline display (12 × 18 dot)																																							
		1	Matrix-outline display (14 × 18 dot)																																							
A	HSZ10	⓪	<table border="1"> <thead> <tr> <th>HSZ10</th> <th>Horizontal direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1T/dot</td> </tr> <tr> <td>1</td> <td>2T/dot</td> </tr> </tbody> </table>			HSZ10	Horizontal direction size	0	1T/dot	1	2T/dot	Character size setting in the horizontal direction for the first line. T : Display frequency cycle																														
		HSZ10	Horizontal direction size																																							
0	1T/dot																																									
1	2T/dot																																									
1																																										
B	TEST11	⓪	It should be fixed to "0".																																							
		1	Can not be used.																																							
C	HSZ20	⓪	<table border="1"> <thead> <tr> <th>HSZ20</th> <th>Horizontal direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1T/dot</td> </tr> <tr> <td>1</td> <td>2T/dot</td> </tr> </tbody> </table>			HSZ20	Horizontal direction size	0	1T/dot	1	2T/dot																															
		HSZ20	Horizontal direction size																																							
0	1T/dot																																									
1	2T/dot																																									
1																																										
D	TEST12	⓪	It should be fixed to "0".			Character size setting in the horizontal direction for the 2nd line to 12th line. T : Display frequency cycle																																				
		1	Can not be used.																																							
E	MODE0 (Note 3)	⓪	<table border="1"> <thead> <tr> <th>MODE1</th> <th>MODE0</th> <th>Output system</th> <th>Display mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1 system</td> <td>Standard.(Note4)</td> </tr> <tr> <td>0</td> <td>1</td> <td>1 system</td> <td>AND</td> </tr> <tr> <td>1</td> <td>0</td> <td>2 system</td> <td>—</td> </tr> <tr> <td>1</td> <td>1</td> <td>1 system</td> <td>OR</td> </tr> </tbody> </table>			MODE1	MODE0	Output system	Display mode	0	0	1 system	Standard.(Note4)	0	1	1 system	AND	1	0	2 system	—	1	1	1 system	OR	Sets the RGB signal output system and the display mode for when 2 pages are displayed at the same time. See "DISPLAY FORM 2". MODE1(address128 ₁₆) .																
		MODE1	MODE0	Output system	Display mode																																					
0	0	1 system	Standard.(Note4)																																							
0	1	1 system	AND																																							
1	0	2 system	—																																							
1	1	1 system	OR																																							
1																																										

Notes 1. The mark ⓪ around the status value means the reset status by the "L" level is input to $\bar{A}C$ pin.
2. The page in which data is written is controlled by the DAF bit. When set to "0", data is written into page 0, whereas when set to "1", data is written into page 1.
3. Registers marked with (Note 3) are found only in page 0, therefore the register value does not change when the DAF bit is set to "1".
4. 2 way settings are available by POPUP (address 126₁₆).

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(9) Address 128₁₆

DA	Register	Contents		Remarks																	
		Status	Function																		
0	BCOL	0	Blanking of BLK0, BLK1	Sets all raster blanking																	
		1	All raster blanking																		
1	B/F (Note 3)	0	Synchronize with the leading edge of horizontal synchronization.	Synchronize with the front porch or back porch of the horizontal synchronazation signal.																	
		1	Synchronize with the trailing edge of horizontal synchronization.																		
2	VMASK (Note 3)	0	Do not mask by VERT input signal	Set mask at phase comparison operating.																	
		1	Mask by VERT input signal																		
3	POLV (Note 3)	0	VERT pin is negative polarity	Set VERT pin polarity.																	
		1	VERT pin is positive polarity																		
4	POLH (Note 3)	0	HOR pin is negative polarity	Set HOR pin polarity.																	
		1	HOR pin is positive polarity																		
5	BLK0	0	<table border="1"> <thead> <tr> <th>BLK1</th> <th>BLK0</th> <th>Blanking mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Matrix-outline size</td> </tr> <tr> <td>0</td> <td>1</td> <td>Character size</td> </tr> <tr> <td>1</td> <td>0</td> <td>Border size</td> </tr> <tr> <td>1</td> <td>1</td> <td>Matrix-outline size</td> </tr> </tbody> </table>	BLK1	BLK0	Blanking mode	0	0	Matrix-outline size	0	1	Character size	1	0	Border size	1	1	Matrix-outline size	Set blanking mode. See "DISPLAY SHAPE 2".		
BLK1	BLK0	Blanking mode																			
0	0	Matrix-outline size																			
0	1	Character size																			
1	0	Border size																			
1	1	Matrix-outline size																			
1	(When DSPn (address 124 ₁₆) = "0")																				
6	BLK1	0																			
		1																			
7	SYAD	0	Border display of character	See "DISPLAY FORM1 (2)".																	
		1	Shadow display of character																		
8	RAMERS	0	RAM not erased	When register RAMERS is set to "1", do not stop the display clock. There is no need to reset because there is no register for this bit.																	
		1	RAM erased																		
9	STOP	0	Oscillation of clock for display	It is a test bit (TEST13) in the page 1 register, therefore fix it to "0".																	
		1	Stop the oscillation of clock for display																		
A	DSPON	0	Display OFF																		
		1	Display ON																		
B	BLINK0	0	<table border="1"> <thead> <tr> <th colspan="2">BLINK</th> <th>Duty</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td rowspan="2">Blinking OFF</td> </tr> <tr> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>25%</td> </tr> <tr> <td>1</td> <td>0</td> <td>50%</td> </tr> <tr> <td>1</td> <td>1</td> <td>75%</td> </tr> </tbody> </table>	BLINK		Duty	1	0	Blinking OFF	0	0	0	1	25%	1	0	50%	1	1	75%	Set blinking duty ratio.
		BLINK		Duty																	
1	0	Blinking OFF																			
0	0																				
0	1	25%																			
1	0	50%																			
1	1	75%																			
1																					
C	BLINK1	0																			
		1																			
D	BLINK2	0	Divided into 64 of vertical synchronous signal	Set blinking frequency.																	
		1	Divided into 32 of vertical synchronous signal																		
E	MODE1 (Note 3)	0	For setting, see MODE0 (address 127 ₁₆).	Sets the RGB signal output system and the display mode for when 2 pages are displayed at the same time.																	
		1																			

Notes 1. The mark ○ around the status value means the reset status by the "L" level is input to AC pin.

2. The page in which data is written is controlled by the DAF bit. When set to "0", data is written into page 0, whereas when set to "1", data is written into page 1.

3. Registers marked with (Note 3) are found only in page 0, therefore the register value does not change when the DAF bit is set to "1".

REGISTER SUPPLEMENTARY DESCRIPTION

(1) Setting external clock input and display frequency mode
 Setting external clock input and display frequency mode (by use of EXCK0 (120₁₆), EXCK1 (123₁₆) and DIV10 to DIV0 (120₁₆), as explained here following.

(a) When (EXCK1, EXCK0) = (0, 0)External clock mode 1
 Fosc = 6.3 to 80 MHz (V_{DD} = 4.75 to 5.25 V)
 Fosc = 6.3 to 40 MHz (V_{DD} = 2.50 to 3.50 V)
 Input from the TCK pin a constant-period continuous external clock that synchronizes with the horizontal synchronous signal. And input from HOR pin a constant period continuous horizontal synchronous signal.
 Never stop inputting the clock while displaying.
 Do not have to set a display frequency because the clock just as it is entered from outside is used as the display clock.

(b) When (EXCK1, EXCK0) = (0, 1)Internal clock mode
 Fosc = 20 to 110 MHz (V_{DD} = 4.75 to 5.25 V)
 Clock input from the TCK pin is unnecessary. The multiply clock of the internally generated horizontal synchronous signal is used as the display clock.
 The display frequency is set by setting the multiply value of the horizontal synchronous frequency (of the display frequency) in DIV10 to DIV0 (address 120₁₆). Also, set the display frequency range. (See the next page.)
 Display frequency is calculated using the below expression.

$$\text{Display frequency} = \text{Horizontal synchronous frequency} \times \text{Multiply value}$$

(c) When (EXCK1, EXCK0) = (1, 0) Setting disabled

(d) When (EXCK1, EXCK0) = (1, 1)External clock mode 2
 Fosc = 20 to 110 MHz (V_{DD} = 4.75 to 5.25 V)
 Input from the TCK pin a constant-period continuous external clock that synchronizes with the horizontal synchronous signal. And input from HOR pin a constant-period continuous horizontal synchronous signal.
 Never stop inputting the clock while displaying.
 An internal clock which is in sync with the external input clock is used as the display clock.
 Because the display frequency equals the external clock frequency, set N1 (division value) that satisfies the below expressions to DIV10 to DIV0 (address 120₁₆) for make the display frequency is equal to the external clock frequency.

$$N1 = \text{external clock frequency} / \text{horizontal synchronous frequency}$$

$$N1 = \sum_{n=0}^{10} 2^n \text{DIV}_n$$

Also, set the display frequency range. (See the next page.)

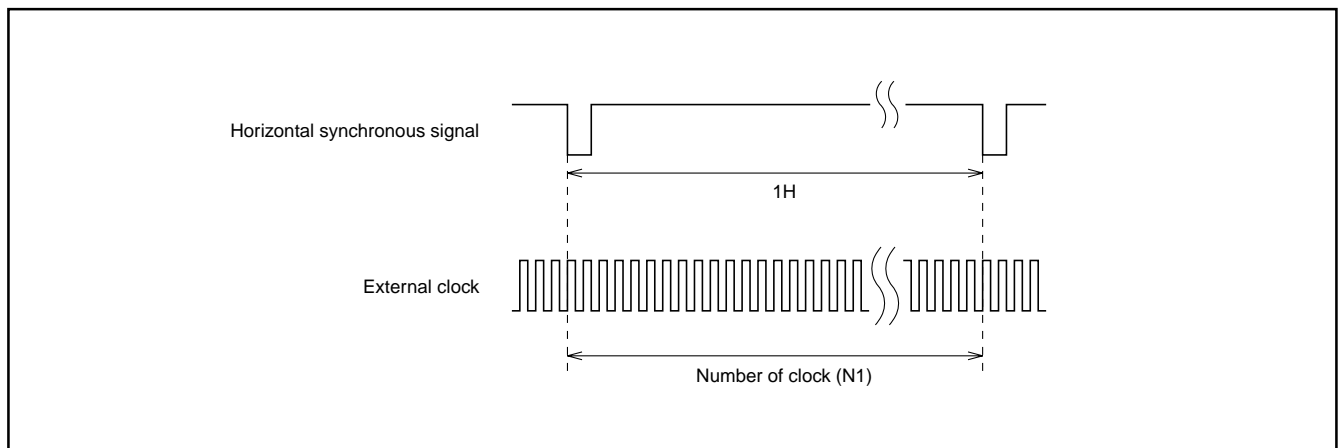


Fig. 4 Example of external clock input

(2) To set display frequency range

Whenever setting display frequency (when EXCK1 = "0", EXCK0 = "1", or EXCK1 = "1", EXCK0 = "1"), always set the display frequency range in accordance with the display frequency. This range is set from DIVS0, DIVS1, DIVS2 (address 120₁₆), RSEL0 (address 121₁₆) and RSEL1 (address 122₁₆). Frequency ranges are given here below.

RSEL1	RSEL0	DIVS2	DIVS1	DIVS0	Display frequency range(MHz)
1	1	0	0	0	100.0 to 110.0
1	0	0	0	0	—
0	1	0	0	0	92.0 to 100.0
0	0	0	0	0	73.0 to 92.0
1	1	0	0	1	66.5 to 73.0
1	0	0	0	1	—
0	1	0	0	1	61.0 to 66.5
0	0	0	0	1	49.0 to 61.0
1	1	0	1	0	—
1	0	0	1	0	—
0	1	0	1	0	45.5 to 49.0
0	0	0	1	0	36.5 to 45.5
1	1	0	1	1	33.5 to 36.5
1	0	0	1	1	—
0	1	0	1	1	30.5 to 33.5
0	0	0	1	1	24.5 to 30.5
1	1	1	0	0	—
1	0	1	0	0	—
0	1	1	0	0	23.0 to 24.5
0	0	1	0	0	20.0 to 23.0

(3) Notes on setting display frequency

To change external clock (display) frequency or horizontal synchronization frequency, always use the following procedures.

To set EXCK1 = "0", EXCK0 = "1"

- Turn the display OFF. ... DSPON (address 128₁₆) = "0"
- Set the display frequency. ... Set from DIV10 to DIV0, DIVS0, DIVS1, DIVS2 (address 120₁₆), RSEL0 (address 121₁₆) and RSEL1 (address 122₁₆).
- Wait 20 ms while the horizontal synchronization signal is being input.
- Turn the display ON. ... DSPON (address 128₁₆) = "1"

To set EXCK1 = "1", EXCK0 = "1"

- Turn the display OFF. ... DSPON (address 128₁₆) = "0"
- Set the display frequency. ... Set from DIV10 to DIV0, DIVS0, DIVS1, DIVS2 (address 120₁₆), RSEL0 (address 121₁₆) and RSEL1 (address 122₁₆).
- Wait 20 ms while the horizontal synchronization signal and external clock are being input.
- Turn the display ON. ... DSPON (address 128₁₆) = "1"

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

DISPLAY FORM 1

M35076-XXXSP has the following four display forms.

(1) Blanking mode

Character size

: Blanking same as the character size.

Border size

: Blanking the background as a size from character.

Matrix-outline size

: Blanking the background 12 × 18 dot.

All blanking size

: When set register BCOL to "1", all raster area is blanking.

The display mode and blanking mode can be set line-by-line, as follows, from registers BCOL, BLK1, BLK0 (address 128₁₆), DSP0 to DSP11 (address 124₁₆).

BCOL	BLK1	BLK0	Line of DSPn = "0"		Line of DSPn = "1"	
			Display mode	Blanking mode	Display mode	Blanking mode
0	0	0	All matrix-outline border display	All matrix-outline size	All matrix-outline display	All matrix-outline size
	0	1	Character display	Character size	Border display	Border size
	1	0	Border display	Border size	All matrix-outline display	All matrix-outlinesize
	1	1	All matrix-outline display	All matrix-outline size	Character display	Character size
1	0	0	All matrix-outline border display	All blanking size	All matrix-outline display	All blanking size
	0	1	Character display		Border display	
	1	0	Border display		All matrix-outline display	
	1	1	All matrix-outline display		Character display	

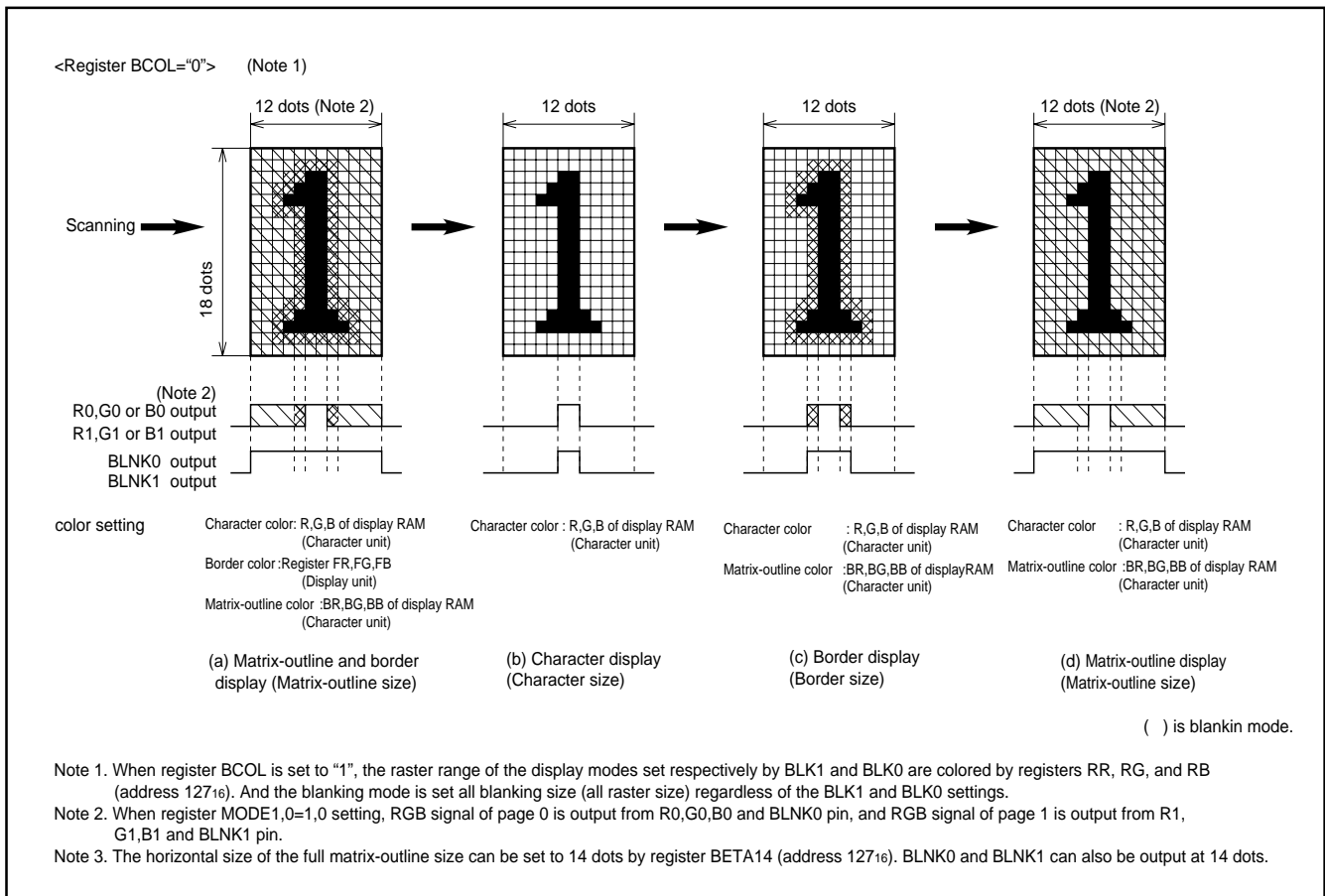


Fig. 5 Example of R0,G0,B0,BLNK0,R1,G1,B1 and BLNK1 signal output

(2) Shadow display

When border display mode, if set SYAD (address 128₁₆) = "0" to "1", it change to shadow display mode.

Border and shadow display are shown below.

Set shadow display color by BR, BG or BB of display RAM or by register FR, FG and FB (address 127₁₆).

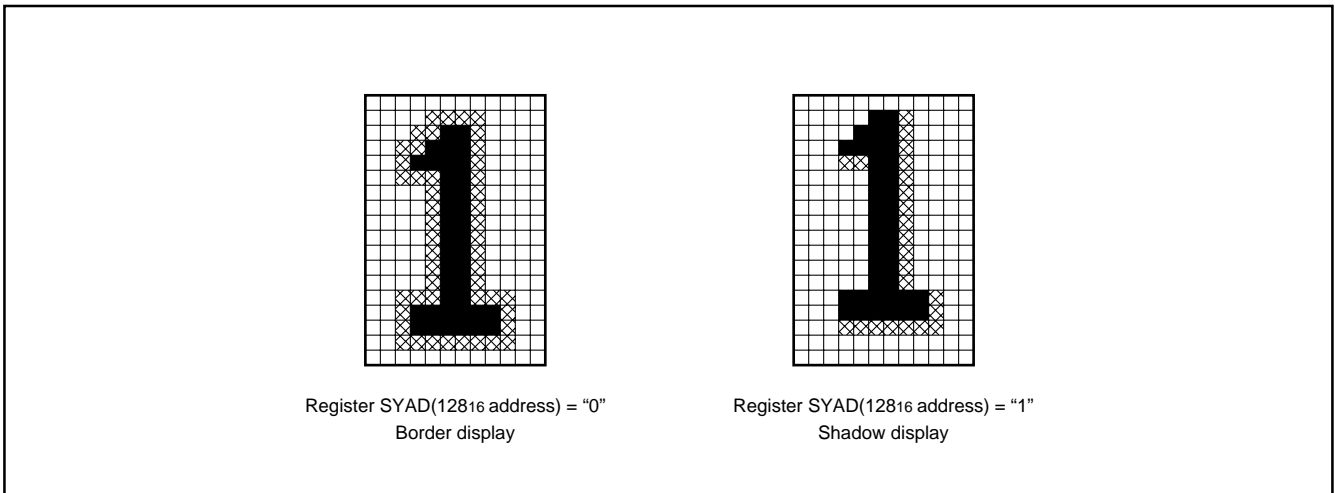


Fig. 6 Border and shadow display

DISPLAY FORM 2

This IC can display both page 0 and page 1 at the same time.

Page 0: Set the DAF bit in each addresses to "0".

Page 1: Set the DAF bit in each addresses to "1".

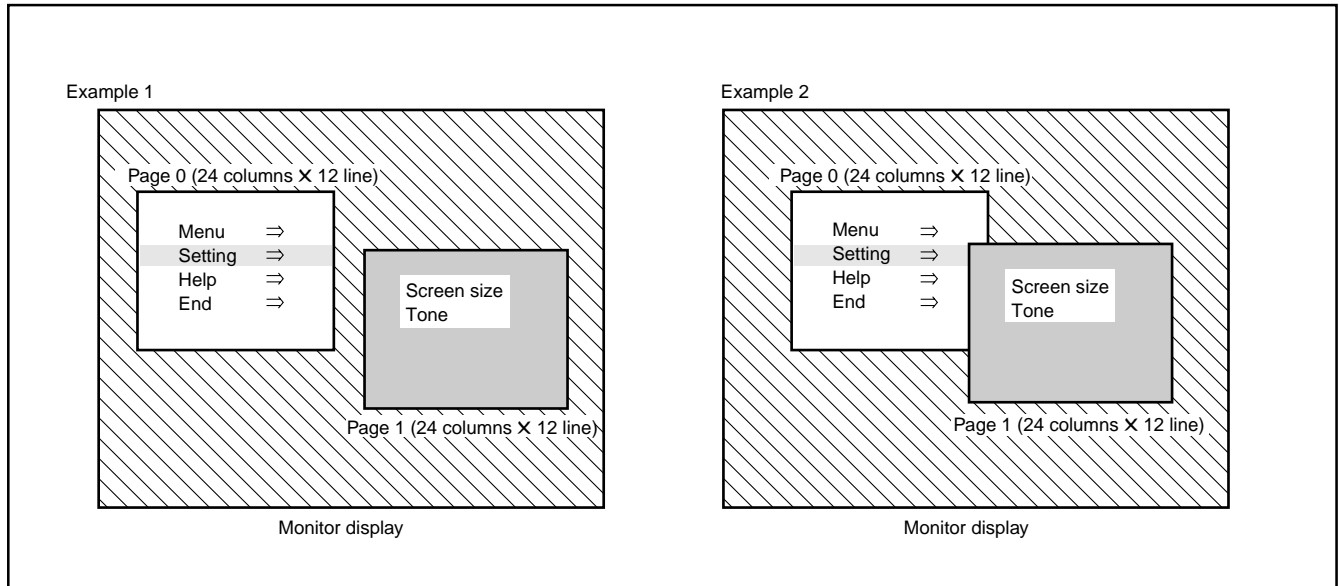


Fig. 7 Example of 2 pages display

Example 1: Display position, display size, color, etc., can be freely set for each page, and the 2 pages can be displayed on top of each other or side-by-side.

Example 2: RGB output of two pages can be outputted by one line or two lines by registers MODE0 (address 127₁₆) and MODE1 (address 128₁₆) and POPUP (address 126₁₆). And, when the display range of the 2 pages overlap on the monitor screen at the time of an one-line output, they can perform the following displays. (The POPUP register is effective only when MODE0 = "0" and MODE1 = "0".)

MODE1	MODE0	POPUP	Output system	Display mode
0	0	0	1 system	Standard (Page 1 priority)
		1	1 system	Standard (Page 0 priority)
0	1	—	1 system	AND
1	0	—	2 systems	—
1	1	—	1 system	OR

(1) Output system

- (a) 1 system : Output RBG signal of both of page 0 and 1 from R0,G0,B0 and BLNK0 pin (For overlapping areas, refer to below.)
- (b) 2 systems : RBG signal of page 0 is output from R0,G0,B0 and BLNK0 pin, RBG signal of page 1 is output from R1,G1,B1 and BLNK1 pin.

(2) Display mode (Overlapping areas of Page 0 and 1)

- (a) Standard (page 1 priority).. Page 1 has priority in overlapping areas. Page 0 is not displayed in those areas.
- (b) Standard (page 0 priority).. Page 0 has priority in overlapping areas. Page 1 is not displayed in those areas.
- (c) AND In overlapping areas, the RGB output of the 2 pages is AND processed and output.
- (d) OR In overlapping areas, the RGB output of the 2 pages is OR processed and output.

Note : Set 0 (port output) to control register PTC2, PTC4 and PT67 except at 2 systems output setting (MODE1=1,MODE0=0.)

CHARACTER FONT

Images are composed on a 12 X 18 dot matrix, and characters can be linked vertically and horizontally with other characters to allow the display the continuous symbols.

Character code FF₁₆ is fixed as a blank without background. Therefore, cannot register a character font in this code.

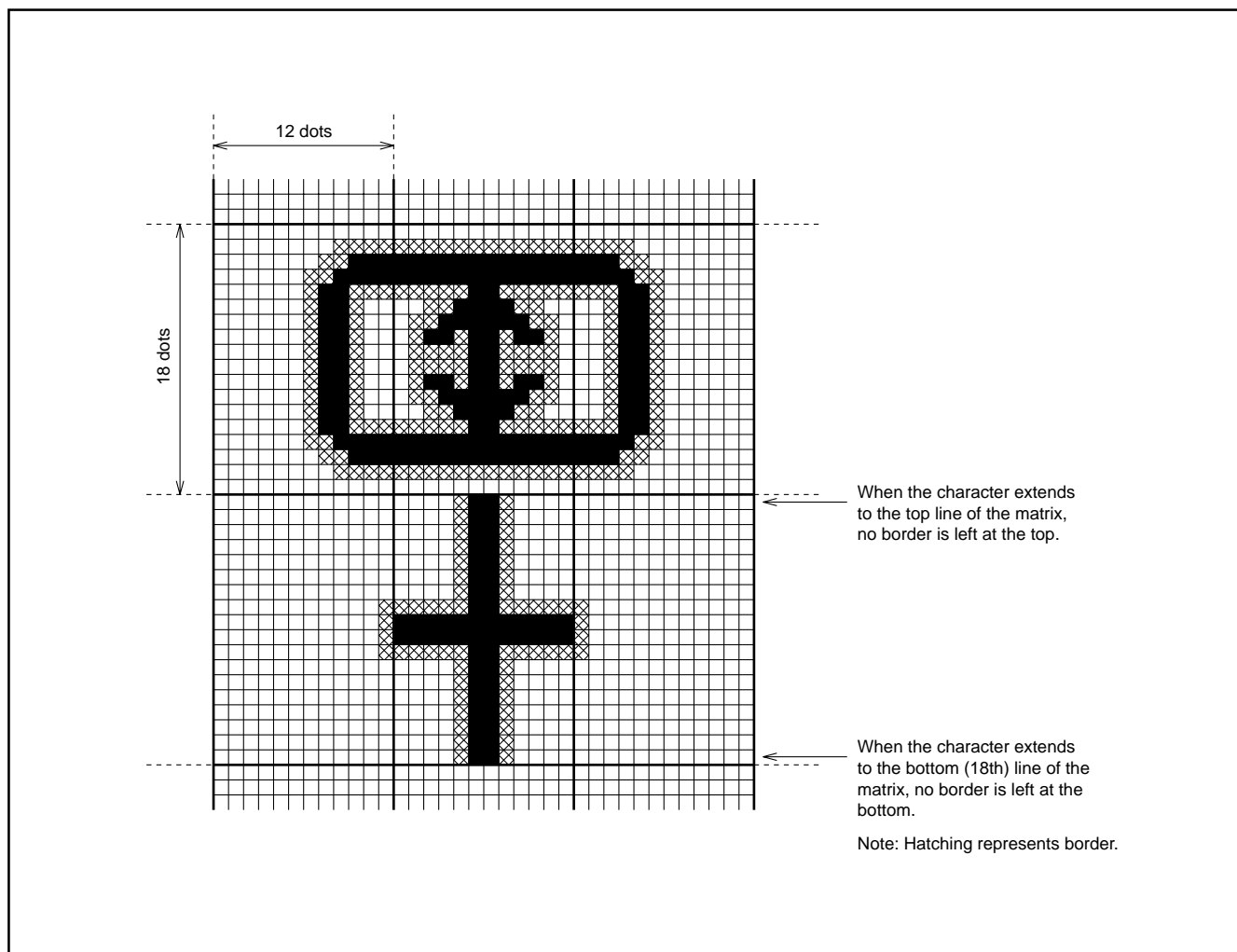


Fig. 8 Example of border display

DATA INPUT EXAMPLE

Data of display RAM and display control registers can be set by the 16-bit serial input function or the I²C-BUS serial input function. Example of data setting is shown in Figure 9 (at EXCK0 = "1", EXCK1 = "0" setting).

Data input example (M35076-XXXSP)																	
Address/data	DAF (Note1)	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	Remarks
200m sec hold																	
System set up (Note 4)																	
Address 12016	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	Address setting
Data 12016	0	1	DIVS2	DIVS1	DIVS0	DIV10	DIV9	DIV8	DIV7	DIV6	DIV5	DIV4	DIV3	DIV2	DIV1	DIV0	Frequency value setting (Note2)
Data 12116	0	RSEL0	PTD7	PTD6	1	PTD4	1	PTD2	1	1	1	0	1	0	1	1	Output setting
Data 12216	0	RSEL1	0	0	0	HP10	HP9	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0	Horizontal display location setting
Data 12316	0	0	0	0	0	0	VP9	VP8	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0	Vertical display location setting
Data 12416	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Display form setting
Data 12516	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Character size setting
Data 12616	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Character size setting
Data 12716	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Color, character size setting
Data 12816	0	0	0	0	0	0	0	0	0	0	0	POLH	POLV	0	0	0	Page 0 display OFF
Address 12216	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	0	Address setting
Data 12216	1	0	0	0	0	HP10	HP9	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0	Horizontal display location setting
Data 12316	1	0	0	0	0	0	VP9	VP8	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0	Vertical display location setting
Data 12416	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Display form setting
Data 12516	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Character size setting
Data 12616	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Character size setting
Data 12716	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Color, character size setting
Data 12816	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Page 1 display OFF
200m sec hold																	
Be stable / Waiting time																	
Data 00016	0	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0	Character setting
⋮	⋮	Background coloring			Blink-ing	Character color			Character code								
Data 11F16	0	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0	
Address 00016	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Character setting
Data 00016	1	BB	BG	BR	BLINK	B	G	R	0	C6	C5	C4	C3	C2	C1	C0	
⋮	⋮	Background coloring			Blink-ing	Character color			⋮	Character code							
Data 11F16	1	BB	BG	BR	BLINK	B	0	R	0	C6	C5	C4	C3	C2	C1	C0	Character setting
Address 12816	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	0	
Data 12816	1	0	0	0	0	1	0	0	0	1	1	0	0	0	0	0	
Address 12816	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	0	Address setting
Data 12816	0	0	0	0	0	1	0	0	0	1	1	POLH	POLV	0	0	0	Page 0 display ON Display form setting (Note 3)

- Notes 1 : The page in which data is written is controlled by the address. To write data into page 0, set "0". To write data into page 1, set "1".
 2 : Input a continuous clock of constant period from the TCK pin. Also, input a horizontal synchronous signal into the HOR pin and a vertical synchronous signal into the VERT pin.
 3 : Matrix-outline display in this data.
 4 : Secure the waiting time of 200ms after releasing AC, and set data from setting the display frequency (setting of the register).
 5 : Set data to display RAM at internal clock (display clock) is stabilized.

Fig 9. Example of data setting

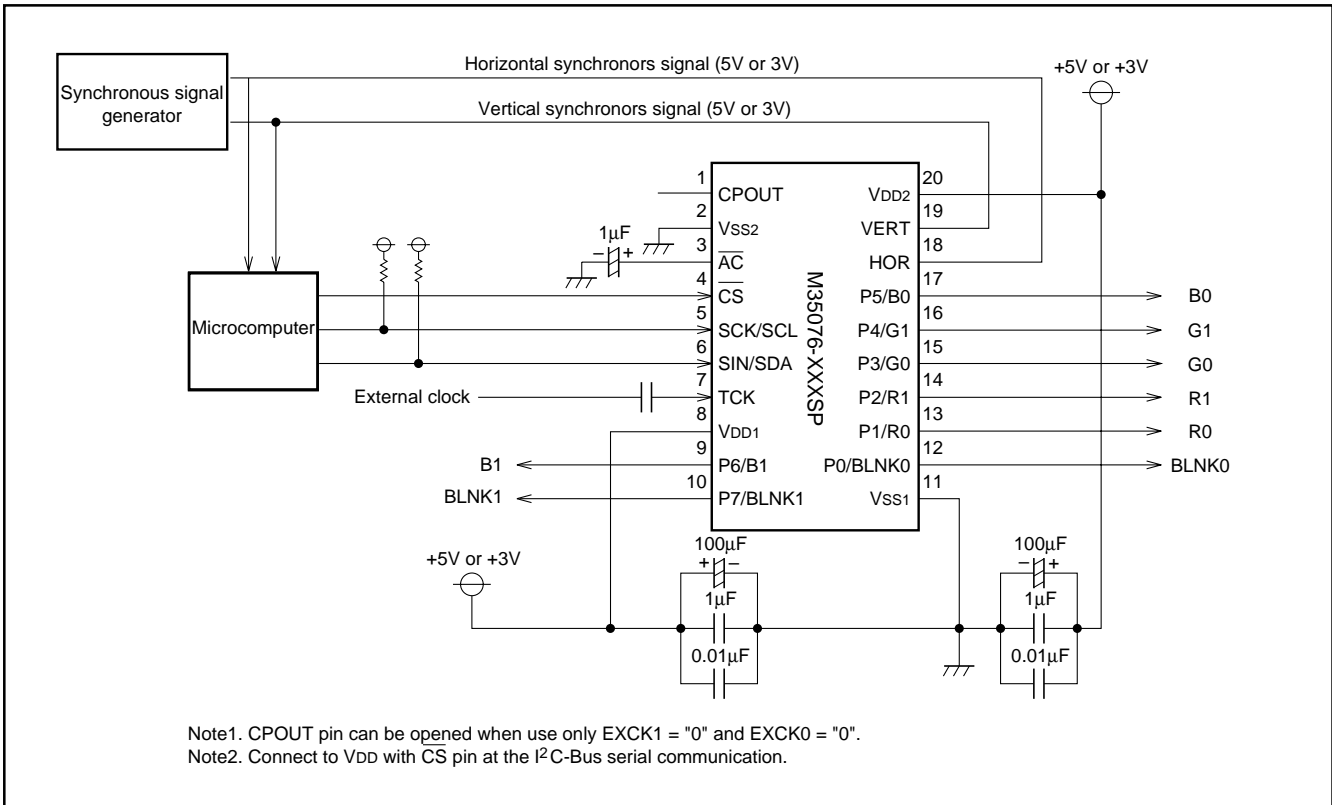


Fig 10. Example of the M35076-XXXSP peripheral circuit (External clock mode 1. At EXCK1 = "0", EXCK0 = "0")

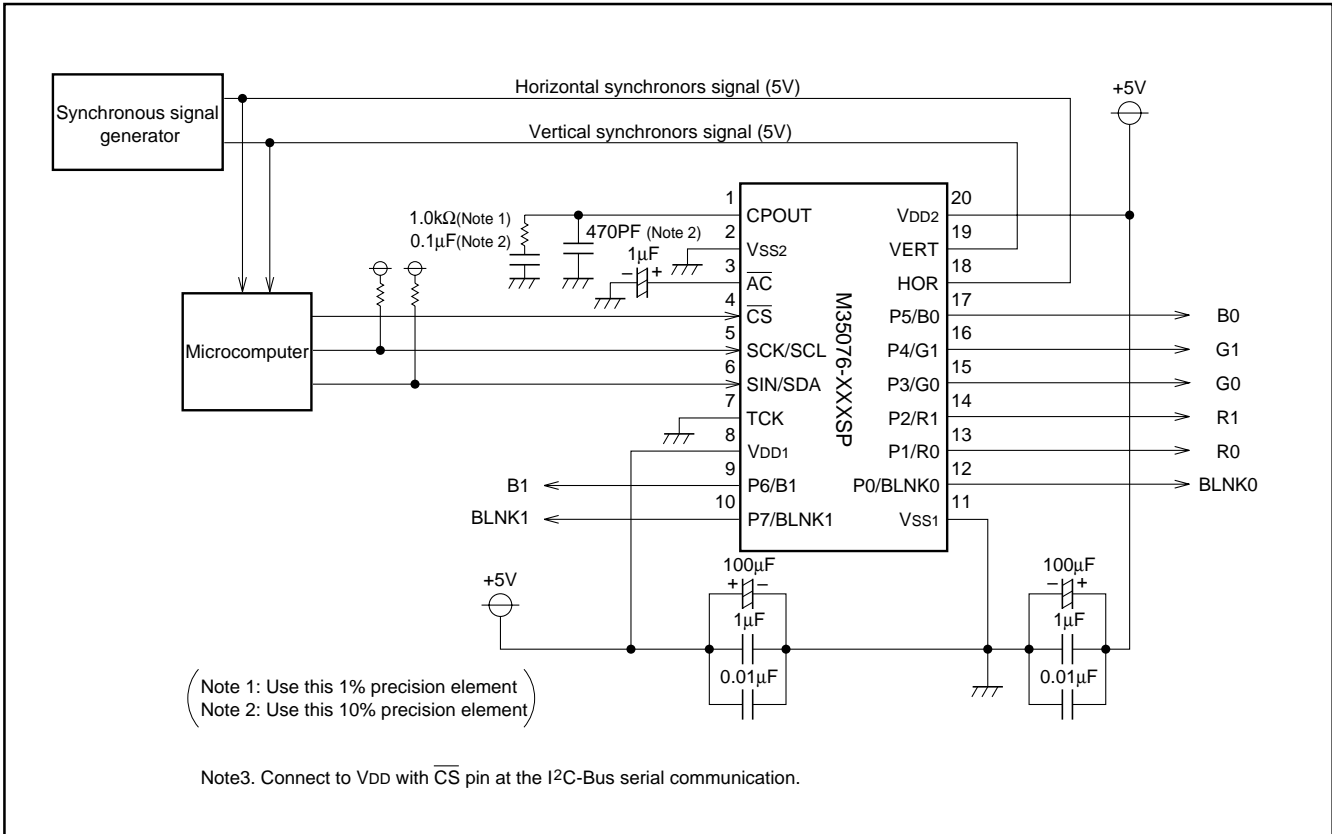


Fig 11. Example of the M35076-XXXSP peripheral circuit (Internal clock mode. At EXCK1 = "0", EXCK0 = "1")

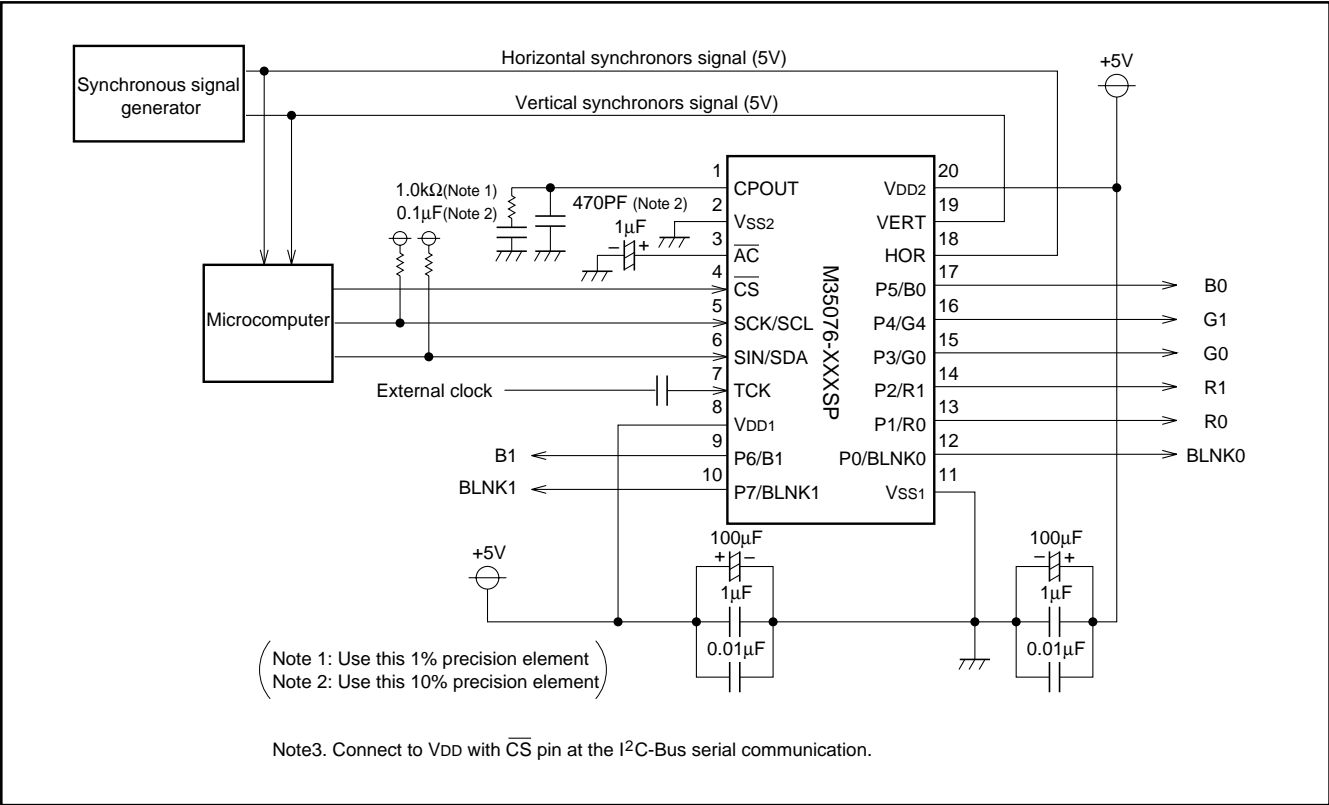


Fig 12. Example of the M35076-XXXSP circuit (External clock mode 2. At EXCK1 = "1", EXCK0 = "1")

(2)Timing requirements

Data input

Symbol	Parameter	Limits			Unit	Remarks
		Min.	Typ.	Max.		
$t_w(\text{SCK})$	SCK width	200	—	—	ns	See Figure 14
$t_{su}(\overline{\text{CS}})$	$\overline{\text{CS}}$ setup time	200	—	—	ns	
$t_h(\overline{\text{CS}})$	$\overline{\text{CS}}$ hold time	2	—	—	μs	
$t_{su}(\text{SIN})$	SIN setup time	200	—	—	ns	
$t_h(\text{SIN})$	SIN hold time	200	—	—	ns	
t_{word}	1 word writing time	10	—	—	μs	

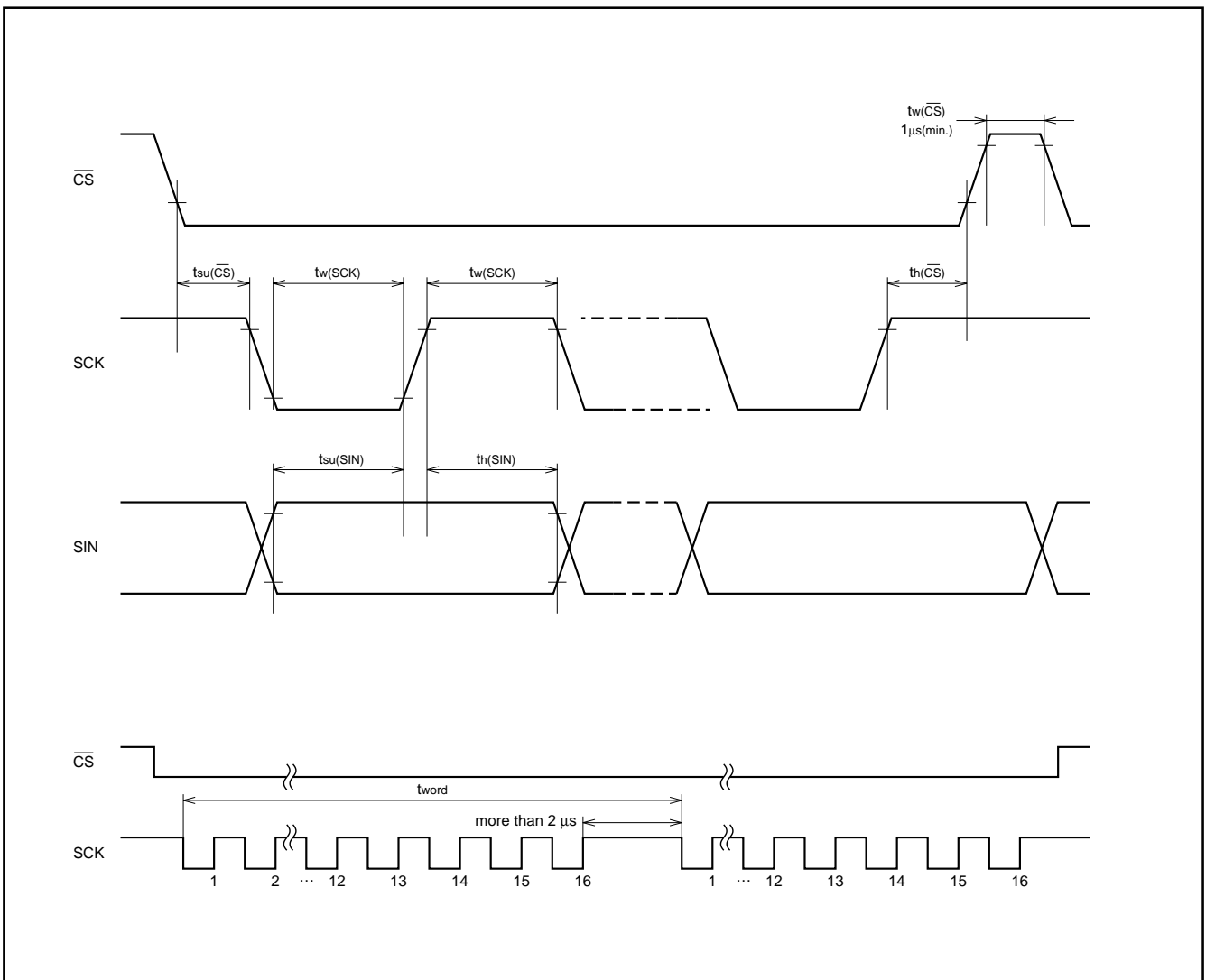


Fig. 14 Serial input timing requirements

DATA INPUT 2

(1) The I²C-Bus communication function (at VDD=5V only)

This IC has a built-in data transmission interface which utilizes 2 unidirectional buses. In communications, this IC functions as a slave reception device. Set \overline{CS} pin to "H" level at the I²C-Bus serial input communication.

The IC is synchronized with the serial clock (SCL) sent from the master device and receives the data (SDA). Communications are controlled from the start/stop states. Also, always input the control byte after attaining the start state.

The below chart shows the start/stop state and control byte configuration.

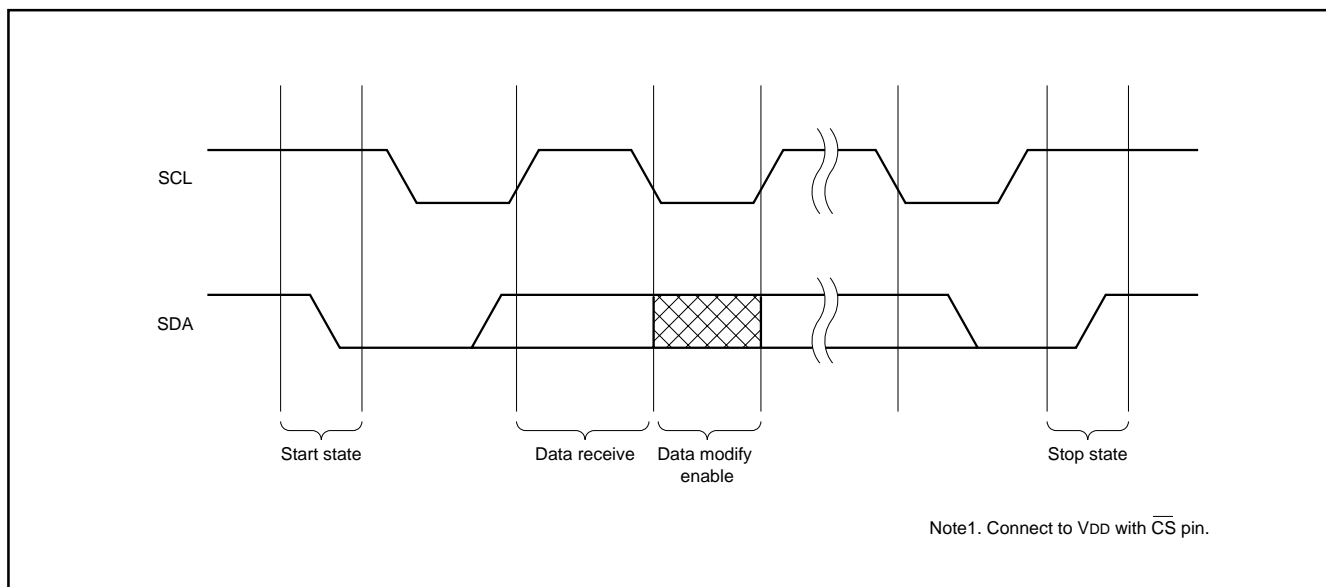


Fig. 15 Start state / Stop state



Fig. 16 Control byte configuration

(2) Data input (Sequence)

- (a) Addresses are consists of 16 bits.
- (b) Data is consists of 16 bits.
- (c) Addresses and data are communicated in 8-bit units. Input the lower 8 bits before the upper 8 bits. Make input from the MSB side.
- (d) After the start state has been attained and the control byte (7CH) received, the next 16 bits (2 bytes) are for inputting the address. Addresses are increased in increments for every 16 bits (2 bytes) of data input thereafter. As a result, it is not necessary to input the address from the second data.

Note: During external synchronous, stop the external clock input from the TCK pin while inputting data.

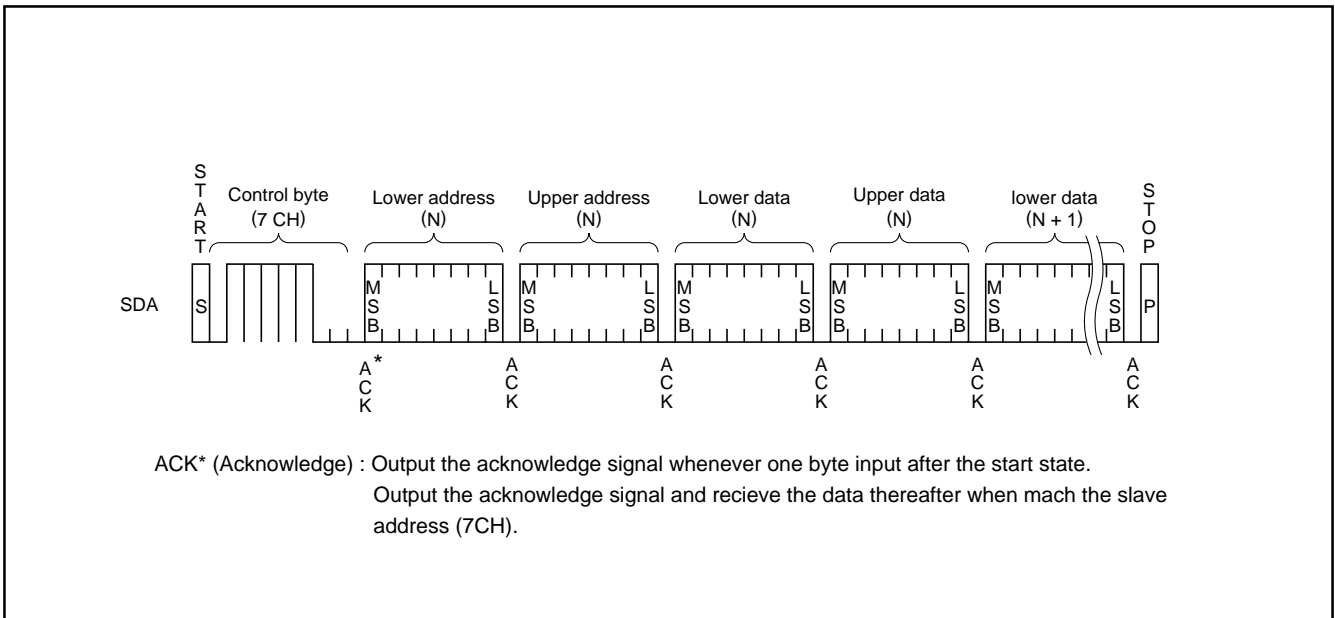


Fig. 17 Data input sequence

(3) Timing requirement

Data input

Symbol	Parameter	Limits				Unit	Remarks
		Typ. mode		High-speed mode			
		Min.	Max.	Min.	Max.		
fCLK	Clock frequency	0	100	0	400	KHz	
tHIGH	HIGH period of Clock	4000	–	600	–	ns	
tLOW	LOW period of Clock	4700	–	1300	–	ns	
tR	SDA & SCL rise time	–	1000	20+(Note) 0.1Cb	300	ns	
tF	SDA & SCL fall time	–	300	20+(Note) 0.1Cb	300	ns	
tHD : STA	Hold time at START status	4000	–	600	–	ns	
tsu : STA	Set up time at START status	4700	–	600	–	ns	Only at START state repeating generation
tHD : DAT	Data input hold time	0	–	0	–	ns	
tsu : DAT	Data input setup time	250	–	100	–	ns	
tsu : STO	Set up time at STOP state	4000	–	600	–	ns	
tBUF	Bus release time	4700	–	1300	–	ns	Time must be re- leased bus before next transmission
tSP	Input filter / spike suppress (SDA & SCL pin)	N/A	N/A	0	50	ns	

Note. C_B = total capacitance of 1 bus line.

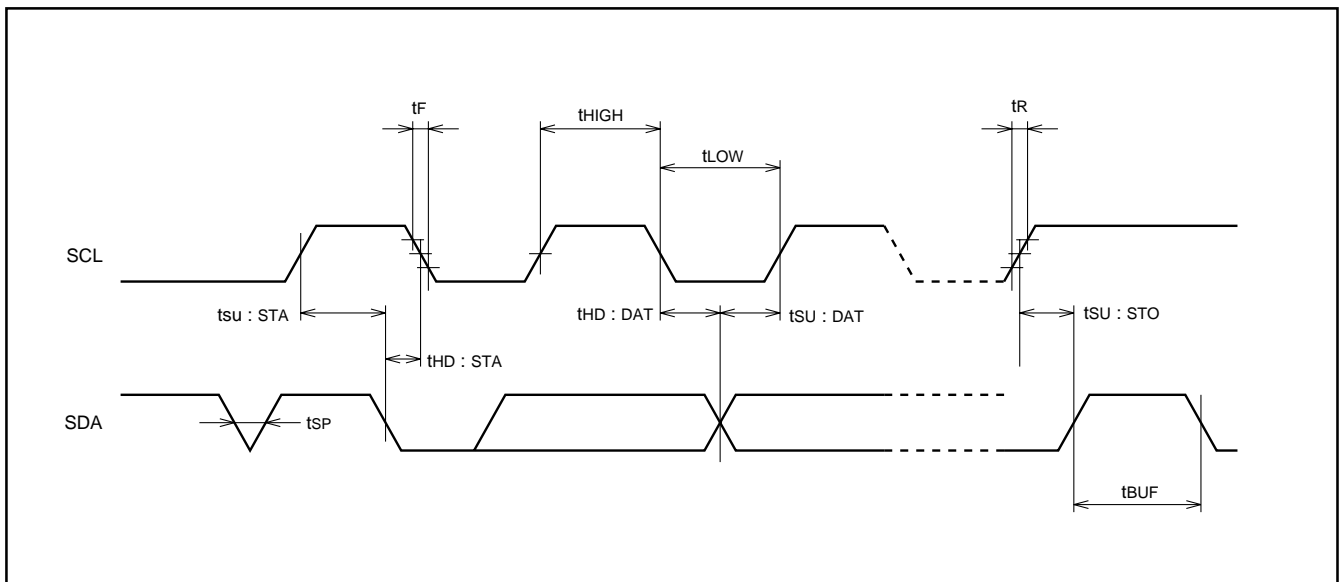


Fig. 18 Data input timing

ABSOLUTE MAXIMUM RATINGS ($V_{DD} = 5.00V$, $T_a = -20$ to $+85^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD}	Supply voltage	With respect to V_{SS} .	-0.3 to +6.0	V
V_i	Input voltage		$V_{SS} - 0.3 \leq V_i \leq V_{DD} + 0.3$	V
V_o	Output voltage		$V_{SS} \leq V_o \leq V_{DD}$	V
P_d	Power dissipation	$T_a = +25^{\circ}C$	+300	mW
T_{opr}	Operating temperature		-20 to +85	$^{\circ}C$
T_{stg}	Storage temperature		-40 to +125	$^{\circ}C$

RECOMMENDED OPERATING CONDITIONS ($V_{DD} = 5.00V$, $T_a = -20$ to $+85^{\circ}C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit	
			Min.	Typ.	Max.		
V_{DD}	Supply voltage	5V	4.75	5.0	5.25	V	
		3V	2.50	3.0	3.50	V	
V_{IH}	"H" level input voltage	\overline{AC} , \overline{CS} , HOR, VERT	$0.8V_{DD}$	V_{DD}	V_{DD}	V	
		SCK/SCL, SIN/SDA	$0.7V_{DD}$	V_{DD}	V_{DD}	V	
V_{IL}	"L" level input voltage	\overline{AC} , \overline{CS} , HOR, VERT	0	0	$0.2V_{DD}$	V	
		SCK/SCL, SIN/SDA	0	0	$0.3V_{DD}$	V	
FOSC	Oscillating frequency for display	External clock mode 1	$V_{DD} = 4.75$ to 5.25 V	6.3	—	80.0	MHz
			$V_{DD} = 2.50$ to 3.50 V	6.3	—	40.0	MHz
		External clock mode 2	$V_{DD} = 4.75$ to 5.25 V	20.0	—	110.0	MHz
			Internal clock mode	$V_{DD} = 4.75$ to 5.25 V	20.0	—	110.0
H.sync	Horizontal synchronous signal input frequency	$V_{DD} = 4.75$ to 5.25 V	15.0	—	130.0	kHz	
		$V_{DD} = 2.50$ to 3.50 V	15.0	—	60.0	kHz	

ELECTRICAL CHARACTERISTICS 1 $V_{DD}=5V$ ($V_{DD} = 5.00V$, $T_a = 25^{\circ}C$, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{DD}	Supply voltage		$T_a = -20$ to $+85^{\circ}C$	4.75	5.0	5.25	V
I_{DD}	Supply current		$V_{DD} = 5.00V$	—	40	60	mA
V_{OH}	"H" level output voltage	P0 to P7 (Note1)	$V_{DD} = 4.75V$, $I_{OH} = -0.4mA$	3.5	—	—	V
		CPOUT	$V_{DD} = 4.75V$, $I_{OH} = -0.05mA$				
V_{OL}	"L" level output voltage	P0 to P7 (Note2)	$V_{DD} = 4.75V$, $I_{OL} = 0.4mA$	—	—	0.4	V
		CPOUT	$V_{DD} = 4.75V$, $I_{OL} = 0.05mA$				
		SIN/SDA	$V_{DD} = 4.75V$, $I_{OL} = 3.0mA$				
R_i	Pull-up resistance \overline{AC} , \overline{CS}		$V_{DD} = 5.00V$	10	30	100	$k\Omega$
V_{TCK}	External clock input width		$4.75V \leq V_{DD} \leq 5.25V$	$0.6V_{DD}$	—	$0.9V_{DD}$	V

- Notes 1. The current from the IC must not exceed - 0.4 mA/port at any of the port pins (P0 to P7).
 2. The current flowing into the IC must not exceed 0.4 mA/port at any of port pins (P0 to P7).

ELECTRICAL CHARACTERISTICS 2 V_{DD}=3V (V_{DD} = 3.00V, Ta = 25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V _{DD}	Supply voltage	Ta = -20 to +85°C	2.50	3.00	3.50	V
I _{DD}	Supply current	V _{DD} = 3.00V	—	20	30	mA
V _{OH}	“H” level output voltage P0 to P7 (Note1)	V _{DD} = 2.70V, I _{OH} = -0.1mA	2.30	—	—	V
V _{OL}	“L” level output voltage P0 to P7 (Note2)	V _{DD} = 2.70V, I _{OH} = 0.1mA	—	—	0.4	V
R _I	Pull-up resistance \overline{AC} , \overline{CS}	V _{DD} = 3.00V	30	—	150	kΩ
V _{TCK}	External clock input width	2.20V ≤ V _{DD} ≤ 3.50V	0.7V _{DD}	—	V _{DD}	V

Notes 1. The current from the IC must not exceed - 0.1 mA/port at any of the port pins (P0 to P7).
 2. The current flowing into the IC must not exceed 0.1 mA/port at any of port pins (P0 to P7).

NOTE FOR SUPPLYING POWER

(1)Timing of power supplying to \overline{AC} pin

The internal circuit of M35076-XXXSP is reset when the level of the auto clear input pin \overline{AC} is "L". This pin is hysteresis input with the pull-up resistor.

The timing about power supplying of \overline{AC} pin is shown in Figure 19.

After supplying the power (V_{DD} and V_{SS}) to M35076-XXXSP and the supply voltage becomes more than $0.8 \times V_{DD}$, it needs to keep V_{IL} time; t_w of the \overline{AC} pin for more than 1ms.

Start inputting from microcomputer after \overline{AC} pin supply voltage becomes more than $0.8 \times V_{DD}$ and keeping 200ms wait time.

(2)Timing of power supplying to V_{DD1} and V_{DD2} .

Supply power to V_{DD1} and V_{DD2} at the same time.

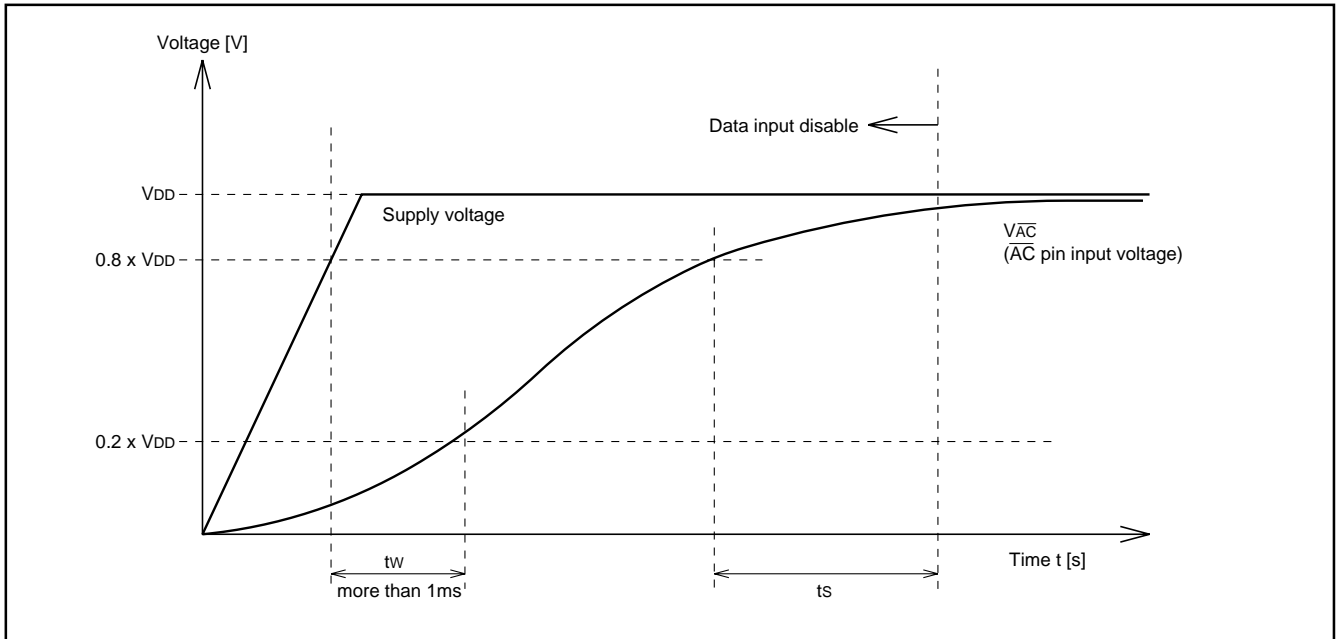


Fig. 19 Timing of power supplying to \overline{AC} pin

PRECAUTION FOR USE

Notes on noise and latch-up

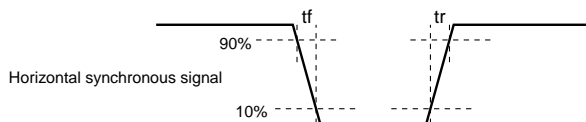
In order to avoid noise and latch-up, connect a bypass capacitor ($\approx 0.1\mu F$) directly between the V_{DD1} pin and V_{SS1} pin, and the V_{DD2} pin and V_{SS2} pin using a heavy wire.

Note for waveform timing of the horizontal signals to the HOR pin

Set horizontal synchronous signal edge* waveform timing to under 5ns and input to HOR pin.

Set only the side which set by B/F register waveform timing under 5ns and input to HOR pin.

*: Set front porch edge or back porch edge by B/F register.



DATA REQUIRED FOR MASK ROM ORDERING

Please send the following data for mask orders.

- (1) M35076-XXXSP mask ROM order confirmation form
- (2) 20P4B mark specification form
- (3) ROM data : EPROMs or floppy disks

*In the case of EPROMs, three sets of EPROMs are required per pattern.

*In the case of floppy disks, 3.5-inch 2HD disk (1BM format) is required per pattern.

STANDARD ROM TYPE : M35076-001SP

M35076-001SP is a standard ROM type of M35076-XXXSP.
The character patterns for 0 page are fixed to the contents of Figure 20 to 23, the character patterns for page 1 are fixed to the contents of Figure 24 to 27.

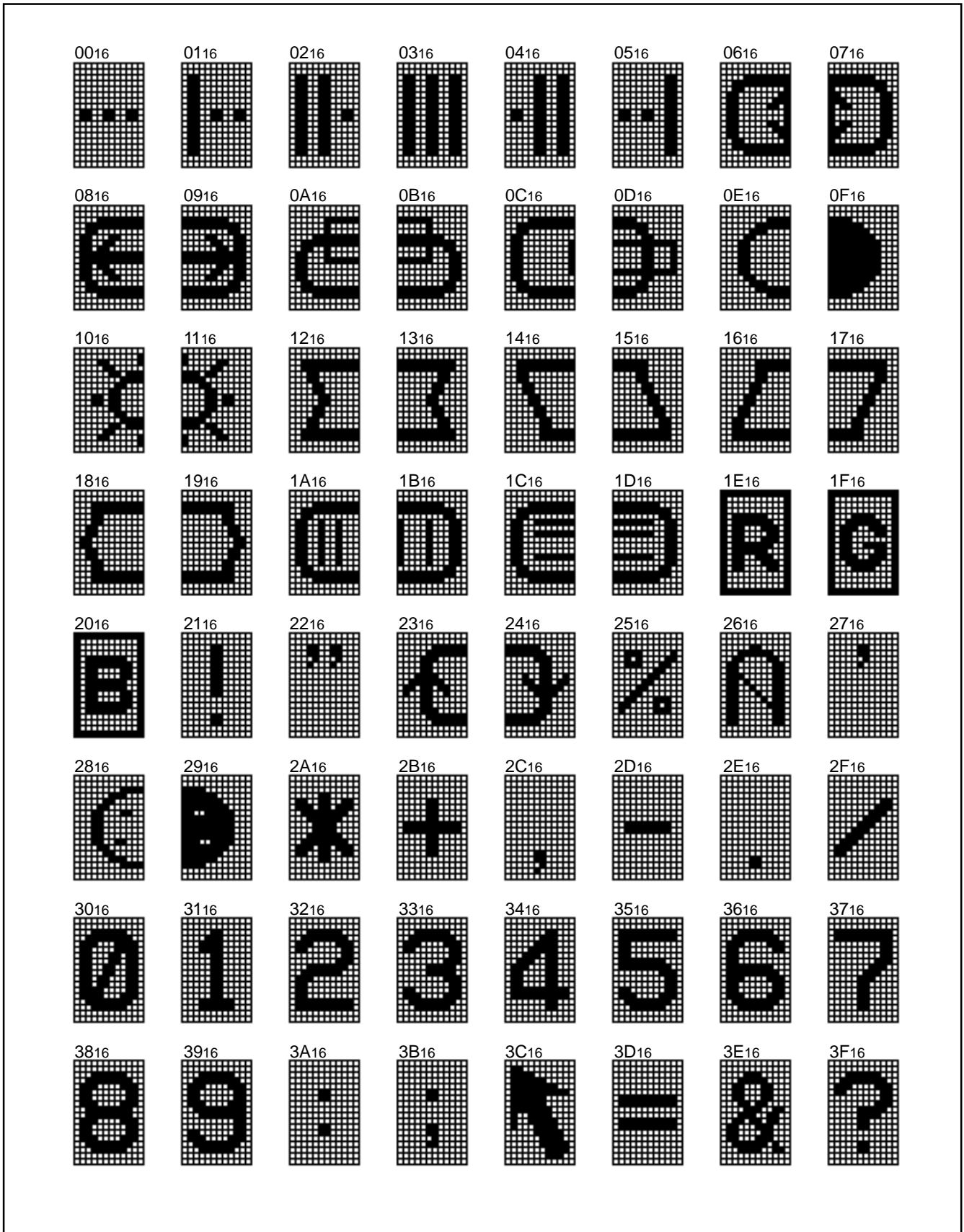


Fig. 20 M35076-001SP character pattern for page 0 (1)



Fig. 21 M35076-001SP character pattern for page 0 (2)

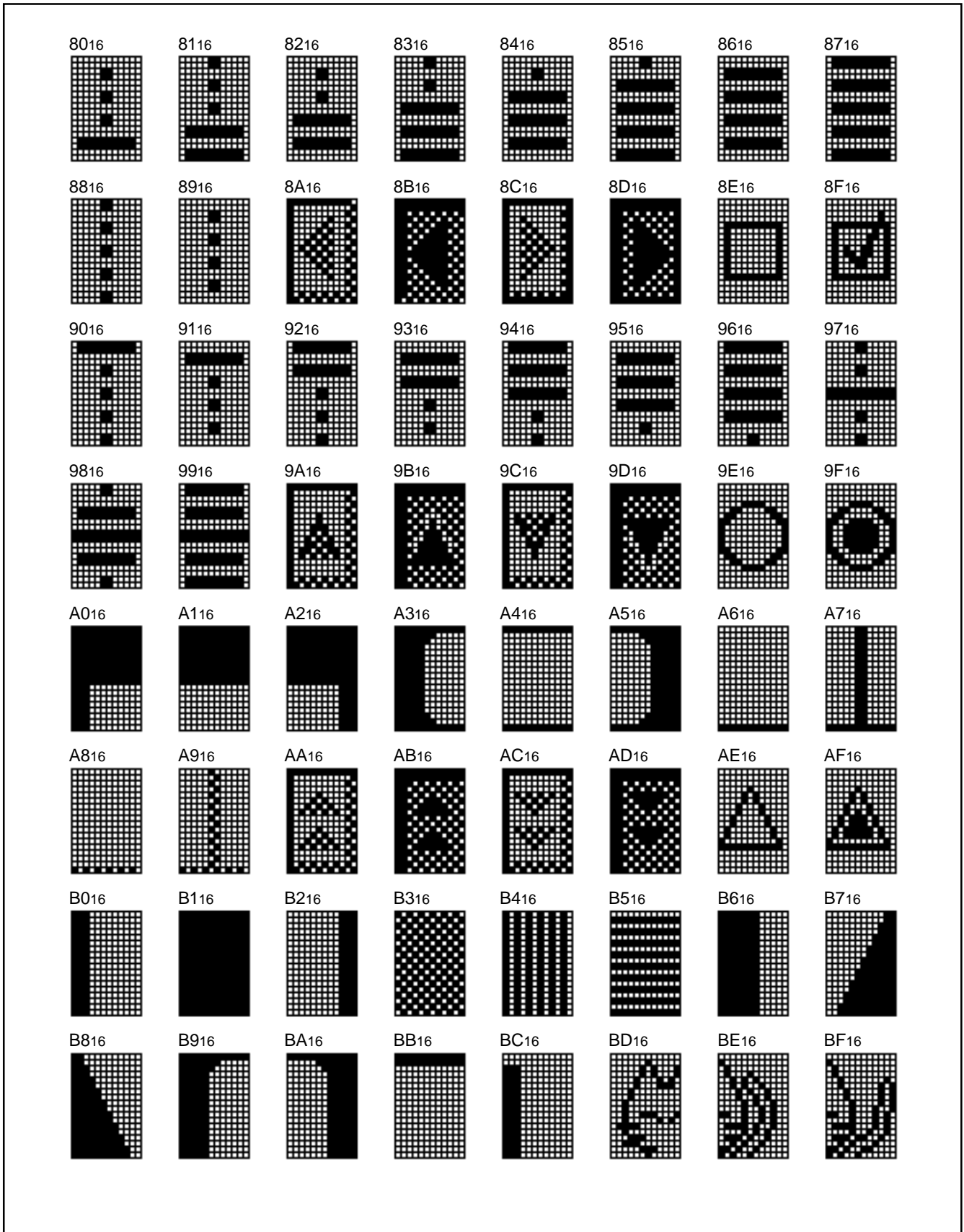


Fig. 22 M35076-001SP character pattern for page 0 (3)

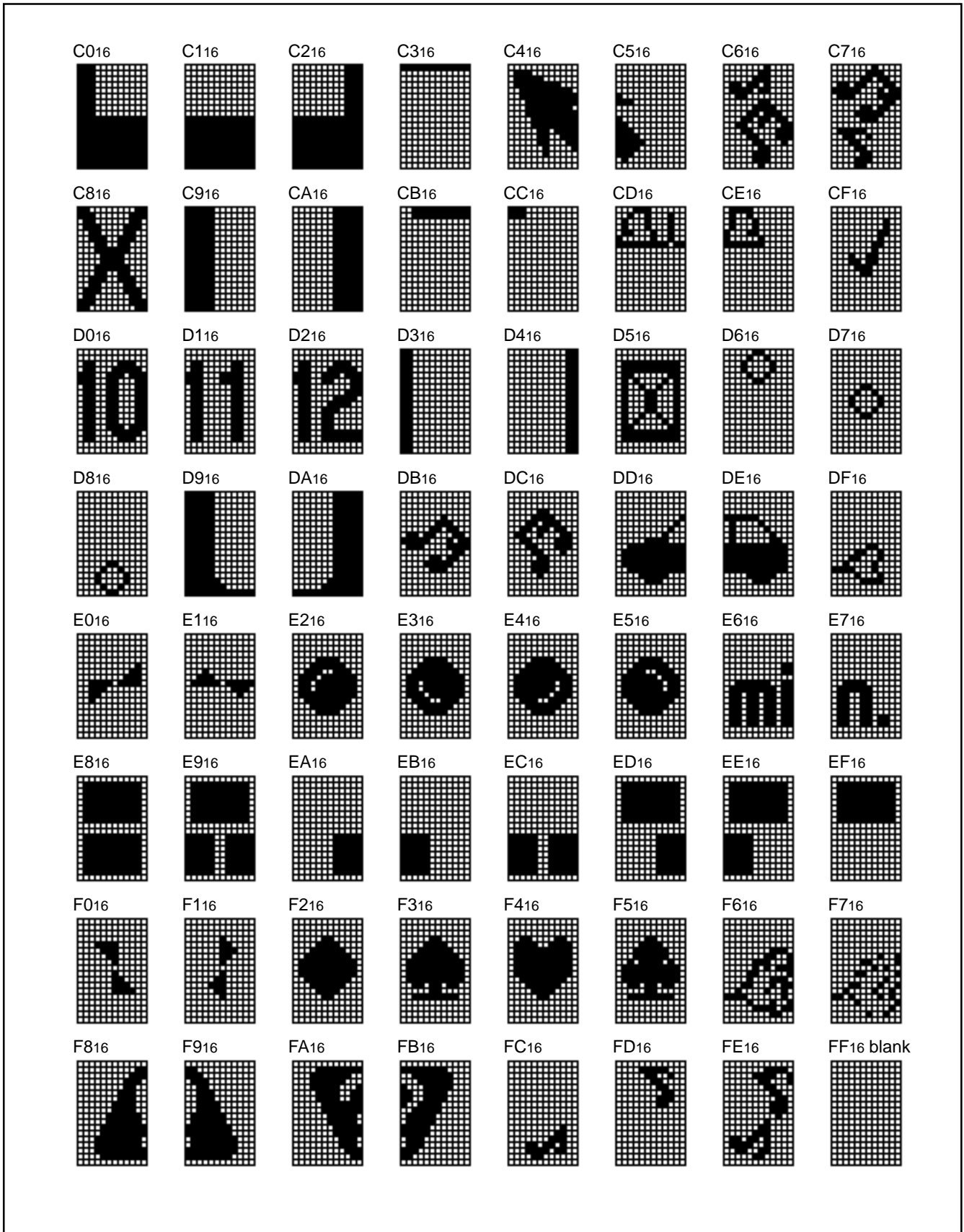


Fig. 23 M35076-001SP character pattern for page 0 (4)

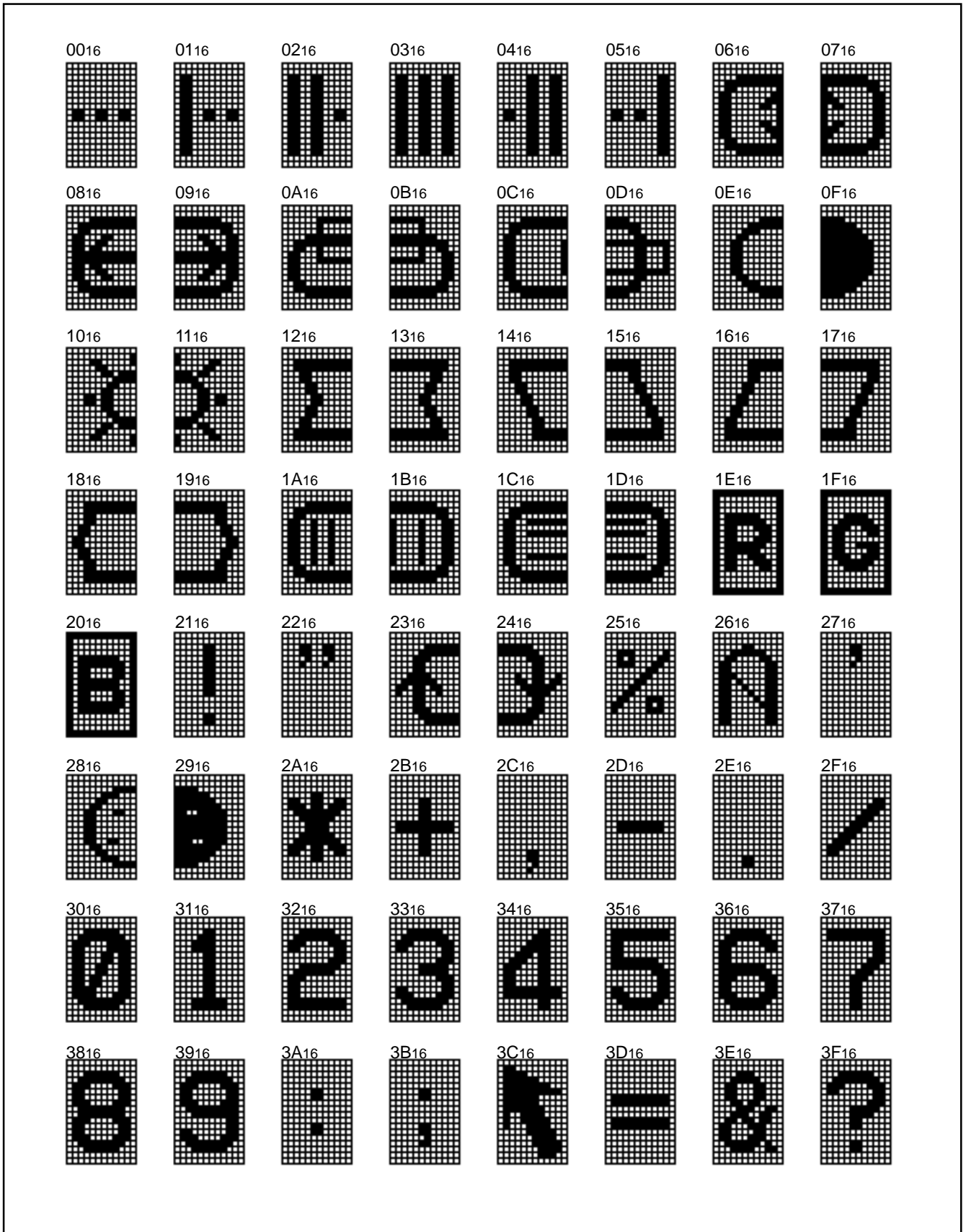


Fig. 24 M35076-001SP character pattern for page 1 (1)

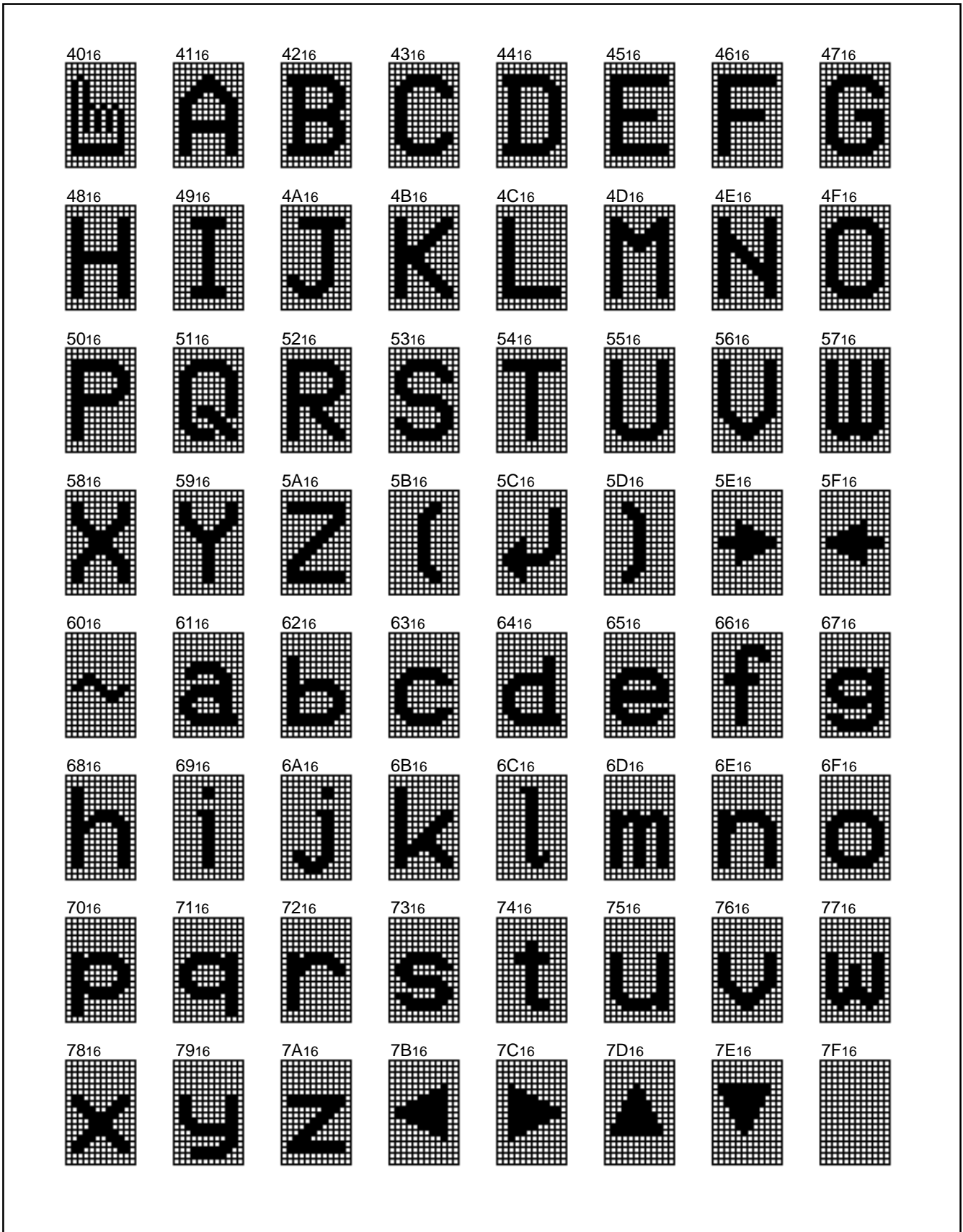


Fig. 25 M35076-001SP character pattern for page 1 (2)

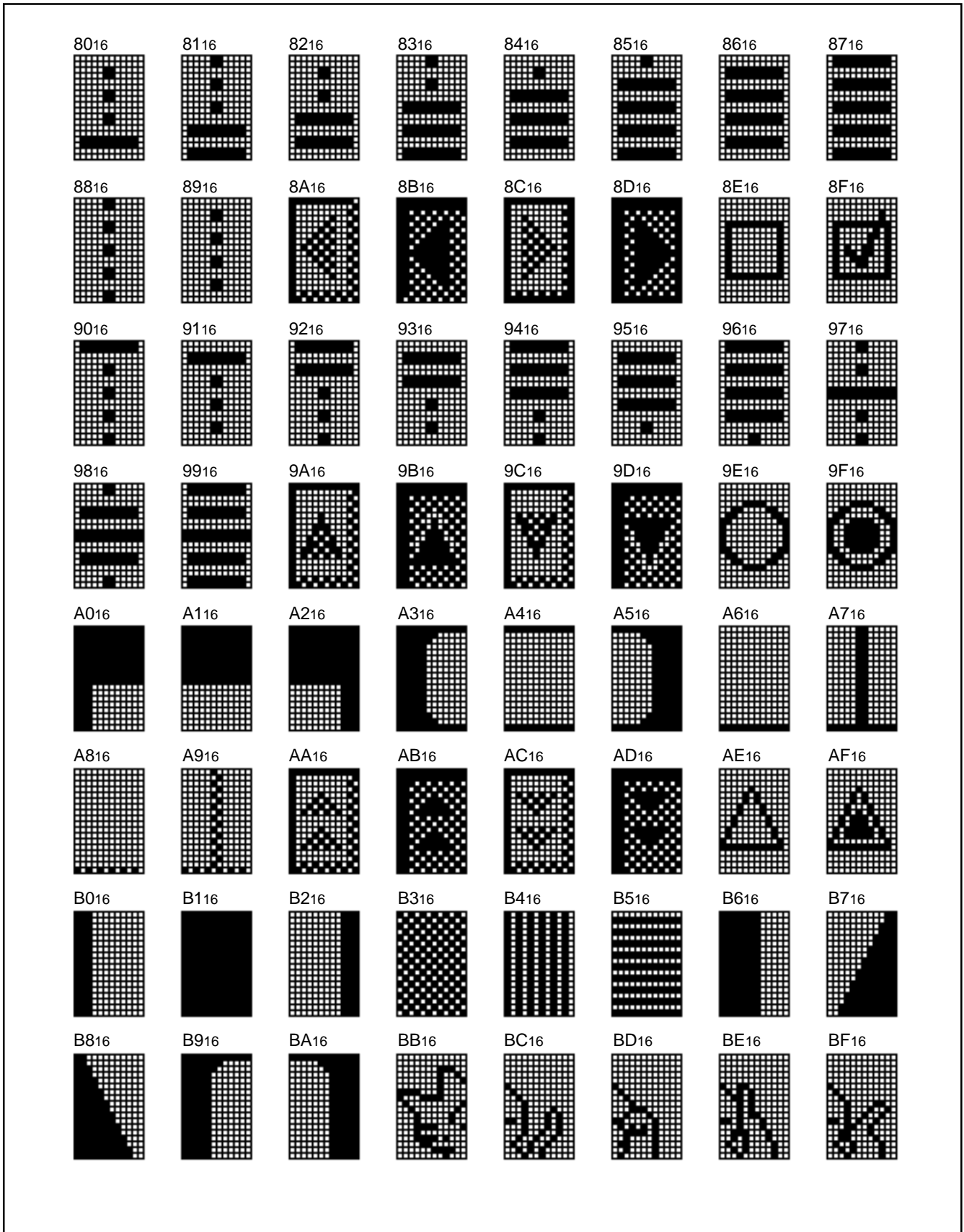


Fig. 26 M35076-001SP character pattern for page 1 (3)

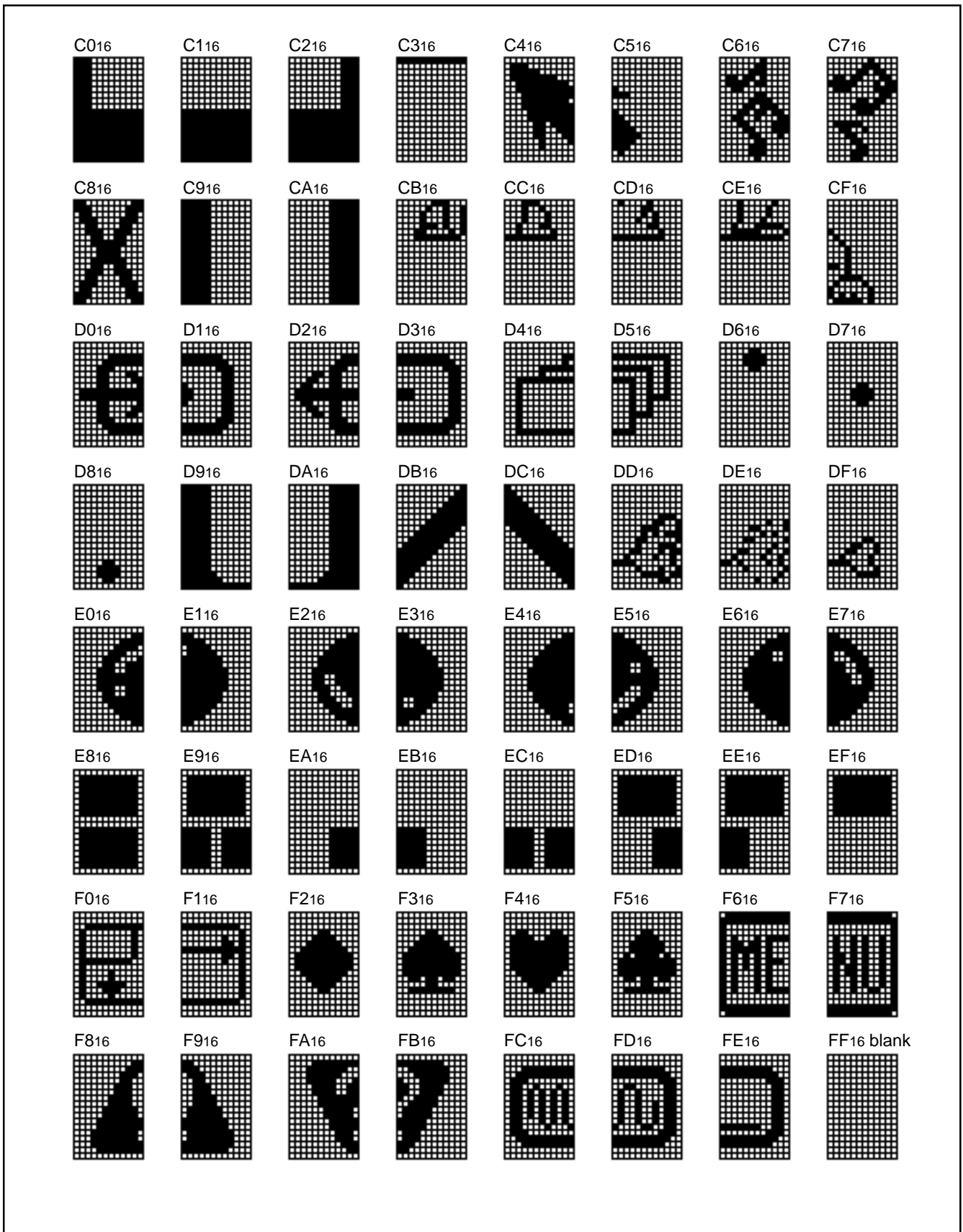
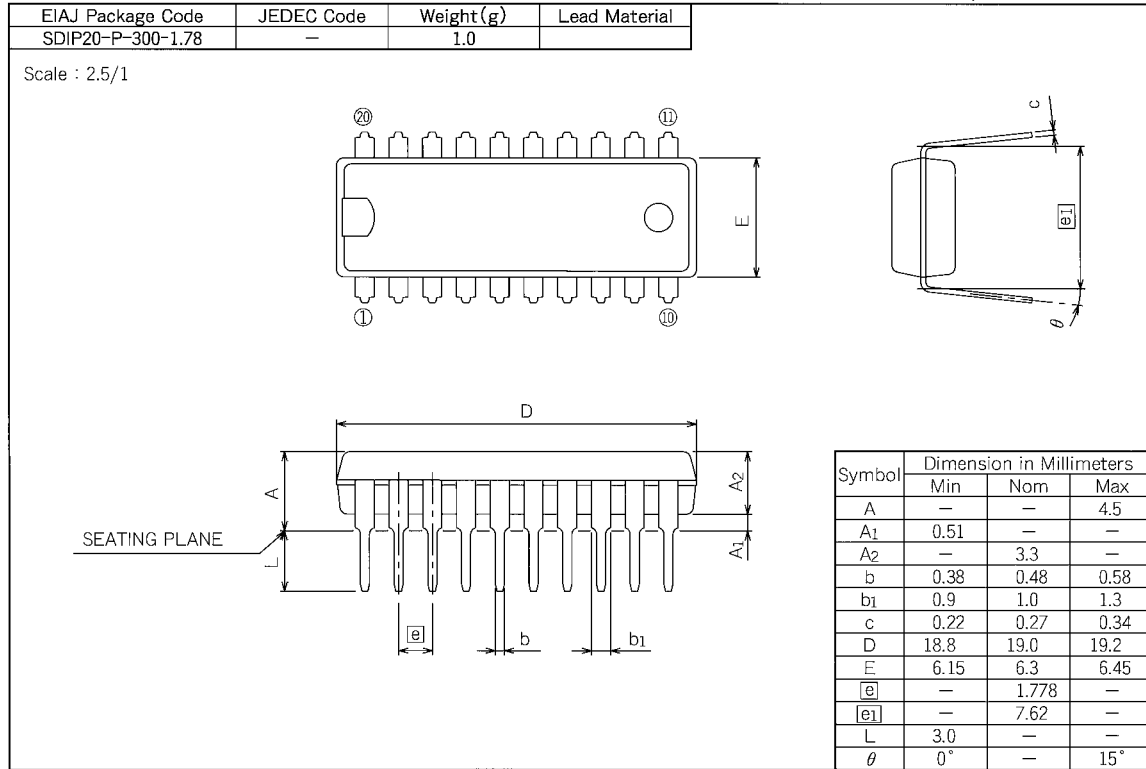


Fig. 27 M35076-001SP character pattern for page 1 (4)

PACKAGE OUTLINE

20P4B

Plastic 20pin 300mil SDIP



Renesas Technology Corp.

Nippon Bldg.,6-2,Otemachi 2-chome,Chiyoda-ku,Tokyo,100-0004 Japan

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REVISION DESCRIPTION LIST

M35076-XXXSP Data Sheet

Rev. No.	Revision Description	Rev. date
1.0	First Edition	0203