To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

M35062-XXXSP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

DESCRIPTION

M35062-XXXSP is CATV screen display control IC which can display 40 (horizontal) × 17 (vertical). It has built-in SYRAM which can be used with character ROM.

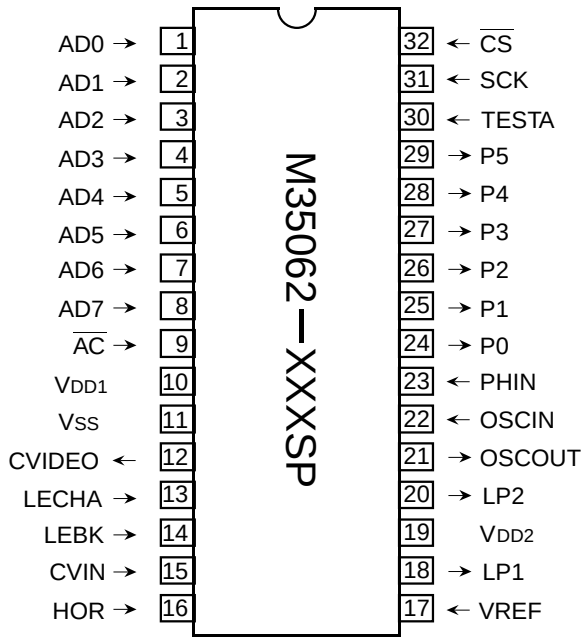
It uses a silicon gate CMOS process and M35062-XXXSP housed in a small 32-pin shrink DIP package. For M35062-001SP that is a standard ROM version of M35062-XXXSP, the character pattern is also mentioned.

FEATURES

- Screen composition ..... 40 characters × 17 lines
  (at scrolling ..... 40 characters × 16 lines)
- Number of characters displayed ..... 680 (Max.)
- Character composition ..... 12 × 13 dot matrix
- Characters available character ROM ..... 128 characters
  SYRAM ..... 7 characters
- Character sizes available horizontal ..... 2 (once, twice)
  vertical ..... 2 (once, twice)
  setting by every line
- Display locations available
  Horizontal direction ..... 486 locations
  Vertical direction ..... 235 locations
- Blinking ..... character units
  Cycle .... approximately 1 second, or approximately 0.5 seconds (per screen)
  Duty ..... 25%, 50% or 75% (per screen)
- Data input ..... 8-bit parallel × 3
- Coloring Character coloring ..... 8 colors choices per character (Note)
  Background coloring ..... 8 colors choices per character (Note)
  Raster coloring ..... 8 colors choices per screen
- Blanking Character size blanking
  Border size blanking
  Matrix-outline
  Halftone blanking
  Can be set by every line
- General-purpose output ports Combined port output ..... 6 (switching to RGB output)
- RAM erase ..... Display RAM erasing by every line
  SYRAM erasing separately
- Scrolling ..... Bit by bit smooth scroll implemented by software
- Composite synchronizating signal generation ..... Built-in (PAL, NTSC, M-PAL)
- Display oscillation circuit ..... Built-in
- Synchronous separation circuit ..... Built-in
- Synchronous correction circuit ..... Built-in

Note: Superimpose coloring is available. (NTSC, PAL, M-PAL)

PIN CONFIGURATION (TOP VIEW)



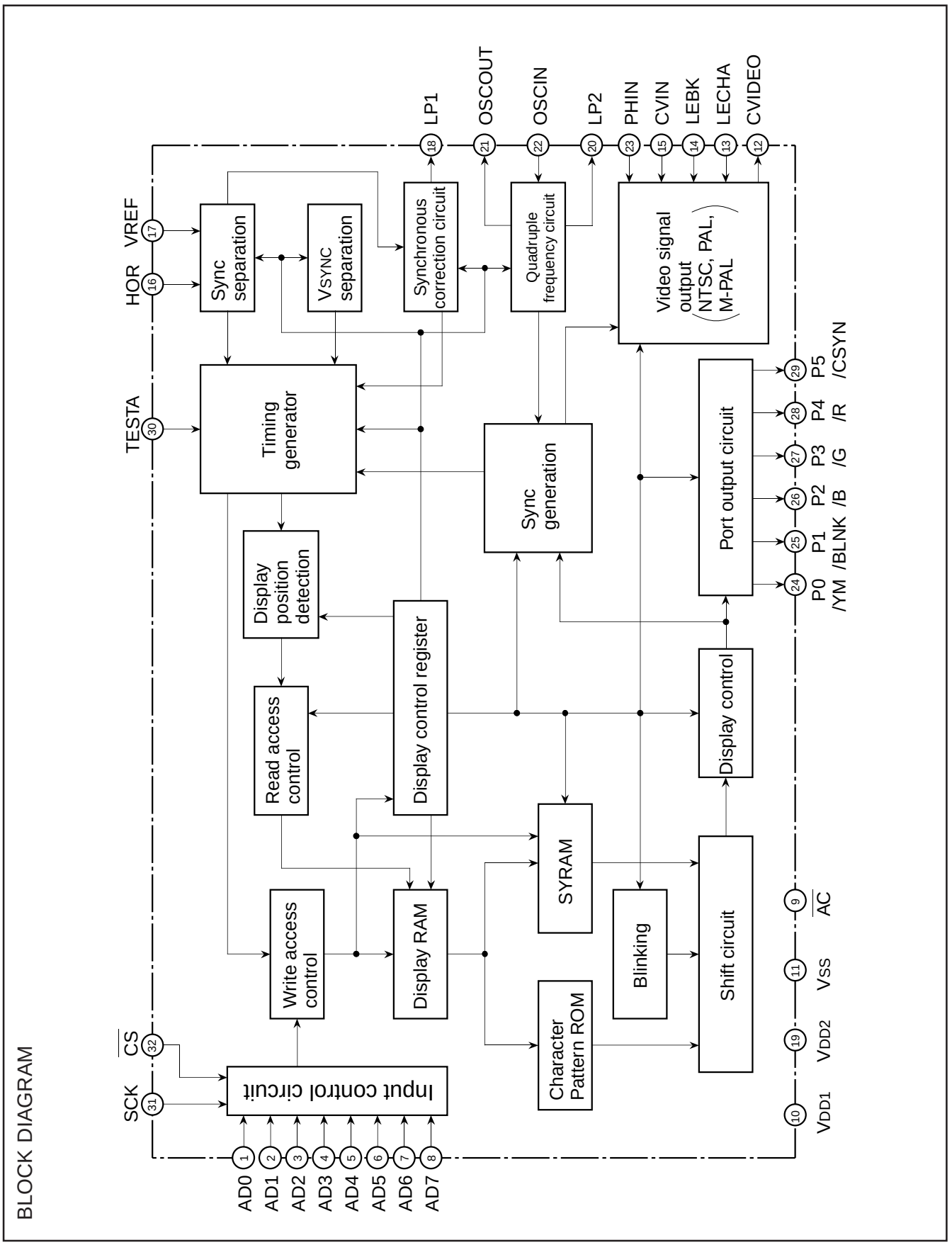
Outline 32P4B

PIN DESCRIPTION

Symbol	Pin name	Input/Output	Function
AD0 to AD7	Parallel data input	Input	These input pins determine address and data of display control register and display data memory by 8-bit parallel. Hysteresis input is required.
$\overline{AC}$	Auto-clear input	Input	When this input pin transitions from “H” to “L”, the device is reset. Built-in a pull-up resistor. Hysteresis input is required.
V_{DD1}	Power pin	—	Digital power supply pin. This pin must be connected to +5 V.
V_{SS}	Earthing pin	—	Ground pin. This pin must be connected to 0 V.
CVIDEO	Composite video signal output	Output	This pin outputs the composite video signal. The output signal is 2 V_{P-P}. In superimpose mode, this pin’s signal consists of the OSD signal combined with the input composite signal CVIN.
LECHA	Character level input	Input	This input pin is used for controlling the “white” character color level of the OSD signal.
LEBK	Black level input	Input	This input pin is used for controlling the “black” character color level of the OSD signal.
CVIN	Composite video signal input	Input	This pin inputs the external composite video signal. In superimpose mode, this pin’s signal consists of the OSD signal combined with the external composite video signal.
HOR	Synchronous signal input	Input	This pin inputs the external composite video signal. This pin inputs the clamped external video signal, sync-sep internal.
VREF	Slice level input	Input	This input pin is used to determine the slice voltage for extracting the sync signals from the video composite signal.
LP1	Filter output 1	Output	This is filter output pin 1.
V_{DD2}	Power pin	—	Analog power supply pin. This pin must be connected to +5 V.
LP2	Filter output 2	Output	This is filter output pin 2.
OSCOUT	fsc I/O pin for synchronous signal generating	Output	These are the sub-carrier oscillation (fsc) input pins for synchronous signal generating. NTSC (3.580 MHz), PAL (4.434 MHz), M-PAL (3.576 MHz) (Note).
OSCIN		Input	
PHIN	PHASE control input	Input	Control the phase changing by scanning line by PAL, M-PAL method.
P0	Port output	Output	This output pin can be configured to port P0 or YM output.
P1	Port output	Output	This output pin can be configured to port P1 or BLNK output.
P2	Port output	Output	This output pin can be configured to port P2 or B output.
P3	Port output	Output	This output pin can be configured to port P3 or G output.
P4	Port output	Output	This output pin can be configured to port P4 or R output.
P5	Port output	Output	This output pin can be configured to port P5 or CSYN output.
TESTA	Test input	Input	Factory test pin. The pin must be connected to GND.
SCK	Clock input for data input	Input	This pin is enabled when the CS pin is “L”. Data input to pins AD0 to AD7 is latched at the rising edge of this signal. This pin is hysteresis input.
$\overline{CS}$	Chip select input	Input	This is chip selection input pin. When this pin is “L”, transmission is enabled. This pin is hysteresis input.

Note: fsc signal input ……refer to “note on when fsc signal input”.

BLOCK DIAGRAM



MEMORY CONSTRUCTION

Address 000$_{16}$ to 2A7$_{16}$ are assigned to the display RAM, 2A8$_{16}$ to 2B0$_{16}$ are assigned to the display control registers and 300$_{16}$ to 36C$_{16}$ are assigned to SYRAM.

The internal circuit is reset and all display control registers (address 2A8$_{16}$ to 2B0$_{16}$) are set to "0". The memory constitution of display RAM and register is shown in Figure 1 and the memory constitution of SYRAM is shown in Figure 2.

Table 1 The memory constitution of display RAM and register

address	DA17	DA16	DA15	DA14	DA13	DA12	DA11	DA10	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
000$_{16}$	SB	SG	SR	0	0	0	SYC2	SYC1	SYC0	BB	BG	BR	BLINK	CB	CG	CR	0	C6	C5	C4	C3	C2	C1	C0
≀	SY color setting			0	0	0	SYRAM setting			Raster color setting			BLINK	Character color setting			0	Character setting						
2A7$_{16}$	SB	SG	SR	0	0	0	SYC2	SYC1	SYC0	BB	BG	BR	BLINK	CB	CG	CR	0	C6	C5	C4	C3	C2	C1	C0
2A8$_{16}$	–	TEST 3	TEST 2	TEST 1	TEST 0	TEST 11	TEST 10	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
2A9$_{16}$	–	–	–	BLINK 3	BLINK 2	BLINK 1	BLINK 0	HSZ 16	HSZ 15	HSZ 14	HSZ 13	HSZ 12	HSZ 11	HSZ 10	HSZ 9	HSZ 8	HSZ 7	HSZ 6	HSZ 5	HSZ 4	HSZ 3	HSZ 2	HSZ 1	HSZ 0
2AA$_{16}$	–	–	–	TEST 12	EQP	TEST 20	HIDE	VSZ 16	VSZ 15	VSZ 14	VSZ 13	VSZ 12	VSZ 11	VSZ 10	VSZ 9	VSZ 8	VSZ 7	VSZ 6	VSZ 5	VSZ 4	VSZ 3	VSZ 2	VSZ 1	VSZ 0
2AB$_{16}$	–	–	TEST 26	TEST 25	PHASE 2	PHASE 1	PHASE 0	DSP0 16	DSP0 15	DSP0 14	DSP0 13	DSP0 12	DSP0 11	DSP0 10	DSP0 09	DSP0 08	DSP0 07	DSP0 06	DSP0 05	DSP0 04	DSP0 03	DSP0 02	DSP0 01	DSP0 00
2AC$_{16}$	–	–	–	LBLACK	LINE B	LINE G	LINE R	DSP1 16	DSP1 15	DSP1 14	DSP1 13	DSP1 12	DSP1 11	DSP1 10	DSP1 09	DSP1 08	DSP1 07	DSP1 06	DSP1 05	DSP1 04	DSP1 03	DSP1 02	DSP1 01	DSP1 00
2AD$_{16}$	–	TEST 23	TEST 22	SERS 0	–	–	–	ERS 16	ERS 15	ERS 14	ERS 13	ERS 12	ERS 11	ERS 10	ERS 9	ERS 8	ERS 7	ERS 6	ERS 5	ERS 4	ERS 3	ERS 2	ERS 1	ERS 0
2AE$_{16}$	–	–	–	–	–	SEND 4	SEND 3	SEND 2	SEND 1	SEND 0	SST 4	SST 3	SST 2	SST 1	SST 0	SLIN 4	SLIN 3	SLIN 2	SLIN 1	SLIN 0	SBIT 3	SBIT 2	SBIT 1	SBIT 0
2AF$_{16}$	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	ALL24	SRAND 2	SRAND 1	SRAND 0	PTD 5	PTD 4	PTD 3	PTD 2	PTD 1	PTD 0	PTC 5	PTC 4	PTC 3	PTC 2	PTC 1	PTC 0
2B0$_{16}$	–	TEST 19	TEST 18	TEST 17	TEST 24	LEVEL 2	LEVEL 1	LEVEL 0	INT NON	PAL NTSC	MPAL	PALH	TEST 16	TEST 15	SEPV1	SEPV0	BLK	–	DSP ONV	DSP ON	–	SEL COR	SCOR	EX

TEST$_n$ (n = number) is MITSUBISHI test memory. Set 0 to all bits.

Table 2 The memory constitution of SYRAM

address	DA17 to DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	SYRAM code
300$_{16}$ ≀ 30C$_{16}$	0	SYEX ⋮ SYEX	S00B ⋮ S00B	S00A ⋮ S00A	S009 ⋮ S009	S008 ⋮ S008	S007 ⋮ S007	S006 ⋮ S006	S005 ⋮ S005	S004 ⋮ S004	S003 ⋮ S003	S002 ⋮ S002	S001 ⋮ S001	S000 ⋮ S000	00$_{16}$
310$_{16}$ ≀ 31C$_{16}$	0	SYEX ⋮ SYEX	S01B ⋮ S01B	S01A ⋮ S01A	S019 ⋮ S019	S018 ⋮ S018	S017 ⋮ S017	S016 ⋮ S016	S015 ⋮ S015	S014 ⋮ S014	S013 ⋮ S013	S012 ⋮ S012	S011 ⋮ S011	S010 ⋮ S010	01$_{16}$
≀	⋮	⋮	≀												≀
350$_{16}$ ≀ 35C$_{16}$	0	SYEX ⋮ SYEX	S05B ⋮ S05B	S05A ⋮ S05A	S059 ⋮ S059	S058 ⋮ S058	S057 ⋮ S057	S056 ⋮ S056	S055 ⋮ S055	S054 ⋮ S054	S053 ⋮ S053	S052 ⋮ S052	S051 ⋮ S051	S050 ⋮ S050	05$_{16}$
360$_{16}$ ≀ 36C$_{16}$	0	SYEX ⋮ SYEX	S06B ⋮ S06B	S06A ⋮ S06A	S069 ⋮ S069	S068 ⋮ S068	S067 ⋮ S067	S066 ⋮ S066	S065 ⋮ S065	S064 ⋮ S064	S063 ⋮ S063	S062 ⋮ S062	S061 ⋮ S061	S060 ⋮ S060	06$_{16}$

≀ : Name or value changes by definite ratio.
⋮ : The same name or value continues.

SCREEN CONSTITUTION

The screen lines and rows are determined from each address of the display RAM.
The screen constitution is shown in Figure 1.

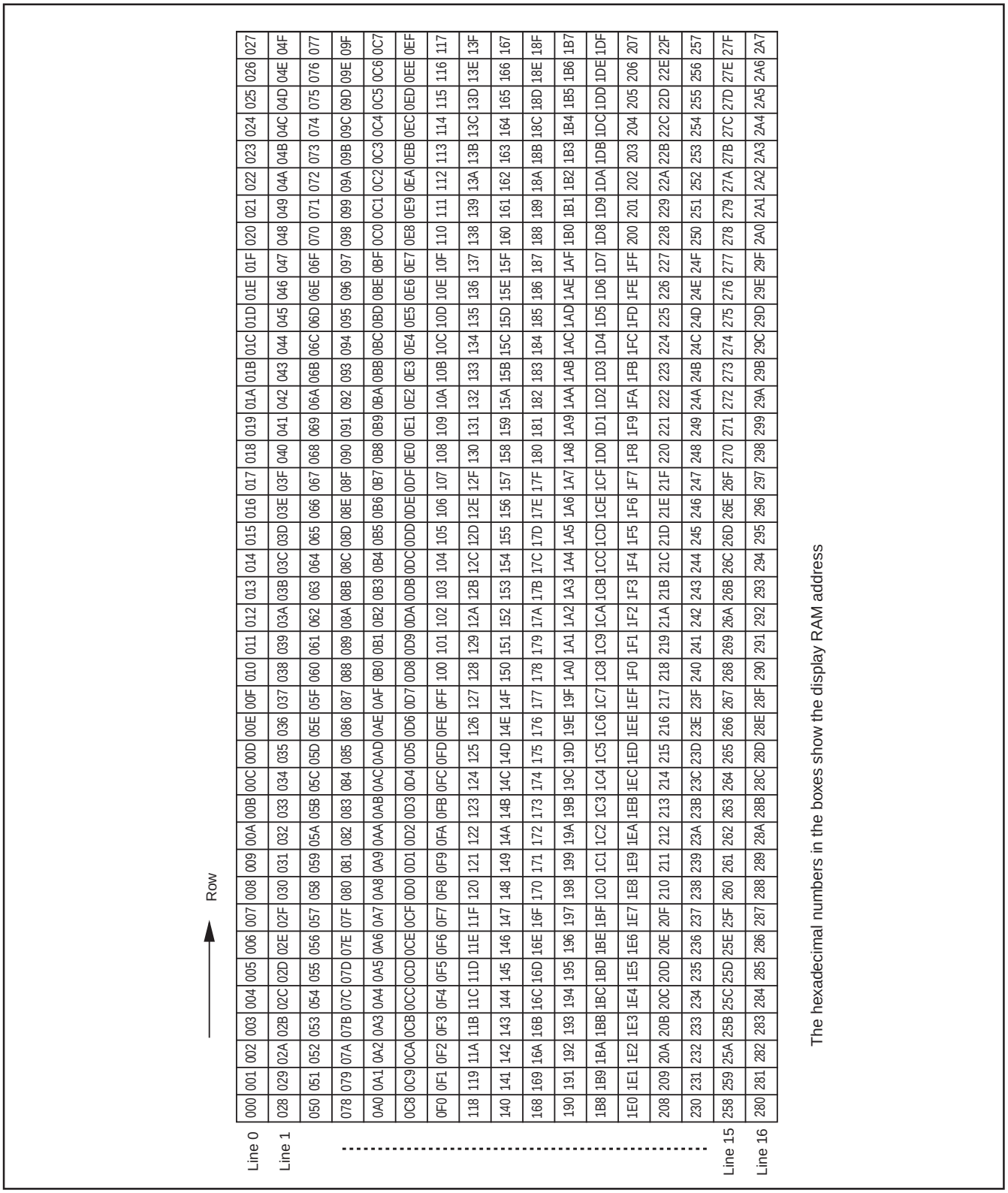
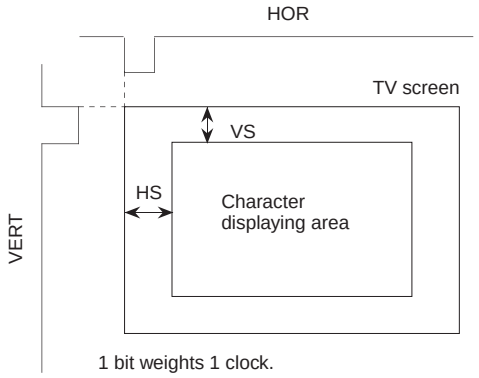


Fig. 1 Screen constitution

REGISTERS DESCRIPTION

(1) Address $2A8_{16}$

DA	Register	Contents		Remarks
		Status	Function	
0	VP0	0	If VS is the vertical display start location, $VS = H \times (\sum_{n=0}^{7} 2^n VP_n)$ H: Cycle with the horizontal synchronizing pulse	The vertical start location is specified using the 8 bits from VP7 to VP0. VP7 to VP0 < 14_{16} are not available.
		1		
1	VP1	0		
		1		
2	VP2	0		
		1		
3	VP3	0		
		1		
4	VP4	0		
		1		
5	VP5	0		
		1		
6	VP6	0		
		1		
7	VP7	0		
		1		
8	HP0	0	If HS is the horizontal display start location, $HS = T \times (\sum_{n=0}^{8} 2^n HP_n + 9)$ T: Cycle with the display clock  1 bit weights 1 clock.	The horizontal start location is specified using the 9 bits from HP8 to HP0. HP8 to HP0 < 19_{16} are not available.
		1		
9	HP1	0		
		1		
A	HP2	0		
		1		
B	HP3	0		
		1		
C	HP4	0		
		1		
D	HP5	0		
		1		
E	HP6	0		
		1		
F	HP7	0		
		1		
10	HP8	0		
		1		
11	TEST10	0	Test mode (Must be cleared to 0.)	
		1		
12	TEST11	0		
		1		
13	TEST0	0		
		1		
14	TEST1	0		
		1		
15	TEST2	0		
		1		
16	TEST3	0		
		1		
17	—	0	Must be cleared to 0.	
		1		

Note: The mark around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

(2) Address 2A9$_{16}$

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>HSZ0</td><td>0
1</td><td rowspan="17"><table><tr><td>HSZx</td><td>Horizontal direction character size</td></tr><tr><td>0</td><td>1T/dot</td></tr><tr><td>1</td><td>2T/dot</td></tr></table>T: Display clock</td><td>Set to line 0 of display RAM</td></tr>
<tr><td>1</td><td>HSZ1</td><td>0
1</td><td>Set to line 1 of display RAM</td></tr>
<tr><td>2</td><td>HSZ2</td><td>0
1</td><td>Set to line 2 of display RAM</td></tr>
<tr><td>3</td><td>HSZ3</td><td>0
1</td><td>Set to line 3 of display RAM</td></tr>
<tr><td>4</td><td>HSZ4</td><td>0
1</td><td>Set to line 4 of display RAM</td></tr>
<tr><td>5</td><td>HSZ5</td><td>0
1</td><td>Set to line 5 of display RAM</td></tr>
<tr><td>6</td><td>HSZ6</td><td>0
1</td><td>Set to line 6 of display RAM</td></tr>
<tr><td>7</td><td>HSZ7</td><td>0
1</td><td>Set to line 7 of display RAM</td></tr>
<tr><td>8</td><td>HSZ8</td><td>0
1</td><td>Set to line 8 of display RAM</td></tr>
<tr><td>9</td><td>HSZ9</td><td>0
1</td><td>Set to line 9 of display RAM</td></tr>
<tr><td>A</td><td>HSZ10</td><td>0
1</td><td>Set to line 10 of display RAM</td></tr>
<tr><td>B</td><td>HSZ11</td><td>0
1</td><td>Set to line 11 of display RAM</td></tr>
<tr><td>C</td><td>HSZ12</td><td>0
1</td><td>Set to line 12 of display RAM</td></tr>
<tr><td>D</td><td>HSZ13</td><td>0
1</td><td>Set to line 13 of display RAM</td></tr>
<tr><td>E</td><td>HSZ14</td><td>0
1</td><td>Set to line 14 of display RAM</td></tr>
<tr><td>F</td><td>HSZ15</td><td>0
1</td><td>Set to line 15 of display RAM</td></tr>
<tr><td>10</td><td>HSZ16</td><td>0
1</td><td>Set to line 16 of display RAM</td></tr>
<tr><td>11</td><td>BLINK0</td><td>0
1</td><td rowspan="2"><table><tr><td>BLINK1 \ BLINK0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>Blinking OFF</td><td>Duty 25%</td></tr><tr><td>1</td><td>Duty 50%</td><td>Duty 75%</td></tr></table></td><td rowspan="2">Blinking duty ratio can be altered.</td></tr>
<tr><td>12</td><td>BLINK1</td><td>0
1</td></tr>
<tr><td>13</td><td>BLINK2</td><td>0</td><td>Cycle approximately 1 second.</td><td rowspan="2">Blinking cycle can be altered.</td></tr>
<tr><td></td><td></td><td>1</td><td>Cycle approximately 0.5 second.</td></tr>
<tr><td rowspan="2">14</td><td rowspan="2">BLINK3</td><td>0</td><td>Normal blinking</td><td>Character is in flashing state.</td></tr>
<tr><td>1</td><td>Normal character, reversed character alternation display.</td><td>Character is always displayed
(normal character, reversed character).</td></tr>
<tr><td>15</td><td>—</td><td>0
1</td><td rowspan="3">Must be cleared to 0.</td><td rowspan="3"></td></tr>
<tr><td>16</td><td>—</td><td>0
1</td></tr>
<tr><td>17</td><td>—</td><td>0
1</td></tr>
</table>

(3) Address 2AA16

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>VSZ0</td><td>0
1</td><td rowspan="22"><table><tr><th>VSZx</th><th>Vertical direction character size</th></tr><tr><td>0</td><td>1H/dot</td></tr><tr><td>1</td><td>2H/dot</td></tr></table>H: Horizontal synchronous pulse</td><td>Set to line 0 of display RAM</td></tr>
<tr><td>1</td><td>VSZ1</td><td>0
1</td><td>Set to line 1 of display RAM</td></tr>
<tr><td>2</td><td>VSZ2</td><td>0
1</td><td>Set to line 2 of display RAM</td></tr>
<tr><td>3</td><td>VSZ3</td><td>0
1</td><td>Set to line 3 of display RAM</td></tr>
<tr><td>4</td><td>VSZ4</td><td>0
1</td><td>Set to line 4 of display RAM</td></tr>
<tr><td>5</td><td>VSZ5</td><td>0
1</td><td>Set to line 5 of display RAM</td></tr>
<tr><td>6</td><td>VSZ6</td><td>0
1</td><td>Set to line 6 of display RAM</td></tr>
<tr><td>7</td><td>VSZ7</td><td>0
1</td><td>Set to line 7 of display RAM</td></tr>
<tr><td>8</td><td>VSZ8</td><td>0
1</td><td>Set to line 8 of display RAM</td></tr>
<tr><td>9</td><td>VSZ9</td><td>0
1</td><td>Set to line 9 of display RAM</td></tr>
<tr><td>A</td><td>VSZ10</td><td>0
1</td><td>Set to line 10 of display RAM</td></tr>
<tr><td>B</td><td>VSZ11</td><td>0
1</td><td>Set to line 11 of display RAM</td></tr>
<tr><td>C</td><td>VSZ12</td><td>0
1</td><td>Set to line 12 of display RAM</td></tr>
<tr><td>D</td><td>VSZ13</td><td>0
1</td><td>Set to line 13 of display RAM</td></tr>
<tr><td>E</td><td>VSZ14</td><td>0
1</td><td>Set to line 14 of display RAM</td></tr>
<tr><td>F</td><td>VSZ15</td><td>0
1</td><td>Set to line 15 of display RAM</td></tr>
<tr><td>10</td><td>VSZ16</td><td>0
1</td><td>Set to line 16 of display RAM</td></tr>
<tr><td>11</td><td>HIDE</td><td>0
1</td><td>SYRAM writting over
SYRAM writting over or character erasing</td><td>Decided by register LINER, G and B or DAC bit (SYEX) of SYRAM.</td></tr>
<tr><td>12</td><td>TEST20</td><td>0
1</td><td>Test mode (Must be cleared to 0.)</td><td></td></tr>
<tr><td>13</td><td>EQP</td><td>0
1</td><td>It does not include equivalent pulse.
It includes equivalent pulse.</td><td></td></tr>
<tr><td>14</td><td>TEST12</td><td>0
1</td><td>Test mode (Must be cleared to 0.)</td><td></td></tr>
<tr><td>15</td><td>—</td><td>0
1</td><td rowspan="3">Must be cleared to 0.</td><td rowspan="3"></td></tr>
<tr><td>16</td><td>—</td><td>0
1</td></tr>
<tr><td>17</td><td>—</td><td>0
1</td></tr>
</table>

(4) Address 2AB16

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>DSP0 00</td><td>0
1</td><td rowspan="16">DSP0XX / DSP1XX
0: Character; Border
1: Matrix-outline; Halftone (Note)

Set by combination of DSP0XX (address 2AB16) and DSP1XX (address 2AC16).
At internal synchronous mode (EX = 1), display monitor signal area is all blanking signal (BLNK output) area.

Note: For half-tone display, it is necessary to input the external composite video signal to the CVIN pin, and externally connect a 100 to 200 Ω resistor in series. However, the half-tone display is possible only with superimposed displays.</td><td>Set to line 0 of display RAM</td></tr>
<tr><td>1</td><td>DSP0 01</td><td>0
1</td><td>Set to line 1 of display RAM</td></tr>
<tr><td>2</td><td>DSP0 02</td><td>0
1</td><td>Set to line 2 of display RAM</td></tr>
<tr><td>3</td><td>DSP0 03</td><td>0
1</td><td>Set to line 3 of display RAM</td></tr>
<tr><td>4</td><td>DSP0 04</td><td>0
1</td><td>Set to line 4 of display RAM</td></tr>
<tr><td>5</td><td>DSP0 05</td><td>0
1</td><td>Set to line 5 of display RAM</td></tr>
<tr><td>6</td><td>DSP0 06</td><td>0
1</td><td>Set to line 6 of display RAM</td></tr>
<tr><td>7</td><td>DSP0 07</td><td>0
1</td><td>Set to line 7 of display RAM</td></tr>
<tr><td>8</td><td>DSP0 08</td><td>0
1</td><td>Set to line 8 of display RAM</td></tr>
<tr><td>9</td><td>DSP0 09</td><td>0
1</td><td>Set to line 9 of display RAM</td></tr>
<tr><td>A</td><td>DSP0 10</td><td>0
1</td><td>Set to line 10 of display RAM</td></tr>
<tr><td>B</td><td>DSP0 11</td><td>0
1</td><td>Set to line 11 of display RAM</td></tr>
<tr><td>C</td><td>DSP0 12</td><td>0
1</td><td>Set to line 12 of display RAM</td></tr>
<tr><td>D</td><td>DSP0 13</td><td>0
1</td><td>Set to line 13 of display RAM</td></tr>
<tr><td>E</td><td>DSP0 14</td><td>0
1</td><td>Set to line 14 of display RAM</td></tr>
<tr><td>F</td><td>DSP0 15</td><td>0
1</td><td>Set to line 15 of display RAM</td></tr>
<tr><td>10</td><td>DSP0 16</td><td>0
1</td><td>Set to line 16 of display RAM</td></tr>
<tr><td>11</td><td>PHASE 0</td><td>0
1</td><td rowspan="2">PHASE 2 / PHASE 1 / PHASE 0 / Color
0 0 0 Black
0 0 1 Red
0 1 0 Green
0 1 1 Yellow
1 0 0 Blue
1 0 1 Gray
1 1 0 Cyan
1 1 1 White</td><td rowspan="2">Raster color setting.
At PHASE 2 through 0 =101, video signal output is gray, and RGB output is magenta.

Refer Fig 3 about phase angle.</td></tr>
<tr><td>12</td><td>PHASE 1</td><td>0
1</td></tr>
<tr><td>13</td><td>PHASE 2</td><td>0
1</td><td></td></tr>
<tr><td>14</td><td>TEST25</td><td>0
1</td><td colspan="2">Test mode (Must be cleared to 0.)</td></tr>
<tr><td>15</td><td>TEST26</td><td>0
1</td><td colspan="2"></td></tr>
<tr><td>16</td><td>—</td><td>0
1</td><td colspan="2">Must be cleared to 0.</td></tr>
<tr><td>17</td><td>—</td><td>0
1</td><td colspan="2"></td></tr>
</table>

(5) Address $2AC_{16}$

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>DSP1 00</td><td>0
1</td><td rowspan="16">
<table>
<tr><th>DSP0XX / DSP1XX</th><th>0</th><th>1</th></tr>
<tr><td>0</td><td>Character</td><td>Border</td></tr>
<tr><td>1</td><td>Matrix-outline</td><td>Halftone (Note)</td></tr>
</table>
Set by combination of DSP_{0XX} (address $2AB_{16}$) and DSP_{1XX} (address $2AC_{16}$).
At internal synchronous mode (EX = 1), display monitor signal area is all blanking signal (BLNK output) area.

Note: For half-tone display, it is necessary to input the external composite video signal to the CVIN pin, and externally connect a 100 to 200 Ω resistor in series. However, the half-tone display is possible only with superimposed displays.
</td><td>Set to line 0 of display RAM</td></tr>
<tr><td>1</td><td>DSP1 01</td><td>0
1</td><td>Set to line 1 of display RAM</td></tr>
<tr><td>2</td><td>DSP1 02</td><td>0
1</td><td>Set to line 2 of display RAM</td></tr>
<tr><td>3</td><td>DSP1 03</td><td>0
1</td><td>Set to line 3 of display RAM</td></tr>
<tr><td>4</td><td>DSP1 04</td><td>0
1</td><td>Set to line 4 of display RAM</td></tr>
<tr><td>5</td><td>DSP1 05</td><td>0
1</td><td>Set to line 5 of display RAM</td></tr>
<tr><td>6</td><td>DSP1 06</td><td>0
1</td><td>Set to line 6 of display RAM</td></tr>
<tr><td>7</td><td>DSP1 07</td><td>0
1</td><td>Set to line 7 of display RAM</td></tr>
<tr><td>8</td><td>DSP1 08</td><td>0
1</td><td>Set to line 8 of display RAM</td></tr>
<tr><td>9</td><td>DSP1 09</td><td>0
1</td><td>Set to line 9 of display RAM</td></tr>
<tr><td>A</td><td>DSP1 10</td><td>0
1</td><td>Set to line 10 of display RAM</td></tr>
<tr><td>B</td><td>DSP1 11</td><td>0
1</td><td>Set to line 11 of display RAM</td></tr>
<tr><td>C</td><td>DSP1 12</td><td>0
1</td><td>Set to line 12 of display RAM</td></tr>
<tr><td>D</td><td>DSP1 13</td><td>0
1</td><td>Set to line 13 of display RAM</td></tr>
<tr><td>E</td><td>DSP1 14</td><td>0
1</td><td>Set to line 14 of display RAM</td></tr>
<tr><td>F</td><td>DSP1 15</td><td>0
1</td><td>Set to line 15 of display RAM</td></tr>
<tr><td>10</td><td>DSP1 16</td><td>0
1</td><td>Set to line 16 of display RAM</td></tr>
<tr><td>11</td><td>LINER</td><td>0
1</td><td rowspan="3">
<table>
<tr><th>LINE B</th><th>LINE G</th><th>LINE R</th><th>Color SELCOR=0</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Red</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Green</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Yellow</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Blue</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Gray</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Cyan</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>White</td></tr>
</table>
</td><td rowspan="3">SYRAM color setting.
Color is decided by DAC bit (SYEX) of SYRAM or HIDE register.
At LINE BGR = 101, video signal output is gray, and RGB output is magenta.

Refer Fig. 3 about phase angle.</td></tr>
<tr><td>12</td><td>LINEG</td><td>0
1</td></tr>
<tr><td>13</td><td>LINEB</td><td>0
1</td></tr>
<tr><td>14</td><td>LBLACK</td><td>0</td><td>Set black level to 2.3V</td><td rowspan="2">Set black level of video signal.</td></tr>
<tr><td></td><td></td><td>1</td><td>Set black level to 2.1V</td></tr>
<tr><td>15</td><td>—</td><td>0
1</td><td rowspan="3">Must be cleared to 0.</td><td rowspan="3"></td></tr>
<tr><td>16</td><td>—</td><td>0
1</td></tr>
<tr><td>17</td><td>—</td><td>0
1</td></tr>
</table>

(6) Address 2AD16

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>ERS0</td><td>0
1</td><td rowspan="26">Erase display RAM
<table><tr><th>ERSx</th><th>RAM erase</th></tr><tr><td>0</td><td>do not erase</td></tr><tr><td>1</td><td>do erase</td></tr></table>Do not set “1” more than 2 bits at the same time.
The setting is not retained even if the bit is set to “1”.
Therefore, it is not necessary to cancel it.</td><td>Set to line 0 of display RAM</td></tr>
<tr><td>1</td><td>ERS1</td><td>0
1</td><td>Set to line 1 of display RAM</td></tr>
<tr><td>2</td><td>ERS2</td><td>0
1</td><td>Set to line 2 of display RAM</td></tr>
<tr><td>3</td><td>ERS3</td><td>0
1</td><td>Set to line 3 of display RAM</td></tr>
<tr><td>4</td><td>ERS4</td><td>0
1</td><td>Set to line 4 of display RAM</td></tr>
<tr><td>5</td><td>ERS5</td><td>0
1</td><td>Set to line 5 of display RAM</td></tr>
<tr><td>6</td><td>ERS6</td><td>0
1</td><td>Set to line 6 of display RAM</td></tr>
<tr><td>7</td><td>ERS7</td><td>0
1</td><td>Set to line 7 of display RAM</td></tr>
<tr><td>8</td><td>ERS8</td><td>0
1</td><td>Set to line 8 of display RAM</td></tr>
<tr><td>9</td><td>ERS9</td><td>0
1</td><td>Set to line 9 of display RAM</td></tr>
<tr><td>A</td><td>ERS10</td><td>0
1</td><td>Set to line 10 of display RAM</td></tr>
<tr><td>B</td><td>ERS11</td><td>0
1</td><td>Set to line 11 of display RAM</td></tr>
<tr><td>C</td><td>ERS12</td><td>0
1</td><td>Set to line 12 of display RAM</td></tr>
<tr><td>D</td><td>ERS13</td><td>0
1</td><td>Set to line 13 of display RAM</td></tr>
<tr><td>E</td><td>ERS14</td><td>0
1</td><td>Set to line 14 of display RAM</td></tr>
<tr><td>F</td><td>ERS15</td><td>0
1</td><td>Set to line 15 of display RAM</td></tr>
<tr><td>10</td><td>ERS16</td><td>0
1</td><td>Set to line 16 of display RAM</td></tr>
<tr><td>11</td><td>–</td><td>0
1</td><td rowspan="6">Must be cleared to 0.</td><td></td></tr>
<tr><td>12</td><td>–</td><td>0
1</td><td></td></tr>
<tr><td>13</td><td>–</td><td>0
1</td><td></td></tr>
<tr><td>14</td><td>SERS0</td><td>0
1</td><td>do not erase SYRAM
erase SYRAM</td><td>Set to SYRAM code 0016 to 0616 (Note)</td></tr>
<tr><td>15</td><td>TEST22</td><td>0
1</td><td rowspan="2">Test mode (Must be cleared to 0.)</td><td rowspan="2"></td></tr>
<tr><td>16</td><td>TEST23</td><td>0
1</td></tr>
<tr><td>17</td><td>—</td><td>0
1</td><td>Must be cleared to 0.</td><td></td></tr>
</table>

Note: The setting is not retained even if the bit is set to “1”. Therefore, it is not necessary to cancel it.

(7) Address 2AE16

DA	Register	Contents		Remarks
		Status	Function	
0	SBIT0	0	Set display start bit of scroll block: $SA = \sum_{n=0}^{3} 2^n (SBIT_n)$	Setting valid SA = 0 to 12 invalid SA = 13 to15
		1		
1	SBIT1	0		
		1		
2	SBIT2	0		
		1		
3	SBIT3	0		
		1		
4	SLIN0	0	Set display start line of scroll block: $SB = \sum_{n=0}^{4} 2^n (SLIN_n)$	Setting valid SB = 0 to 16 invalid SB = 17 to 31
		1		
5	SLIN1	0		
		1		
6	SLIN2	0		
		1		
7	SLIN3	0		
		1		
8	SLIN4	0		
		1		
9	SST0	0	Set start line of scroll block (last line number of the fixed block 1): $SC = \sum_{n=0}^{4} 2^n (SST_n)$	Setting valid SC = 0 to 15 invalid SC = 16 to 31
		1		
A	SST1	0		
		1		
B	SST2	0		
		1		
C	SST3	0		
		1		
D	SST4	0		
		1		
E	SEND0	0	Set start line of fixed block 2 (last line number of the scroll block): $SD = \sum_{n=0}^{4} 2^n (SEND_n)$	When the scrolling on setting valid SD = 2 to 17 invalid SD = 18 to 31 When the scrolling off set SD = 0 SD > SC + 2
		1		
F	SEND1	0		
		1		
10	SEND2	0		
		1		
11	SEND3	0		
		1		
12	SEND4	0		
		1		
13	—	0	Must be cleared to 0.	
		1		
14	—	0		
		1		
15	—	0		
		1		
16	—	0		
		1		
17	—	0		
		1		

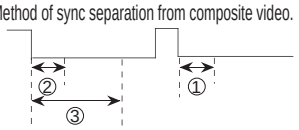
Note: When the scrolling on, set the ratio which will be SC < SB < SD.

(8) Address 2AF16

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>PTC0</td><td>0</td><td>Port P0 output</td><td rowspan="2">Select P0 pin</td></tr>
<tr><td></td><td></td><td>1</td><td>YM output</td></tr>
<tr><td>1</td><td>PTC1</td><td>0</td><td>Port P1 output</td><td rowspan="2">Select P1 pin</td></tr>
<tr><td></td><td></td><td>1</td><td>BLNK output</td></tr>
<tr><td>2</td><td>PTC2</td><td>0</td><td>Port P2 output</td><td rowspan="2">Select P2 pin</td></tr>
<tr><td></td><td></td><td>1</td><td>B output</td></tr>
<tr><td>3</td><td>PTC3</td><td>0</td><td>Port P3 output</td><td rowspan="2">Select P3 pin</td></tr>
<tr><td></td><td></td><td>1</td><td>G output</td></tr>
<tr><td>4</td><td>PTC4</td><td>0</td><td>Port P4 output</td><td rowspan="2">Select P4 pin</td></tr>
<tr><td></td><td></td><td>1</td><td>R output</td></tr>
<tr><td>5</td><td>PTC5</td><td>0</td><td>Port P5 output</td><td rowspan="2">Select P5 pin</td></tr>
<tr><td></td><td></td><td>1</td><td>CSYN output</td></tr>
<tr><td>6</td><td>PTD0</td><td>0</td><td>When port output: 0 output, when YM output: negative polarity.</td><td rowspan="2">Select data of P0 pin</td></tr>
<tr><td></td><td></td><td>1</td><td>When port output: 1 output, when YM output: polarity.</td></tr>
<tr><td>7</td><td>PTD1</td><td>0</td><td>When port output: 0 output, when BLNK output: negative polarity.</td><td rowspan="2">Select data of P1 pin</td></tr>
<tr><td></td><td></td><td>1</td><td>When port output: 1 output, when BLNK output: polarity.</td></tr>
<tr><td>8</td><td>PTD2</td><td>0</td><td>When port output: 0 output, when B output: negative polarity.</td><td rowspan="2">Select data of P2 pin</td></tr>
<tr><td></td><td></td><td>1</td><td>When port output: 1 output, when B output: polarity.</td></tr>
<tr><td>9</td><td>PTD3</td><td>0</td><td>When port output: 0 output, when G output: negative polarity.</td><td rowspan="2">Select data of P3 pin</td></tr>
<tr><td></td><td></td><td>1</td><td>When port output: 1 output, when G output: polarity.</td></tr>
<tr><td>A</td><td>PTD4</td><td>0</td><td>When port output: 0 output, when R output: negative polarity.</td><td rowspan="2">Select data of P4 pin</td></tr>
<tr><td></td><td></td><td>1</td><td>When port output: 1 output, when R output: polarity.</td></tr>
<tr><td>B</td><td>PTD5</td><td>0</td><td>When port output: 0 output, when CSYN output: negative polarity.</td><td rowspan="2">Select data of P5 pin</td></tr>
<tr><td></td><td></td><td>1</td><td>When port output: 1 output, when CSYN output: polarity.</td></tr>
<tr><td>C</td><td>SRAND0</td><td>0</td><td rowspan="4"><table><tr><th>SRAND 1</th><th>SRAND 0</th><th colspan="2">SRAND2</th></tr><tr><td></td><td></td><td>0</td><td>1</td></tr><tr><td>0</td><td>0</td><td>Complete border = 1 dot</td><td>Right and dot border = 1 dot</td></tr><tr><td>0</td><td>1</td><td>Complete border = 2 dot</td><td>Right and dot border = 2 dot</td></tr><tr><td>1</td><td>0</td><td>Complete border = 3 dot</td><td>Right and dot border = 3 dot</td></tr><tr><td>1</td><td>1</td><td>Complete border = 4 dot</td><td>Right and dot border = 4 dot</td></tr></table></td><td rowspan="4">Condition of border display is changeable.</td></tr>
<tr><td></td><td>SRAND0</td><td>1</td></tr>
<tr><td>D</td><td>SRAND1</td><td>0</td></tr>
<tr><td></td><td></td><td>1</td></tr>
<tr><td>E</td><td>SRAND2</td><td>0</td><td colspan="2">Vertical direction is 1 dot only.</td></tr>
<tr><td></td><td></td><td>1</td><td colspan="2"></td></tr>
<tr><td>F</td><td>ALL24</td><td>0</td><td>Blanking with all 40 characters in matrix-outline mode</td><td rowspan="2">Horizontal display range can be altered when all characters are in matrix-outline size.
At external synchronous, set to 0.
Operation of character code FF16 becomes ineffective.</td></tr>
<tr><td></td><td></td><td>1</td><td>Horizontal display period fully blanked with all characters in matrix-outline size.</td></tr>
<tr><td>10</td><td>PC0</td><td>0</td><td rowspan="18">Display frequency fT control
$f_T = f_H \times \{ \sum_{n=0}^{7} (2^n PC_n) + 512 \}$</td><td rowspan="18">PC7 to PC0 < 3616,
PC7 to PC0 > C616 is not available.</td></tr>
<tr><td></td><td></td><td>1</td></tr>
<tr><td>11</td><td>PC1</td><td>0</td></tr>
<tr><td></td><td></td><td>1</td></tr>
<tr><td>12</td><td>PC2</td><td>0</td></tr>
<tr><td></td><td></td><td>1</td></tr>
<tr><td>13</td><td>PC3</td><td>0</td></tr>
<tr><td></td><td></td><td>1</td></tr>
<tr><td>14</td><td>PC4</td><td>0</td></tr>
<tr><td></td><td></td><td>1</td></tr>
<tr><td>15</td><td>PC5</td><td>0</td></tr>
<tr><td></td><td></td><td>1</td></tr>
<tr><td>16</td><td>PC6</td><td>0</td></tr>
<tr><td></td><td></td><td>1</td></tr>
<tr><td>17</td><td>PC7</td><td>0</td></tr>
<tr><td></td><td></td><td>1</td></tr>
</table>

Note: At EX (address 2B016) = “0” (external synchronous), setting “1” of ALL24 register is not available.
Refer Fig. 2 about PTC0 to 5, PTD0 to 5.

(9) Address 2B0$_{16}$

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>EX</td><td>0</td><td>External synchronization</td><td>(Note 1)</td></tr>
<tr><td></td><td></td><td>1</td><td>Internal synchronization</td><td></td></tr>
<tr><td>1</td><td>SCOR</td><td>0</td><td>Superimpose black and white display</td><td>Valid at only register “EX”=0 (at external synchronous) (Note 2, 3 and 4)</td></tr>
<tr><td></td><td></td><td>1</td><td>Superimpose coloring display</td><td></td></tr>
<tr><td>2</td><td>SELCOR</td><td>0</td><td>Normal</td><td>Refer to Table 3 and 6.</td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td><td></td></tr>
<tr><td>3</td><td>—</td><td>0</td><td>Must be cleared to 0.</td><td></td></tr>
<tr><td></td><td></td><td>1</td><td></td><td></td></tr>
<tr><td>4</td><td>DSPON</td><td>0</td><td>Digital output display OFF</td><td></td></tr>
<tr><td></td><td></td><td>1</td><td>Digital output display ON</td><td></td></tr>
<tr><td>5</td><td>DSPONV</td><td>0</td><td>Composite video output display OFF</td><td></td></tr>
<tr><td></td><td></td><td>1</td><td>Composite video output display ON</td><td></td></tr>
<tr><td>6</td><td>—</td><td>0</td><td>Must be cleared to 0.</td><td></td></tr>
<tr><td></td><td></td><td>1</td><td></td><td></td></tr>
<tr><td>7</td><td>BLK</td><td>0</td><td>Matrix outline</td><td>Only at register “DSP1xx” = 1 (xx = 00 ~ 16) is valid.</td></tr>
<tr><td></td><td></td><td>1</td><td>Matrix outline + border (border color is black)</td><td></td></tr>
<tr><td>8</td><td>SEPV0</td><td>0</td><td rowspan="3"><table><tr><th>SEPV1</th><th>SEPV0</th><th>Composite Sync Spearation Function</th></tr><tr><td>0</td><td>0</td><td>Separation is performed during 1 in vertical blanking period</td></tr><tr><td>0</td><td>1</td><td>Separation is performed during 2 in vertical blanking period</td></tr><tr><td>1</td><td>0</td><td>Separation is performed during 3 in vertical blanking period</td></tr><tr><td>1</td><td>1</td><td>Setting disabled</td></tr></table></td><td rowspan="3">Method of sync separation from composite video.
 

Case 1 condition: vertical sync must repeat 2X within 2 or 3; indicates this area.</td></tr>
<tr><td></td><td></td><td>1</td></tr>
<tr><td>9</td><td>SEPV1</td><td>0</td></tr>
<tr><td></td><td></td><td>1</td><td></td><td></td></tr>
<tr><td>A</td><td>TEST15</td><td>0</td><td rowspan="3">Test mode (Must be cleared to 0.)</td><td rowspan="3"></td></tr>
<tr><td></td><td></td><td>1</td></tr>
<tr><td>B</td><td>TEST16</td><td>0</td></tr>
<tr><td></td><td></td><td>1</td><td></td><td></td></tr>
<tr><td>C</td><td>PALH</td><td>0</td><td>Interlace/noninterlace normal mode</td><td>Valid at only PAL and MPAL mode.</td></tr>
<tr><td></td><td></td><td>1</td><td>Interlace/noninterlace expansion mode</td><td></td></tr>
<tr><td>D</td><td>MPAL</td><td>0</td><td rowspan="3"><table><tr><th>PAL/NTSC</th><th>MPAL</th><th>Format</th></tr><tr><td>0</td><td>0</td><td>NTSC</td></tr><tr><td>0</td><td>1</td><td>M-PAL</td></tr><tr><td>1</td><td>0</td><td>PAL</td></tr><tr><td>1</td><td>1</td><td>Setting disabled</td></tr></table></td><td rowspan="3"></td></tr>
<tr><td></td><td></td><td>1</td></tr>
<tr><td>E</td><td>PAL/$\overline{\text{NTSC}}$</td><td>0</td></tr>
<tr><td></td><td></td><td>1</td><td></td><td></td></tr>
<tr><td>F</td><td>$\overline{\text{INT}}$/NON</td><td>0</td><td>Interlace</td><td></td></tr>
<tr><td></td><td></td><td>1</td><td>Noninterlace</td><td></td></tr>
</table>

Notes 1: For internal synchronization, shut out (mute) the external video signal input, outside the IC. This avoids external video signal leaks inside the IC.
2: For superimposed color displays, input an fsc signal which is synchronized with the color burst of the composite video signal (input to the CVIN pin) to the OSCIN pin.
3: When EX (address 2B016) = “1” (internal synchronization), set the SCOR register to “0”.
4: When using a crystal oscillator (for the fsc input) between the OSCIN and OSCOUT pin, set the SCOR register to “0”.

(9) Address 2B0$_{16}$ (cont.)

DA	Register	Contents		Remarks
		Status	Function	
10	LEVEL0	0	Composite video generation is off.	Refer to Table 4 and 5.
		1	Composite video generation is on.	
11	LEVEL1	0	Display clock is on (oscillating).	
		1	Display clock is off (not oscillating).	
12	LEVEL2	0	Sync separation is disabled.	
		1	Sync separation is enabled.	
13	TEST24	0	Test mode (Must be cleared to 0.)	
		1		
14	TEST17	0		
		1		
15	TEST18	0		
		1		
16	TEST19	0		
		1		
17	—	0	Must be cleared to 0.	
		1		

REGISTER CONSTRUCTION COMPOSITION

Table 3 Color and phase of NTSC, PAL (SELCOR = 0)

PHASE2 / LINEB	PHASE1 / LINEG	PHASE0 / LINER	Phase (rad) NTSC	Phase (rad) PAL	Color
0	0	0	—	—	Black
0	0	1	7π/16	± 7π/16	Red
0	1	0	27π/16	∓5π/16	Green
0	1	1	π/16	± π/16	Yellow
1	0	0	17π/16	∓15π/16	Blue
1	0	1	—	—	Gray
1	1	0	23π/16	∓9π/16	Cyan
1	1	1	—	—	White

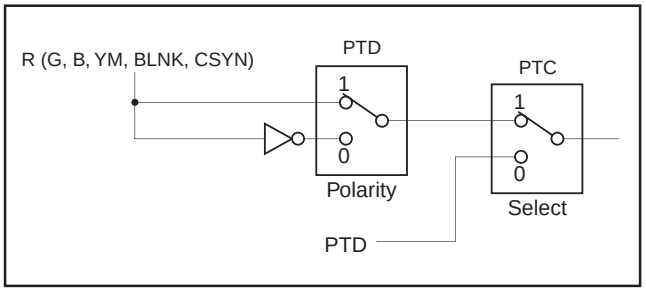


Fig. 2 Switching port output with R, G and B output

Table 4 Setting condition at LEVEL 0, 1 and 2

	At display clock operates	At display clock stops
LEVEL1	0	1
DSPON	1	0
DSPONV	1	0
$\overline{CS}$ pin	L	H

No character display at display clock

Table 5 Setting condition at LEVEL 0, 1 and 2 (at operation)

	Operation state	Stop state
LEVEL0	1	0
LEVEL1	0	1
LEVEL2	1	0

Table 6 Video signal level (SELCOR = 0)

Color name	Phase (rad) NTSC	Phase (rad) PAL	Luminance level (V) (Note1) Min.	Typ.	Max.	Chroma amplitude (Notes 1 and 2) Min.	Typ.	Max.
Sync	—	—	1.40	1.50	1.60	—	—	—
Pedestal	—	—	2.00	2.10	2.20	—	—	—
Color Burst	0	±4π/16	2.00	2.10	2.20	—	1.00	—
Black	—	—	2.00	2.10	2.20	—	—	—
Red	7π/16 ± 2π/16	± 7π/16 ± 2π/16	2.00	2.25	2.35	1.23	1.46	1.69
Green	27π/16 ± 2π/16	∓ 5π/16 ± 2π/16	2.15	2.45	2.55	1.11	1.31	1.51
Yellow	π/16 ± 2π/16	± π/16 ± 2π/16	2.35	2.75	2.85	0.85	1.00	1.15
Blue	17π/16 ± 2π/16	∓ 15π/16 ± 2π/16	2.65	2.15	2.75	0.91	1.08	1.25
Gray	—	—	—	2.55	—	—	—	—
Cyan	23π/16 ± 2π/16	∓ 9π/16 ± 2π/16	2.40	2.50	2.60	1.37	1.62	1.86
White	—	—	2.85	2.95	3.05	—	—	—

Notes 1: The luminance level and the chroma amplitude of this video signal are ruled only for PAL method.
2: The chroma amplitude is ruled by each color's chroma and color burst's chroma.

DISPLAY FORMS

1. Blanking mode

Display forms are shown in Table 7, display forms at each display mode are shown in Fig. 3.

Table 7 Display forms

Display mode	DSP1 XX (Address 2AC16)	DSP0 XX (Address 2AB16)	BLNK output
Character	0	0	Character size
Border	0	1	Border size
Matrix-outline	1	0	All blanking
Halftone	1	1	Blanking OFF

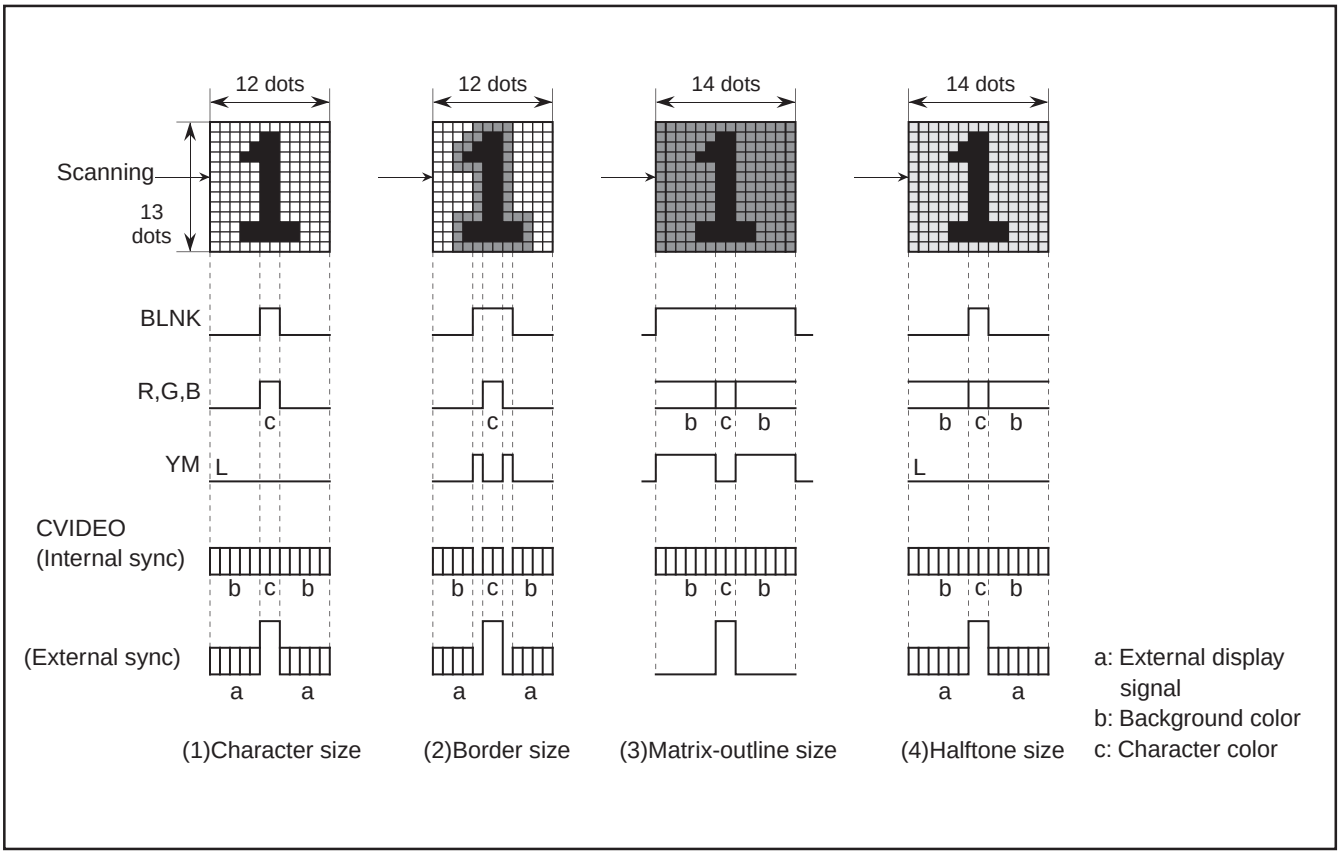


Fig. 3 Display forms at each display mode

For matrix and halftone, a character's number of dots in the horizontal direction increases to 14.
Figure 4 shows a display example for a case where adjacent characters have different background colors and for character code FF_{16}.

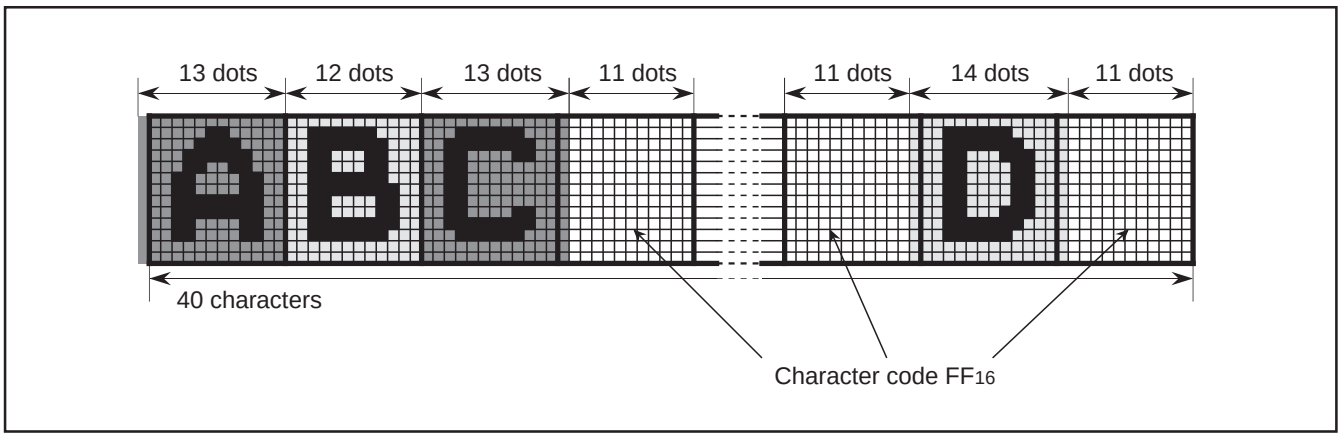
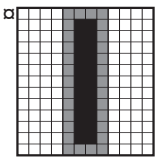
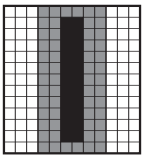
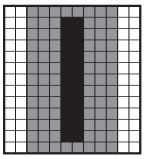
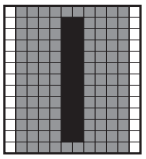
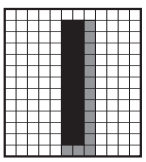
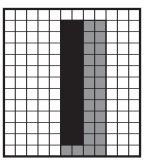
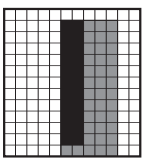
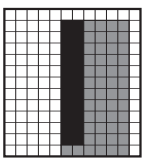


Fig. 4 Number of dots in the horizontal direction at matrix-outline or halftone

2. Border mode

In border mode, characters are displayed with borders. (Refer to Table 7.) In matrix and halftone modes also, characters are displayed with borders if the BLK register (address $2B0_{16}$) is set to 1.
Table 8 lists the types of borders.

Table 8 Bordering

SRAND2 (Address $2AF_{16}$) \ SRAND1, 0	00	01	10	11
0	The zero dot  1dot in horizontal direction	 2 dots in horizontal direction	 3 dots in horizontal direction	 4 dots in horizontal direction
1	 1 dot in horizontal direction	 2 dots in horizontal direction	 3 dots in horizontal direction	 4 dots in horizontal direction

Horizontal direction bordering is only 1 dot. When the character extends to the top line of the matrix, no border is left at the top, and when the character extends to the bottom (12th) line of the matrix, no border is left at the bottom.

3. Setting matrix outline

The ALL24 register (address $2AF_{16}$) allows you to set a matrix outline. A matrix outline can be set for each line by using the DSP1XX register (address $2AC_{16}$) .
However, this setting is inhibited if the EX register (address $2B0_{16}$) is 0 (external sync). An example of how you set a matrix outline is shown in Figure 5.

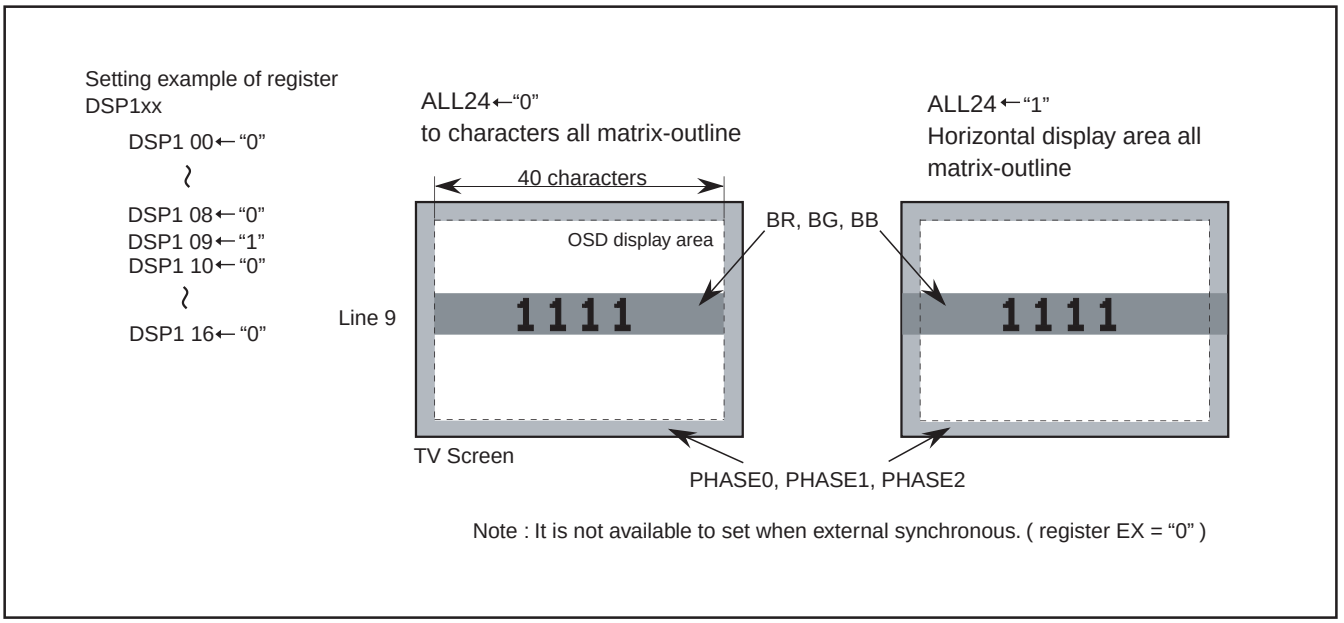


Fig. 5 Setting example all matrix-outline area

4. Blinking mode

Two patterns blinking by register BLINK3 (address $2A9_{16}$) or BLINK bit of display RAM.
Blinking mode is shown in Table 9 (SYRAM do not blink).

Use registers BLINK0, 1, and 2 (address $2A9_{16}$) to set the duty ratio and period that determines the blinking time. Tables 12 and 13 list the relationship between the register settings and the duty ratio and period.

Table 9 Blinking mode

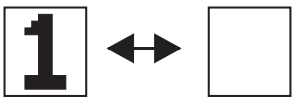
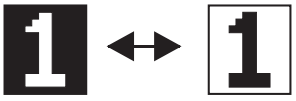
BLINK3	Blinking mode	at blinking OFF
0	Blinking 	Normal 
1	Normal character, reversed character alternation display 	Reverse 

Table 10 Setting of duty ratio

BLINK1 \ BLINK0	0	1
0	Blink OFF	Duty 25%
1	Duty 50%	Duty 75%

Table 11 Setting of cycle

BLINK2	Cycle
0	Approximately 1 second (Vertical sync divided into 1/64)
1	Approximately 0.5 second (Vertical sync divided into 1/32)

5. Scroll display mode

The scroll display mode is entered by setting registers SBIT0 to 3 (SA), SLIN0 to 4 (SB), SST0 to 4 (SC), and SEND0 to 4 (SD) (all at address $2AE_{16}$). (Scroll is turned off when SD = 0.)

The screen is scrolled in the range from the (SC)'th line to the (SD-1)'th line, and sections above and below this range are fixed. The beginning line and beginning dot of scroll are the (SA)'th dot on the (SB)'th line.

The screen can be scrolled up or down by successively incrementing or decrementing SA and SB.

Figure 6 shows examples of how the display is scrolled. The scroll range in these examples contains 12 lines (second to the 13th lines). However, the screen can display only 11 lines at a time, and the remaining one line is handled as a dummy line and not displayed.

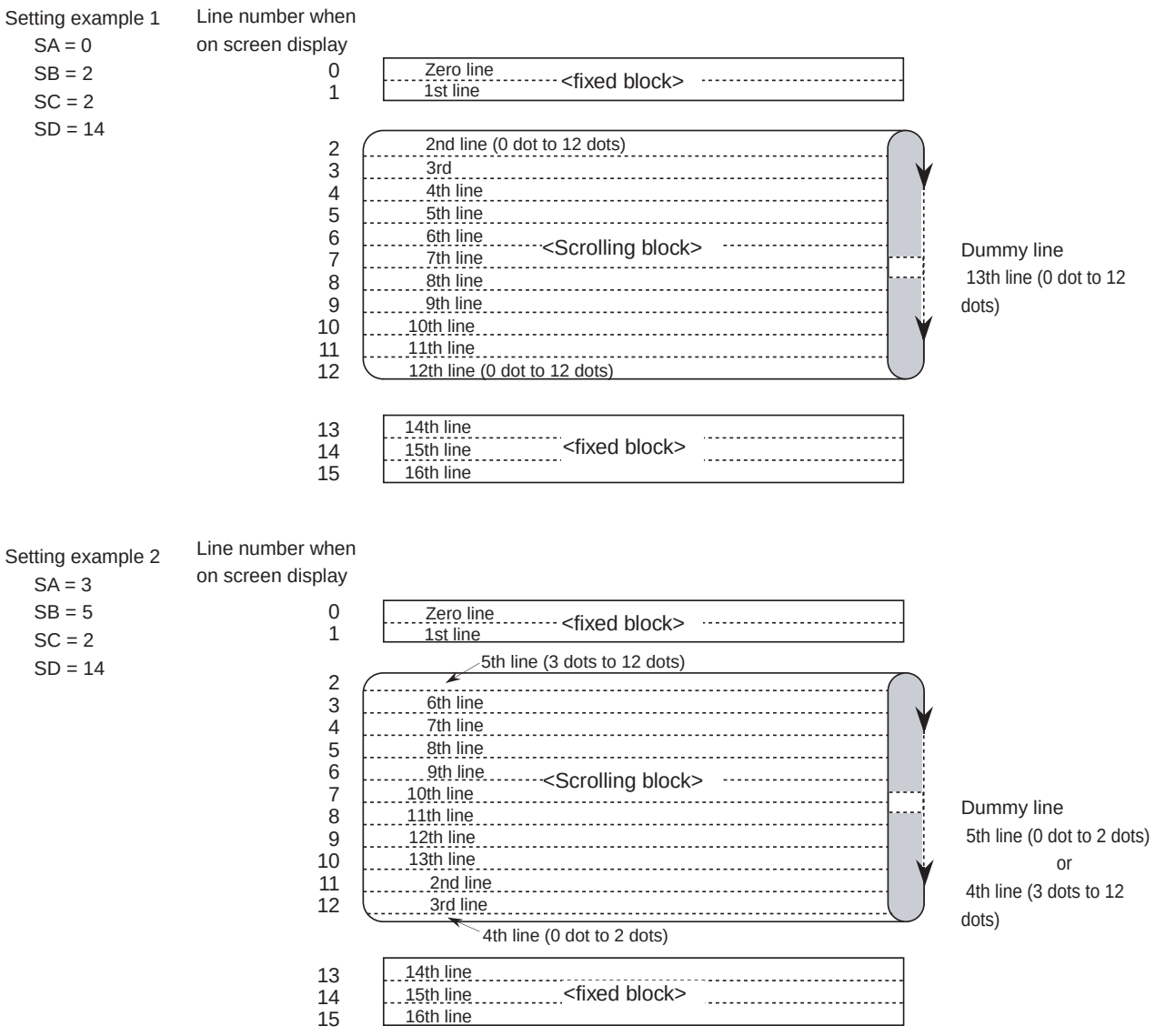


Fig. 6 Scrolling example

6. Character font

(1) Character ROM

Images are composed on a 12 × 13 dot matrix, and characters can be linked vertically and horizontally with other characters to allow the display the continuous symbols.

Character code FF_{16} is fixed as blank, without a background.

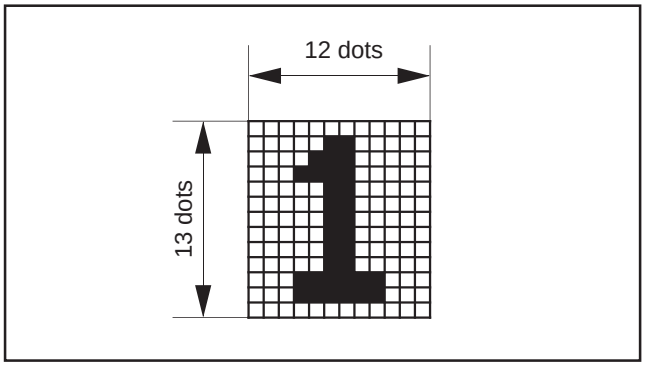


Fig. 7 Character construction

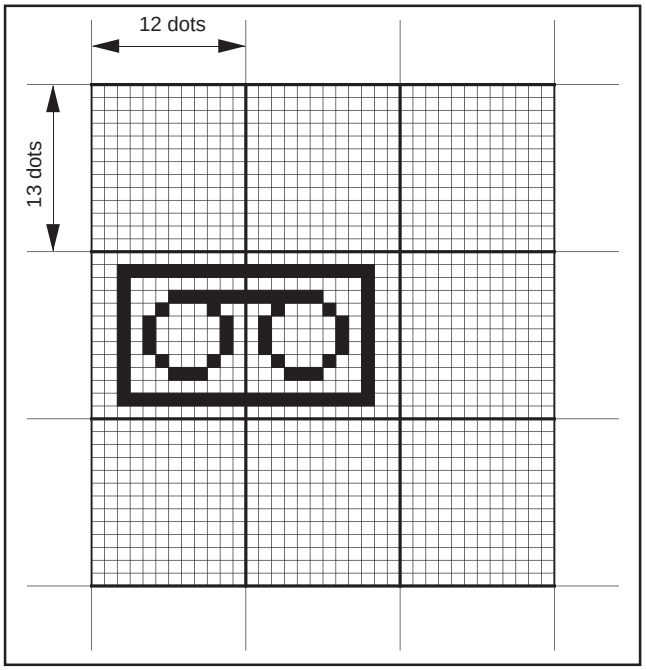
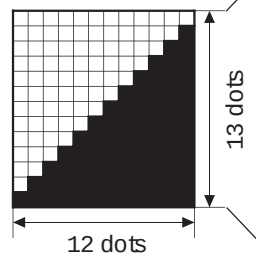


Fig. 8 Example for displaying a continuous pattern

(2) SYRAM

You can set characters for 7 letters per screen (SYRAM code 00_{16} to 06_{16}). Figure 9 shows an example of how to set.
Use display RAM's SYC2 to 0 (00_{16} to 06_{16}) to specify SYRAM.
Note that SYRAM code 07_{16} is fixed to a blank, so you cannot set a character font to this code.
If you do not put SYRAM and a character together, use code 07_{16}.

(ex) SYRAM code 00_{16} ..... Set character by setting data to address 300_{16} to $30C_{16}$



Address	DA															
	17	…	D	C	B	A	9	8	7	6	5	4	3	2	1	0
300_{16}	0	…	0	*	0	0	0	0	0	0	0	0	0	0	0	0
301_{16}	0	…	0	*	0	0	0	0	0	0	0	0	0	0	0	1
302_{16}	0	…	0	*	0	0	0	0	0	0	0	0	0	0	1	1
303_{16}	0	…	0	*	0	0	0	0	0	0	0	0	0	1	1	1
304_{16}	0	…	0	*	0	0	0	0	0	0	0	0	1	1	1	1
305_{16}	0	…	0	*	0	0	0	0	0	0	0	1	1	1	1	1
306_{16}	0	…	0	*	0	0	0	0	0	0	1	1	1	1	1	1
307_{16}	0	…	0	*	0	0	0	0	0	1	1	1	1	1	1	1
308_{16}	0	…	0	*	0	0	0	0	1	1	1	1	1	1	1	1
309_{16}	0	…	0	*	0	0	0	1	1	1	1	1	1	1	1	1
$30A_{16}$	0	…	0	*	0	0	1	1	1	1	1	1	1	1	1	1
$30B_{16}$	0	…	0	*	0	1	1	1	1	1	1	1	1	1	1	1
$30C_{16}$	0	…	0	*	1	1	1	1	1	1	1	1	1	1	1	1

13 dots

12 dots

Color expansion bit SYEX (set for each dot line)
The HIDE register (address $2AA_{16}$) becomes valid for only the dot line where * = 1.
For details, refer to the next section, "(3) Compounding character ROM and SYRAM."

1 bit: 1 dot of character

Fig. 9 Setting example of SYRAM

(3) Compounding character ROM and SYRAM

You can compound characters in character ROM with SYRAM. The compounding method is determined by the SYEX color expansion bit and the HIDE register (address $2AA_{16}$).

For dot lines where SYEX = 0, the SYRAM color is set by the display RAM's SR, SG, and SB irrespective of the HIDE register's content.

If the HIDE register's content is 0, the SYRAM color for dot lines where SYEX = 1 is set by the LINER, LINEG, and LINEB registers (address $2AC_{16}$).

If the HIDE register's content is 1, the character ROM part of the dot lines where SYEX = 1 is overwritten in HIDE mode with colors set by the LINER, LINEG, and LINEB registers irrespective of the ROM's content and color. The color of the SYRAM part is set by the display RAM's SR, SG, and SB as in the case of dot lines where SYEX = 0.

Figure 10 shows an example for each instance of compounding.

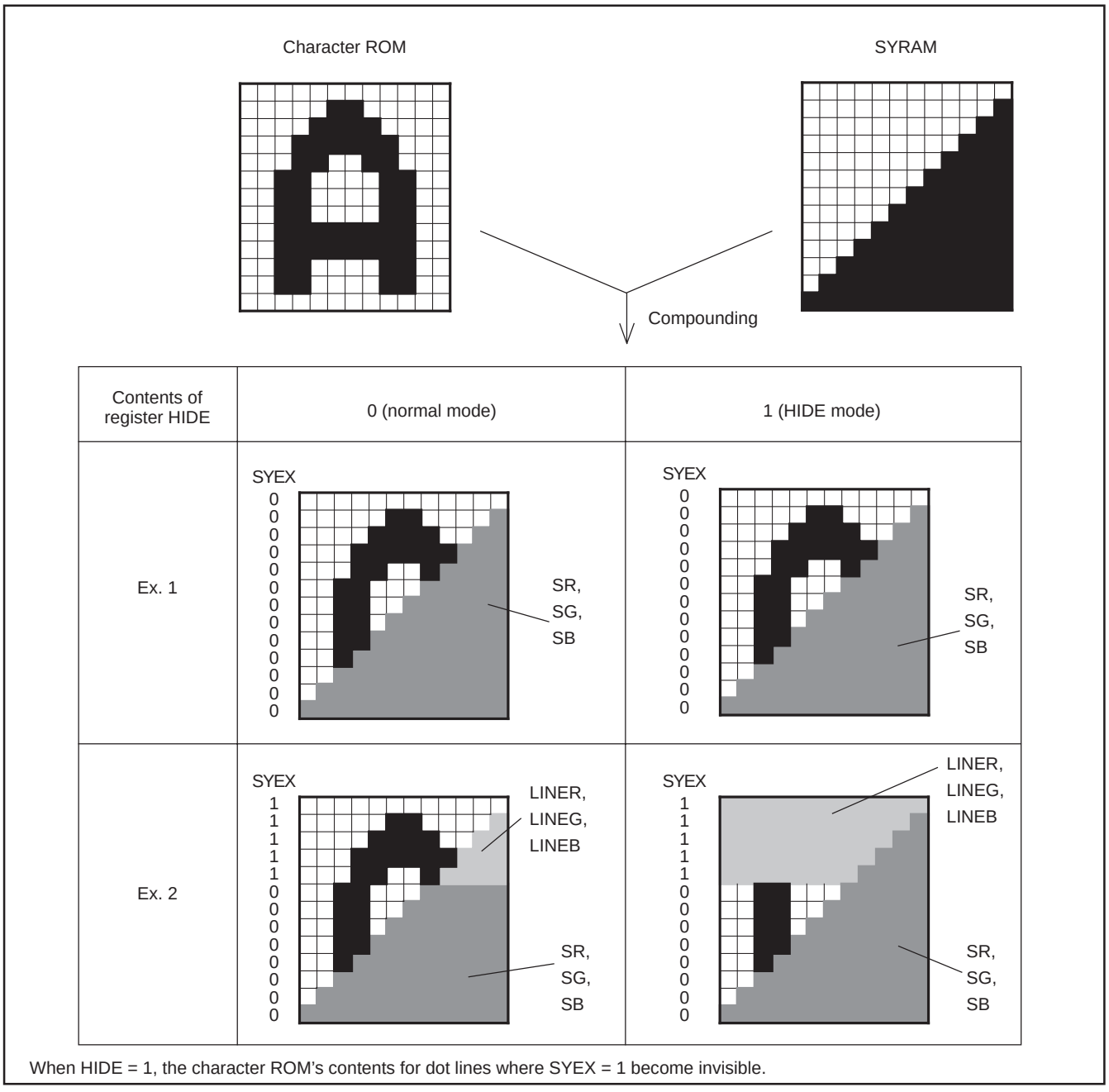


Fig. 10 Compounding example

EXAMPLE FOR DATA INPUT

Use an 8-bit parallel × 3 serial input to set data in the display RAM, display control register, and SYRAM. Table 12 lists an example of how data is set.

Table 12 Data setting

No.	Contents		DA 17	DA 16	DA 15	DA 14	DA 13	DA 12	DA 11	DA 10	DA F	DA E	DA D	DA C	DA B	DA A	DA 9	DA 8	DA 7	DA 6	DA 5	DA 4	DA 3	DA 2	DA 1	DA 0
	Address/data	Remarks																								
1	Address (2B0$_{16}$)	Address setting	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1	0	0	0	0
2	Data (2B0$_{16}$)	Display OFF	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3	Data (300$_{16}$)	Set addresses SYRAM 300$_{16}$ to 36C$_{16}$	0	0	0	0	0	0	0	0	0	0	0	SYEX	0	0	0	S018	S017	S016	S015	S014	S013	S012	S011	S010
4	Data (301$_{16}$)		0	0	0	0	0	0	0	0	0	0	0	SYEX	S01B	S01A	S019	S018	S3E7	S3E6	S3E5	S3E4	S3E3	S3E2	S3E1	S3E0
~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~
93	Data (36C$_{16}$)		0	0	0	0	0	0	0	0	0	0	0	SYEX	BLINK	CB	CG	CR	0	C6	C5	C4	C3	C2	C1	C0
94	Address (000$_{16}$)	Set address	0	0	0	0	0	0	0	0	0	0	0	BR	BLINK	CB	CG	CR	0	C6	C5	C4	C3	C2	C1	C0
95	Data (000$_{16}$)	Set registers address display RAM 000$_{16}$ to 2A7$_{16}$	SB	SG	SR	0	0	0	SYC 2	SYC 1	SYC 0	BB	BG	BR	BLINK	CB	CG	CR	0	C6	C5	C4	C3	C2	C1	C0
96	Data (001$_{16}$)		SB	SG	SR	0	0	0	SYC 2	SYC 1	SYC 0	BB	BG	BR	BLINK	CB	CG	CR	0	C6	C5	C4	C3	C2	C1	C0
~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~
773	Data (2A7$_{16}$)		SB	SG	SR	0	0	0	SYC 2	SYC 1	SYC 0	BB	BG	BR	BLINK	CB	CG	CR	0	C6	C5	C4	C3	C2	C1	C0
774	Data (2A8$_{16}$)	Set registers address 2A8$_{16}$ to 2AF$_{16}$	0	0	0	0	0	0	0	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
775	Data (2A9$_{16}$)		0	0	0	BLINK 3	BLINK 2	BLINK 1	BLINK 0	HSZ 16	HSZ 15	HSZ 14	HSZ 13	HSZ 12	HSZ 11	HSZ 10	HSZ 9	HSZ 8	HSZ 7	HSZ 6	HSZ 5	HSZ 4	HSZ 3	HSZ 2	HSZ 1	HSZ 0
776	Data (2AA$_{16}$)		0	0	0	0	EQP	0	HIDE	VSZ 16	VSZ 15	VSZ 14	VSZ 13	VSZ 12	VSZ 11	VSZ 10	VSZ 9	VSZ 8	VSZ 7	VSZ 6	VSZ 5	VSZ 4	VSZ 3	VSZ 2	VSZ 1	VSZ 0
777	Data (2AB$_{16}$)		0	0	0	0	PHASE 2	PHASE 1	PHASE 0	DSP 016	DSP 015	DSP 014	DSP 013	DSP 012	DSP 011	DSP 010	DSP 009	DSP 008	DSP 007	DSP 006	DSP 005	DSP 004	DSP 003	DSP 002	DSP 001	DSP 000
778	Data (2AC$_{16}$)		0	0	0	1	LINE B	LINE G	LINE R	ERS 16	ERS 15	ERS 14	ERS 13	ERS 12	ERS 11	ERS 10	ERS 9	ERS 8	ERS 7	ERS 6	ERS 5	ERS 4	ERS 3	ERS 2	ERS 1	ERS 0
779	Data (2AD$_{16}$)		0	0	0	SERS 0	0	0	0	SEND 2	SEND 1	SEND 0	SRAND 1	SRAND 0	PTD 5	PTD 4	PTD 3	PTD 2	PTD 1	PTD 0	PTC 5	PTC 4	PTC 3	PTC 2	PTC 1	PTC 0
780	Data (2AE$_{16}$)		0	0	0	0	0	SEND 4	SEND 3	SEND 2	SEND 1	SRAND 2	SST 4	SST 3	SST 2	SST 1	SST 0	SLIN 4	SLIN 3	SLIN 2	SLIN 1	SLIN 0	SBIT 3	SBIT 2	SBIT 1	SBIT 0
781	Data (2AF$_{16}$)		PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	ALL24		ERS 14	ERS 13	ERS 12	ERS 11	ERS 10	ERS 9	ERS 8	ERS 7	ERS 6	ERS 5	ERS 4	ERS 3	ERS 2	ERS 1
782	Data (2B0$_{16}$)	Display ON	0	0	0	0	0	1	0	1	1	0	0	0	0	0	SEPV 1	SEPV 0	BLK	0	1	1	0	0	0	EX

SERIAL DATA INPUT TIMING

(1) The address consists of 8 bits × 3.
(2) The data consists of 8 bits × 3.
(3) The 8 bits × 3 in the SCK after the $\overline{CS}$ signal has fallen are the address, and for succeeding input data, the address is incremented every 24 bits (8 bits × 3). Refer to Fig.12 about detail for address increment.

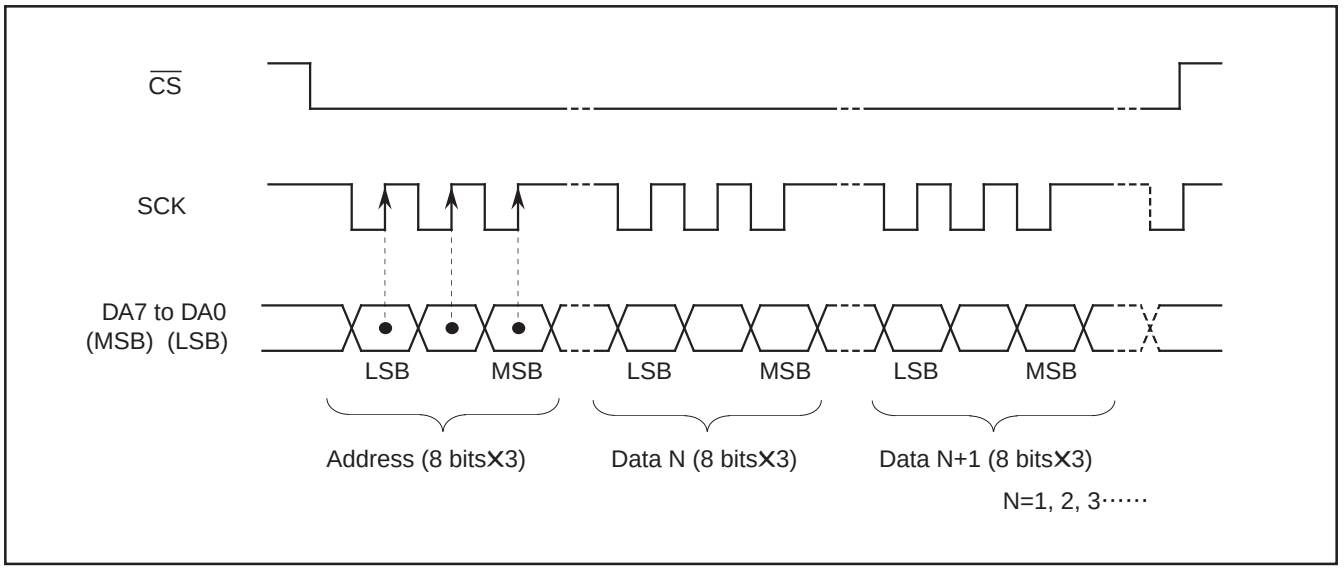
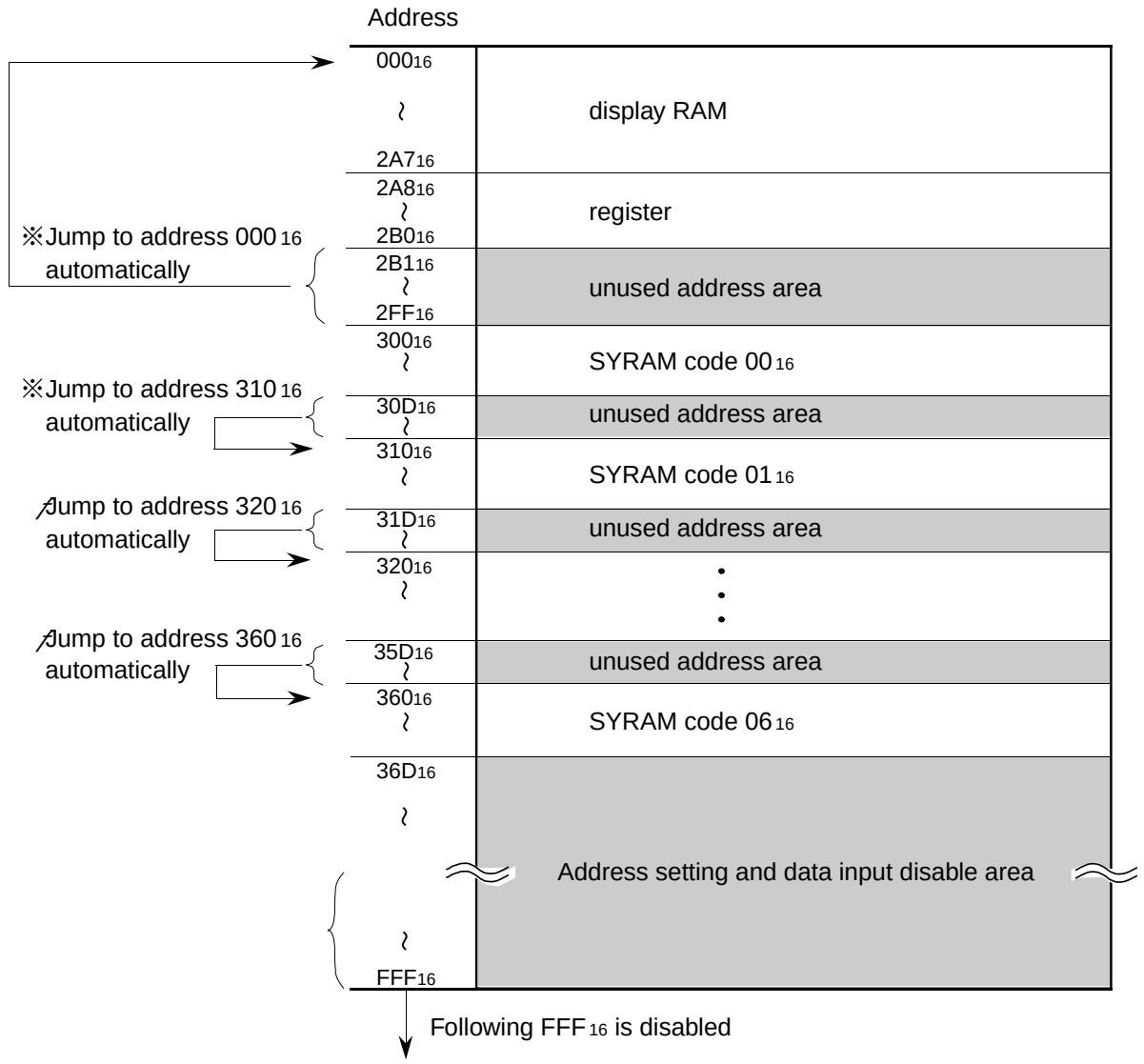


Fig. 11 Serial input timing



When entering data, note that although addresses are incremented every data entry (8 bits × 3), if an address value falls in the unused address area, it is automatically converted to the address value indicated by the arrow. When entering SYRAM data, for example, you can set this data simply by setting address 300_{16} first and then entering data 300_{16} to $30C_{16}$ (SYRAM code 00_{16}) and next data 310_{16} to $31C_{16}$ (SYRAM code 01_{16}). The same applies for SYRAM code 02_{16} to 06_{16}.However, set CS to H after setting SYRAM code 06_{16} (360_{16} to $36C_{16}$).

Fig. 12 Address construction

Notes on others

1. At system start-up

At system start-up, always set the $\overline{AC}$ pin to low level before setting registers.

2. Power supply noise

When power supply noise is generated, the internal oscillator circuit does not stabilize, whereby causing horizontal jitters across the picture display. Therefore, connect a bypass capacitor between the power supply and GND.

3. At power on

When power to the M35062-XXXSP is activated, characters are sometimes output without defining the internal display RAM, composite RAM and register. Also, immediately after power is turned on, up until the oscillator circuit stabilizes, data is sometimes not set correctly in the register. Therefore, use the following start-up procedure.

(a) Activate power. ($\overline{AC}$ pin = "L")
(b) Engage auto clear. ($\overline{AC}$ pin = "H")
(c) Disable data input for a 200 m sec (time enough to allow the internal oscillator circuit to stabilize).
(d) Set register LEVEL n.
(e) Set register PAL/$\overline{NTSC}$.
(f) Set register PC n.
(g) Disable data input for a 20 m sec (time enough to allow the internal oscillator circuit to stabilize).
(h) Set other registers.
(i) Set the SYRAM.
(j) Set the internal display RAM.
(k) Turn registers DSPON and DSPONV on.

4. When resuming internal oscillation from the off state

The internal oscillator circuit stops oscillating when register LEVEL 1 = 1, DSPON = 0, DSPONV = 0 and $\overline{CS}$ pin = "H".
When resuming internal oscillation from the off state, up until the oscillator circuit stabilizes, data is sometimes not set correctly in the register. Therefore, start oscillation as follows.

(a) $\overline{CS}$ pin = "H" (Oscillation off)
(b) $\overline{CS}$ pin ="L" (Oscillation start)
(c) Wait for a 20 m sec (time enough to allow the internal oscillator circuit to stabilize).
(d) Set register LEVEL 1 = 0.
(e) Set other registers, SYRAM and internal display RAM.
(f) Turn registers DSPON and DSPONV on.

5. Other notes on oscillation

Make note of the fact that the internal oscillator circuit cannot stabilize in the below situations.

(a) When the external composite video signal is discontinuous (when changing channels, etc.)
(b) When register PC n setting is changed
(c) When register LEVEL n setting is changed

Before changing settings, turn registers DSPON and DSPONV off. Also, disable data input for 20 m sec after making settings.

6. When no external composite video signal is input

Without a signal, characters cannot be displayed by external synchronization. Therefore, switch to internal synchronization.

7. When signal level of the external composite video signal is extremely poor

With a weak electric field, character display is uncontrollable by external synchronization. Therefore, switch to internal synchronization.

8. When a crystal oscillator is used as the IC's fsc input

It is possible to connect a crystal oscillator between OSCIN and OSCOUT to input the subcarrier frequency (fsc) signal to the OSCIN pin. Talk with the manufacturer of the crystal oscillator you want to use about matching it to this IC.
However, when using a crystal oscillator, it is not possible to superimpose colors. Therefore, set the SCOR register (address $2B0_{16}$ in DAI register) to "0".

Crystal oscillator frequency
- NTSC system: 3.580 MHz
- PAL system: 4.434 MHz
- M-PAL system: 3.576 MHz

9. Notes on superimposed colors

(1) Register setting
The below table gives register settings for superimposed colors.

Register / Broad-casting method	PAL/$\overline{\text{NTSC}}$	MPAL	EX	SCOR	PHIN pin
NTSC	0	0	0	1	Connect to GND
PAL	1	0	0	1	Input control signal. Refer to (2)
M-PAL	0	1	0	1	Input control signal. Refer to (2)

(2) Signal input to PHIN (23-pin) pin
It is necessary to input a control signal for alternating color burst phase (CB1/CB2) every other scanning line. The signal is input into the PHIN (23-pin) pin.
The below figure shows timing for the signal input to the PHIN (23-pin) pin.

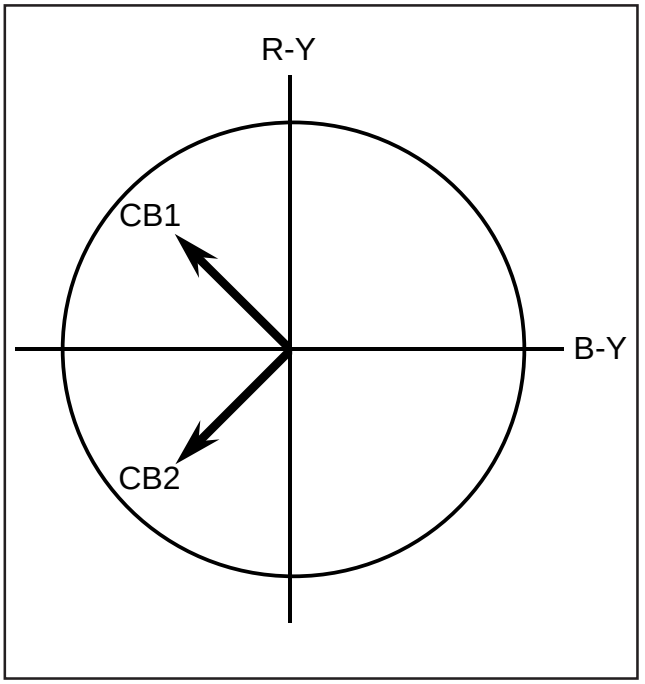
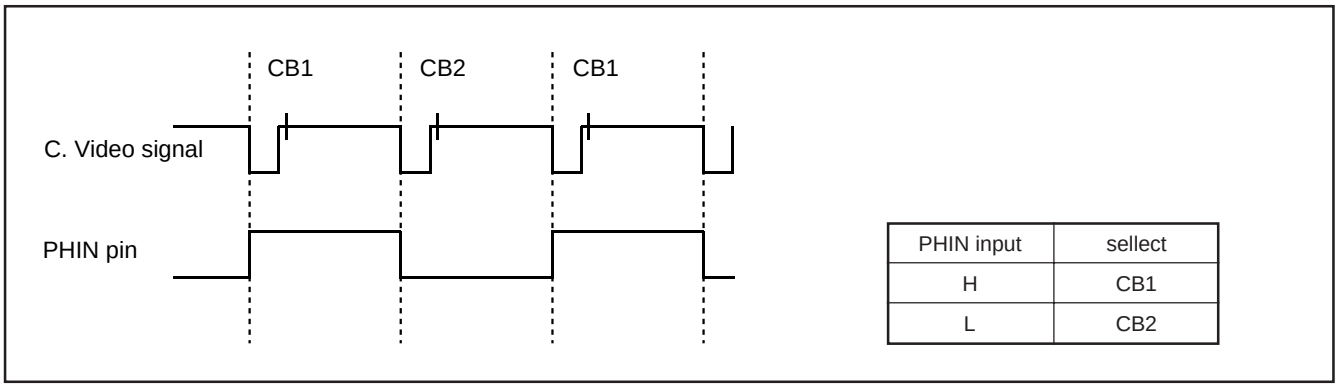


Fig. 13 Bector phase of PAL, M-PAL method



PHIN input	sellect
H	CB1
L	CB2

Fig. 14 Signal input timing for PHIN (23-pin) pin

10. Notes on fsc signal input

(1) This IC amplifies the subcarrier frequency (fsc) signal (NTSC system: 3.580 MHz, PAL system: 4.434 MHz, M-PAL system: 3.576 MHz) input to the OSCIN pin and generates the composite video signal internally.
The amplified fsc signal can be destabilized in the following cases.
(a) When the fsc signal is outside of recommended operating conditions
(b) When the waveform of the fsc signal is distorted
(c) When DC level in the fsc waveform fluctuates
When the amplified signal is unstable, the composite video signal generated inside the IC is also unstable in terms of synchronization with the subcarrier and phase.
Consequently, this results in color flicker and lost synchronization when the composite video signal is generated. Make note of the fact that this may prevent a stable blue background from being formed.

(2) When switching to internal synchronization from external synchronization (fsc signal is OFF), start fsc signal input 20 m sec or more before the internal oscillator circuit stabilizes.

11. Procedure for fixing to the first field in PAL system

The M35062-XXXSP allows to fix the scanning fields to the first field during PAL system noninterlaced display (internally synchronized). In this case, the display must be placed in the interlaced mode temporarily before entering the noninterlaced mode in order to ensure that the scanning fields are fixed. Follow the setup procedure described below.

(1) When powering on
(a) Turn on the power ($\overline{AC}$ pin = low).
(b) Deactivate auto clear ($\overline{AC}$ pin = high).
(c) Disable data input during a 200 ms wait state (internal stabilization period).
(d) Set the registers LEVEL 0 and 2 = high and LEVEL 1 = low.
(e) Disable data input during a 20 ms wait state (internal oscillator stabilization period).
(f) Set the registers EX and PAL/$\overline{NTSC}$ = high and $\overline{INT}$/NON = low. (The display is temporarily placed in the interlaced mode.)
(g) Disable data input during a 30 ms wait state (internal oscillator stabilization period).
(h) Set the registers $\overline{INT}$/NON and PALH = high (for 628 scanning lines). (The scanning fields are fixed to the first field.)
(i) Set up the register PCn.
(j) Disable data input during a 20 ms wait state (internal oscillator stabilization period).
(k) Set up other registers.
(l) Set up SYRAM.
(m) Set up the display RAM.
(n) Set the registers DIPON and DISPONV = high.(The display is turned on.)

(2) To switch from external sync to internal sync when the oscillator is already stable
(a) Set the registers DIPON and DISPONV = low. (The display is turned off.)
(b) Disable data input during a 20 ms wait state (internal oscillator stabilization period).
(c) Set the registers EX and PAL/$\overline{NTSC}$ = high and $\overline{INT}$/NON = low. (The display is temporarily placed in the interlaced mode.)
(d) Disable data input during a 30 ms wait state (internal oscillator stabilization period).
(e) Set the registers $\overline{INT}$/NON and PALH = high (for 628 scanning lines). (The scanning fields are fixed to the first field.)
(f) Set up other registers, SYRAM, and display RAM.
(g) Set the registers DIPON and DISPONV = high. (The display is turned on.)

M35062-XXXSP PERIPHERAL CIRCUIT (For external fsc input)

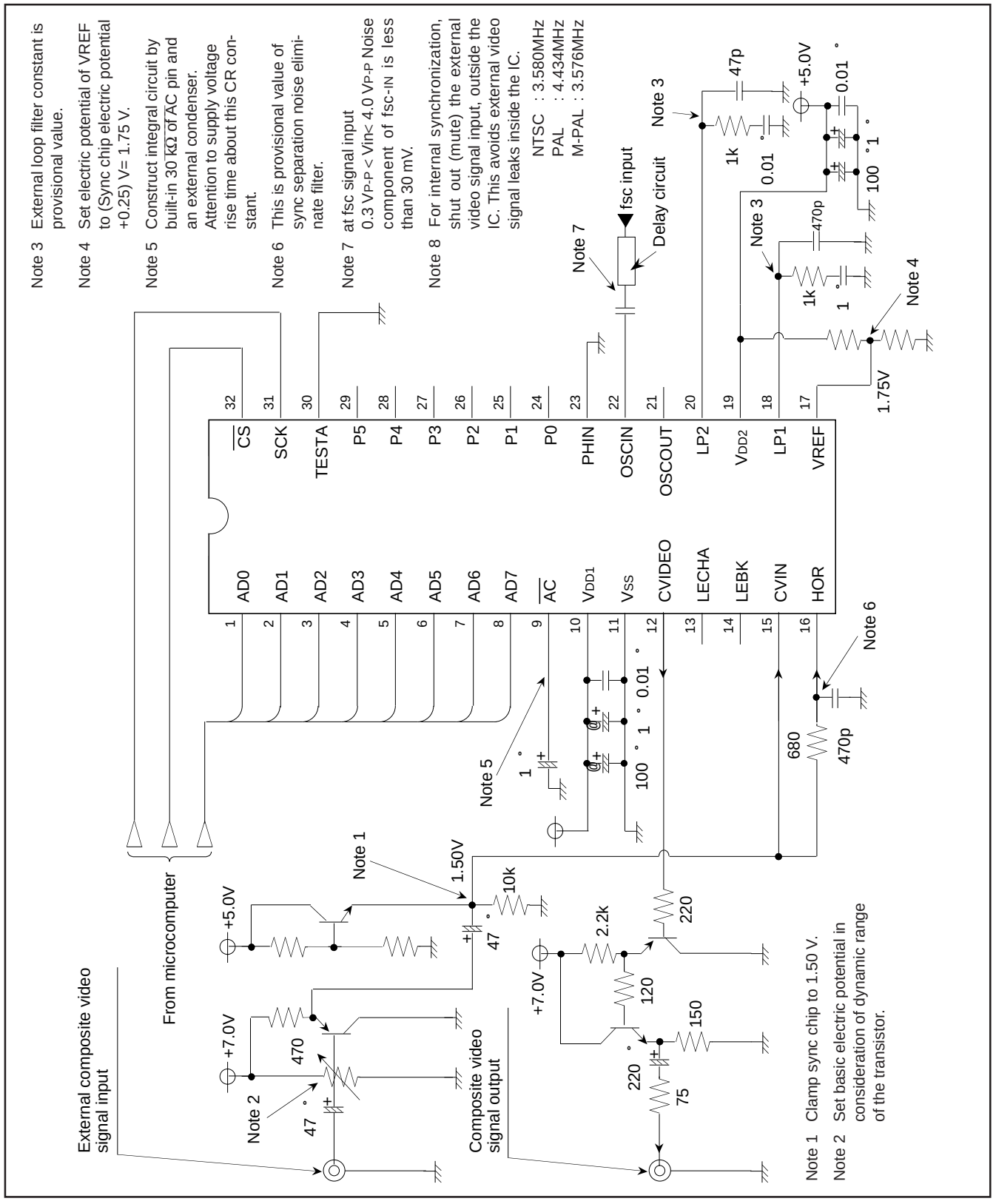


Fig.15 M35062-XXXSP example of peripheral circuit

M35062-XXXSP PERIPHERAL CIRCUIT (When using a crystal oscillator)

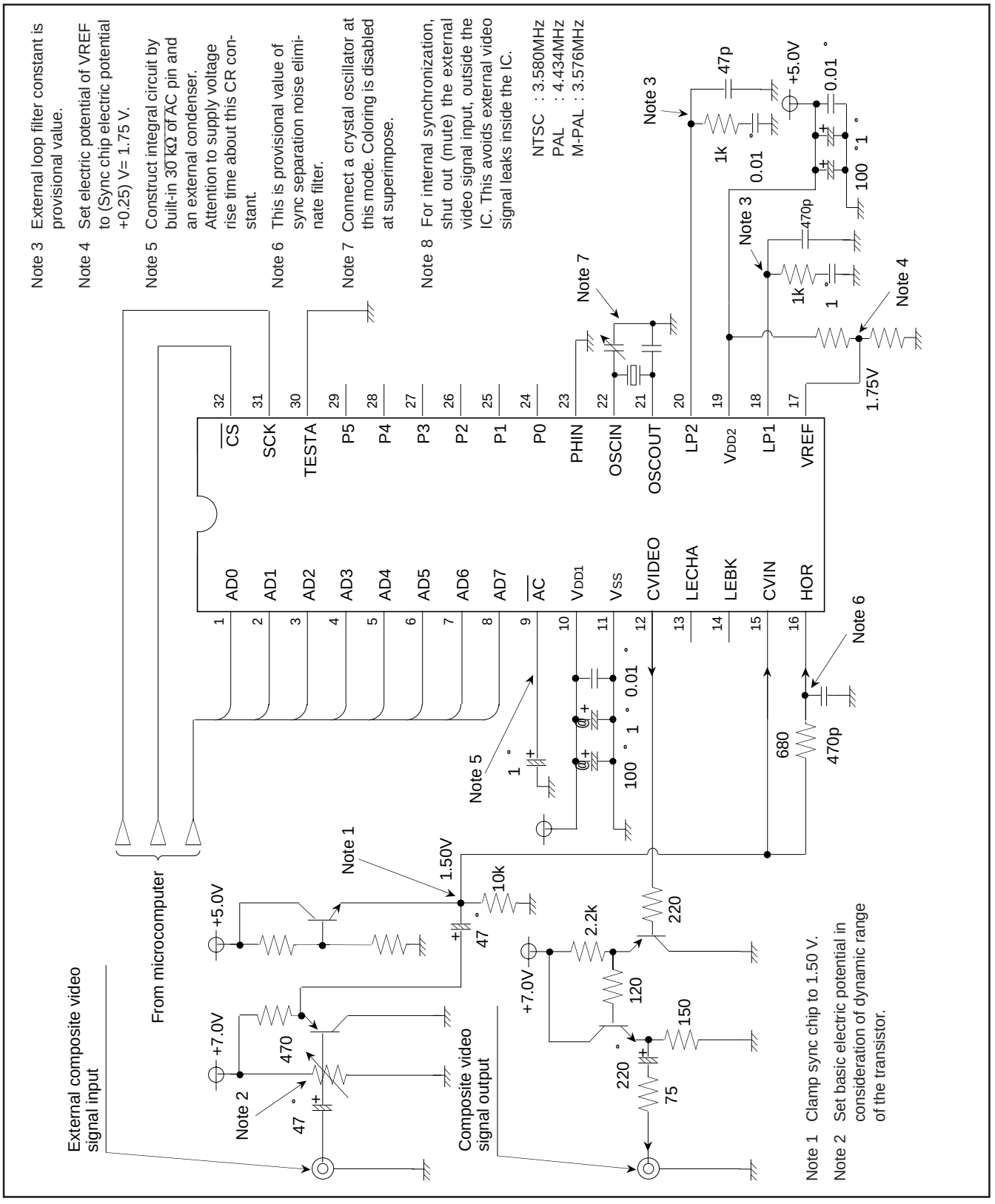


Fig.16 M35062-XXXSP example of peripheral circuit

TIMING REQUIREMENTS (T_a = – 20°C to + 70°C, V_{DD} = 5.00 ± 0.25V unless otherwise noted)

DATA INPUT

Symbol	Paramenter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W\ (SCK)}$	SCK width	200	—	—	ns
$t_{su\ (\overline{CS})}$	$\overline{CS}$ setup time	200	—	—	ns
$t_{h\ (\overline{CS})}$	$\overline{CS}$ hold time	2	—	—	µs
$t_{su\ (AD)}$	AD setup time	200	—	—	ns
$t_{h\ (AD)}$	AD hold time	200	—	—	ns
$t_{h\ (SCK)}$	1 word hold time	2	—	—	µs

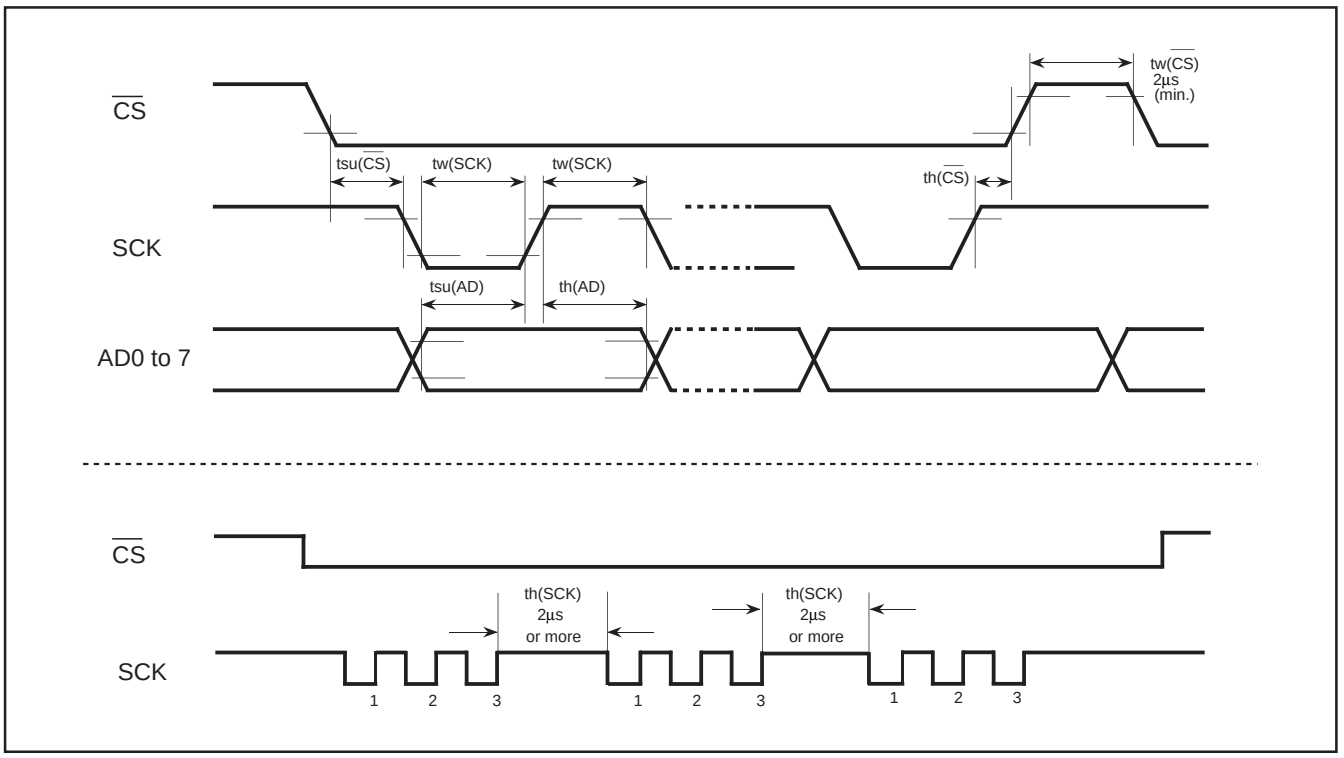


Fig. 17 Serial input timing requirements

ABSOLUTE MAXIMUM RATINGS (V_{DD} = 5.00V, T_a = – 20°C to +70°C unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD}	Supply voltage	With respect to V_{SS}.	– 0.3 to 6.0	V
V_I	Input voltage		V_{SS} – 0.3 < V_I < V_{DD} + 0.3	V
V_O	Output voltage		V_{SS} < V_O < V_{DD}	V
Pd	Power dissipation	T_a = 25°C	300	mW
Topr	Operating temperature		– 20 to 70	°C
Tstg	Storage temperature		– 40 to 125	°C

RECOMMENDED OPERATIONAL CONDITIONS (V_{DD} = 5.00 V, T_a = – 20°C to +70°C unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{DD}	Supply voltage	4.75	5.00	5.25	V
V_{IH}	"H" level input voltage $\overline{AC}$, $\overline{CS}$, SCK, AD0 to AD7	0.8 × V_{DD}	V_{DD}	V_{DD}	V
V_{IL}	"L" level input voltage $\overline{AC}$, $\overline{CS}$, SCK, AD0 to AD7	0	0	0.2 × V_{DD}	V
V_{CVIN}	Composite video input voltage CVIN	—	2 V_{P-P}	—	V
V_{OSCIN}	Input voltage OSCIN	0.3 V_{P-P}	—	4.0 V_{P-P}	V
fOSCIN	Oscillation frequency for synchronous signal (Duty 40 to 60%)	—	3.580 4.434 3.576	—	MHz

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{DD}	Supply voltage	T_a = – 20°C to +70°C	4.75	5.00	5.25	V
I_{DD}	Supply current	V_{DD} = 5.00 V	—	25	50	mA
V_{OH}	"H" level output voltage P0 to P5	V_{DD} = 4.75, I_{OH} = – 0.2 mA	3.75	—	—	V
V_{OL}	"L" level output voltage P0 to P5	V_{DD} = 4.75, I_{OL} = 0.2 mA	—	—	0.4	V
R_I	Pull-up resistance $\overline{AC}$	V_{DD} = 5.00 V	10	30	100	kΩ

VIDEO SIGNAL INPUT CONDITIONS (V_{DD} = 5.00 V, T_a = – 20°C to +70°C)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{IN-CU}	Composite video signal input clamp voltage	Sync-chip voltage	—	1.5	—	V

NOTE FOR SUPPLYING POWER

(1) Timing of power supplying to $\overline{AC}$ pin

The internal circuit of M35062-XXXSP is reset when the level of the auto clear input pin $\overline{AC}$ is "L".

This pin is hysteresis input with the pull-up resistor. The timing about power supplying of $\overline{AC}$ pin is shown in Figure 18.

After supplying the power (V_{DD} and V_{SS}) to M35062-XXXSP, the tw time must be reserved for 1 ms or more.

Before starting input from the microcomputer, the waiting time (ts) must be reserved for 200 ms after the supply voltage to the $\overline{AC}$ pin becomes $0.8 \times V_{DD}$ or more.

(2) Timing of power supplying to $V_{DD}1$ pin and $V_{DD}2$ pin

The power need to supply to $V_{DD}1$ and $V_{DD}2$ at a time, though it is separated perfectly between the $V_{DD}1$ as the digital line and the $V_{DD}2$ as the analog line.

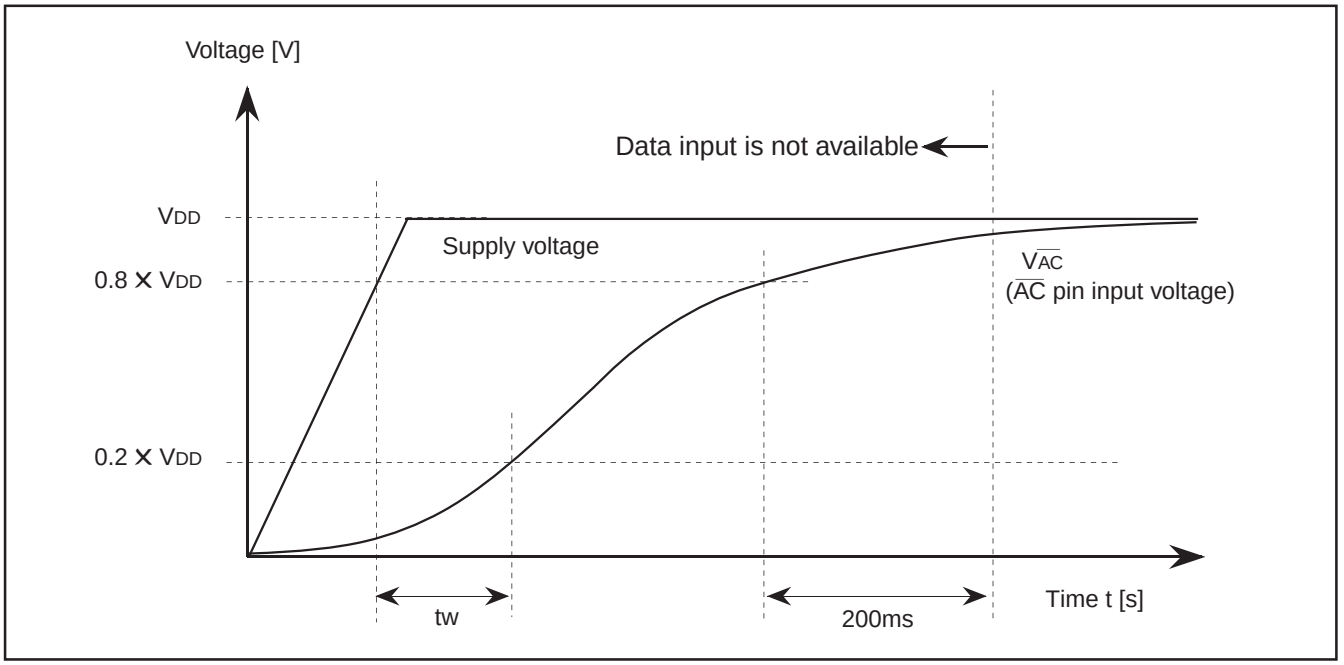


Fig. 18 Timing of power supplying to $\overline{AC}$ pin

PRECAUTION FOR USE

Notes on noise and latch-up

In order to avoid noise and latch-up, connect a bypass capacitor (≈ 0.1 ˚F) directly between the V_{DD1} pin and V_{SS} pin, and the V_{DD2} pin and V_{SS} pin using a heavy wire.

DATA REQUIRED FOR MASK ROM ORDERING

Please send the following data for mask orders.

(1) M35062-XXXSP mask ROM order confirmation form

(2) 32P4B mask specification form

(3) ROM data (EPROM 3 sets)

(4) Floppy disks containing the character font generating program +character data

STANDARD ROM TYPE : M35062-XXXSP

M35062-001SP is a standard ROM type of M35062-XXXSP.
Character patterns are fixed to the contents of Figures 19 and 20.

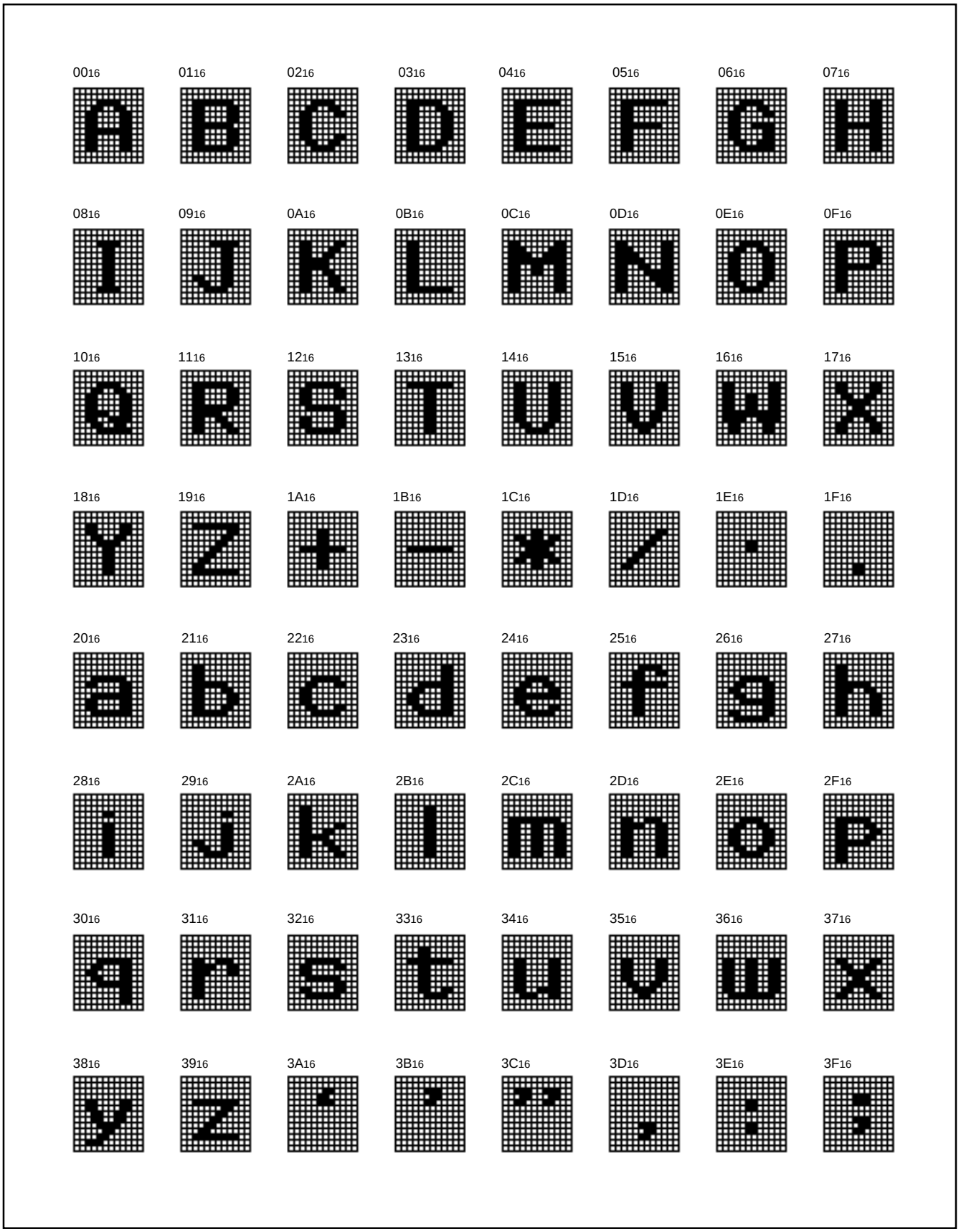


Fig. 19 M35062-001SP character patterns (1)

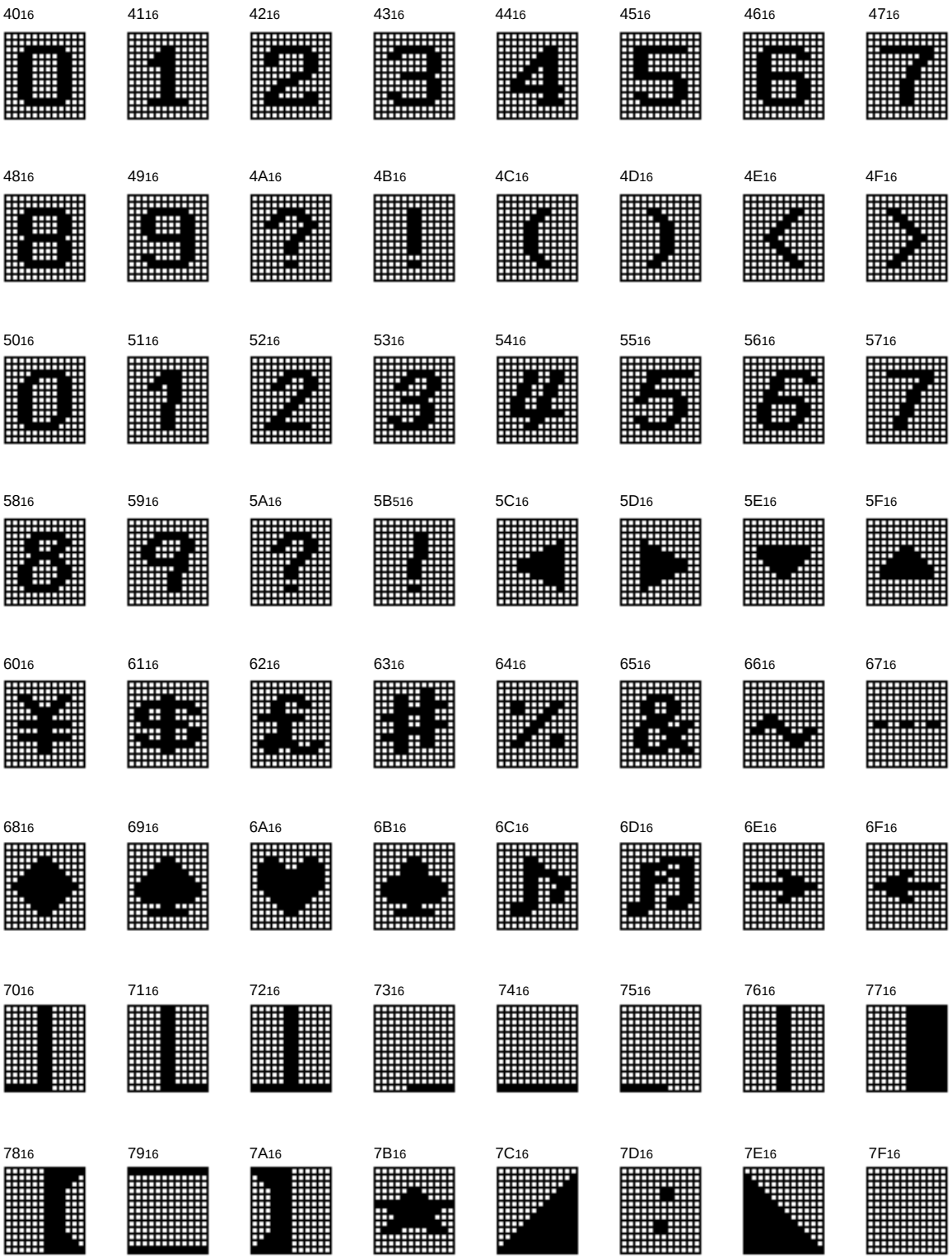


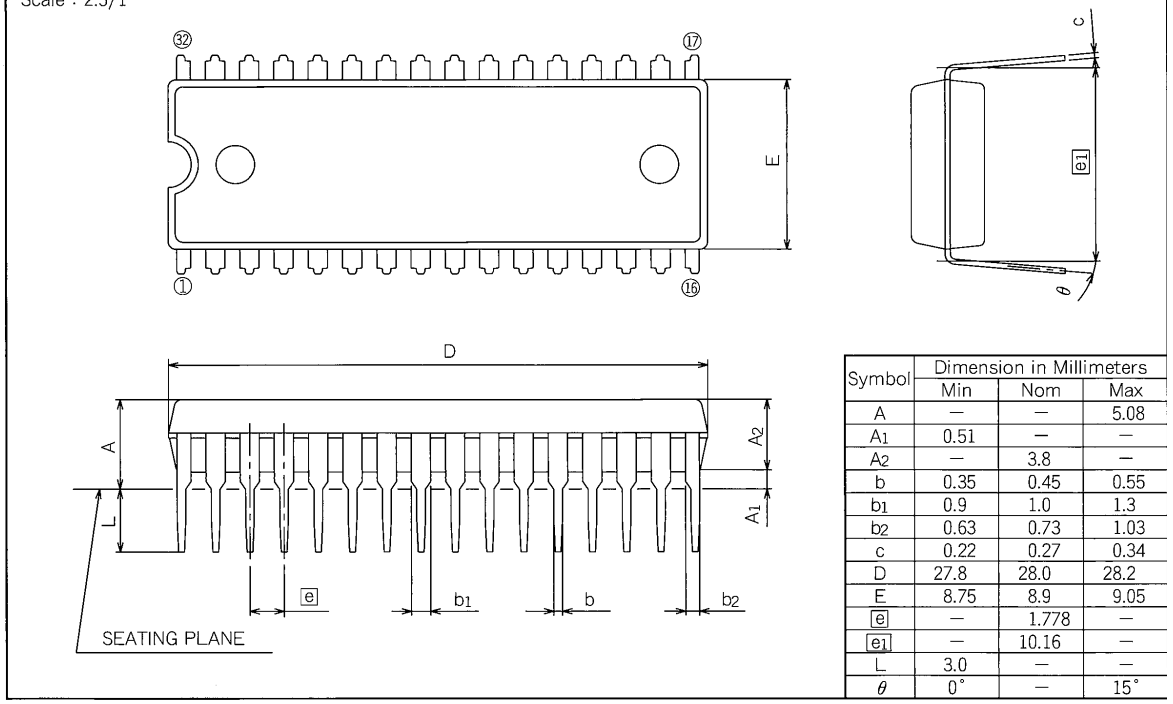
Fig. 20 M35062-001SP character patterns (2)

PACKAGE OUTLINE

32P4B Plastic 32pin 400mil SDIP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SDIP32-P-400-1.78	—	2.2	Alloy 42/Cu Alloy

Scale : 2.5/1



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	5.08
A_1	0.51	—	—
A_2	—	3.8	—
b	0.35	0.45	0.55
b_1	0.9	1.0	1.3
b_2	0.63	0.73	1.03
c	0.22	0.27	0.34
D	27.8	28.0	28.2
E	8.75	8.9	9.05
e	—	1.778	—
e_1	—	10.16	—
L	3.0	—	—
θ	0°	—	15°

M35062-XXXSP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

Renesas Technology Corp.
Nippon Bldg.,6-2,Otemachi 2-chome,Chiyoda-ku,Tokyo,100-0004 Japan

RENESAS
Renesas Technology Corp.

REVISION DESCRIPTION LIST	M35062-XXXSP DATA SHEET

Rev. No.	Revision Description	Rev. date
1.0	First Edition	980402
1.1	• Deletes some Japanese font and create pdf file (some pages) • P41 and P42 MARK SPECIFICATION FORM and PACKAGE OUTLINE are added	000725
1.2	Delete Mask ROM ORDER CONFIRMATION FORM and MASK SPECIFICATION FORM	000829