Ordering number : EN*A0906A

Preliminary

SANYO Semiconductors
DATA SHEET

LC074146LP — CMOS IC
Monaural CODEC+Audio I/F +Video driver IC

Overview

The LC074146LP is an IC that integrates a video driver with audio CODEC developed for digital still cameras and other portable equipment. Incorporating 16-bit A/D and D/A converters as well as a microphone amplifier and speaker driver that are necessary for audio recording and playback, the one-chip IC is ideal for use to create audio interfaces.

Features and Functions

■Audio Block

- ΔΣ method 16-bit monaural A/D and D/A converters
- Generates bias voltage (2.3V) for microphone
- Supports microphone amplifier differential inputs (0/+20/+26dB)
- Amplifier with automatic level control (ALC)(-14dB to +34dB) for recording system
- Programmable digital filter
- Digital volume with automatic level control (ALC) for playback system
  Supports zerocross detection and soft switching
- Line output
  Onchip MUTE and POP-noise suppression circuits
- Speaker driver
  Supports SV_{DD}=5V (piezoelectric speaker supported)
  BTL drive, rated output of 350mW at 8Ω, SV_{DD}=3V
  Idling current adjustable
  Supports BEEP input, volume level switchable
- Audio interfaces
  I^2S, Left-justified mode, Right-justified mode
- PLL
  Input: 12MHz, 13.5MHz, 24MHz, 27MHz
  Sampling frequency: 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
  PLL master mode/slave (EXT) mode
- Loopback: ADOUT to DAIN switch incorporated

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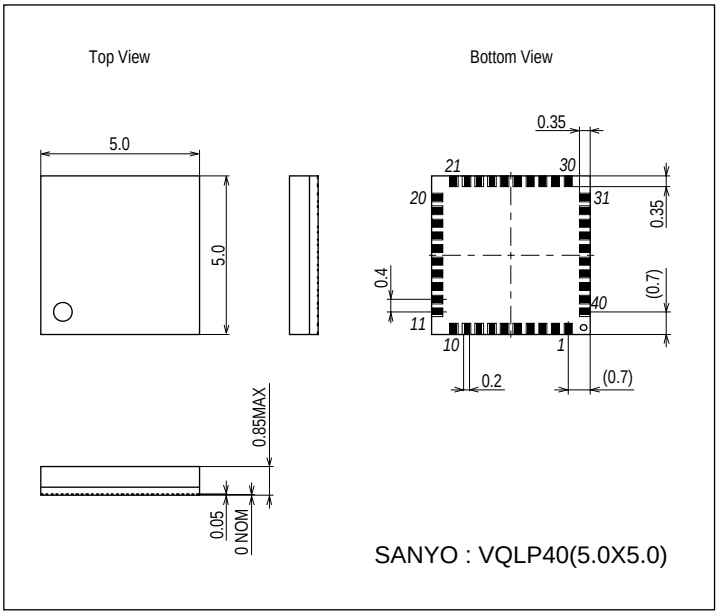
■Video Block

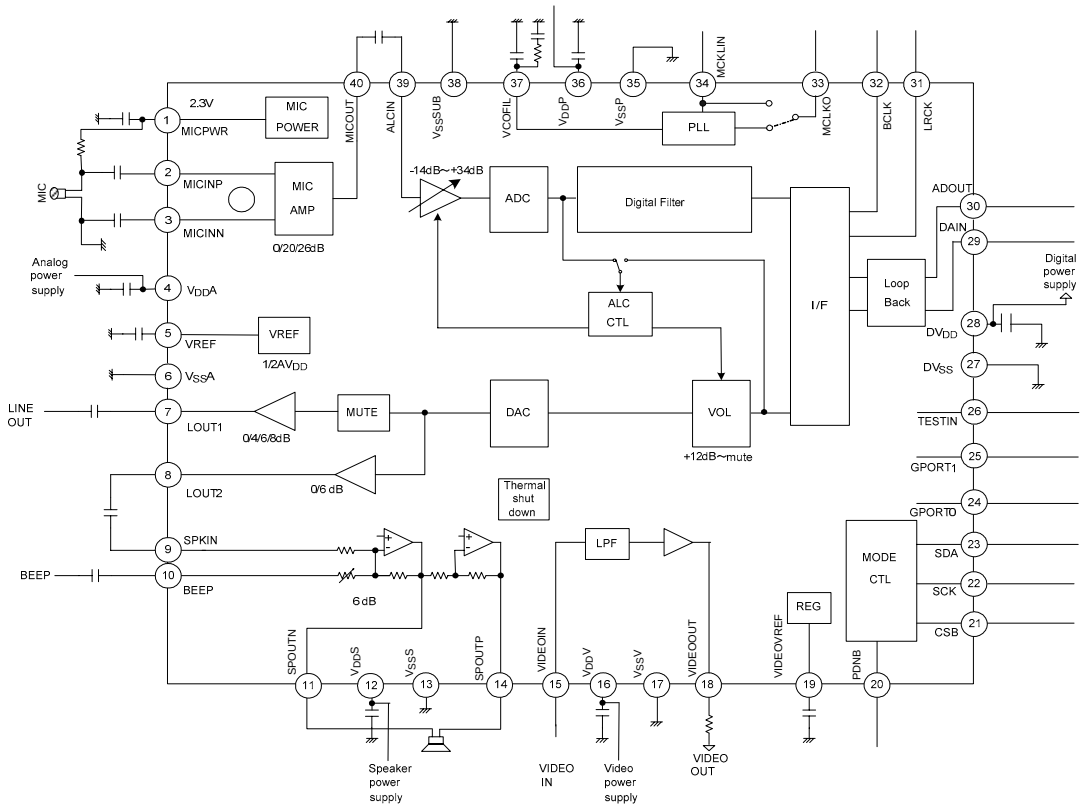
- DC direct coupling input/output
- Built-in 6th order low-pass filter (fc=7.5MHz)
- Amplifier gain selectable (6dB or 12dB)
- Drive capacity 75Ω, 1 system
- 3-line serial register control
- Supply voltage: 3.0V (2.7 to 3.6V)
- Operating ambient temperature: -15 to +80°C

Package Dimensions

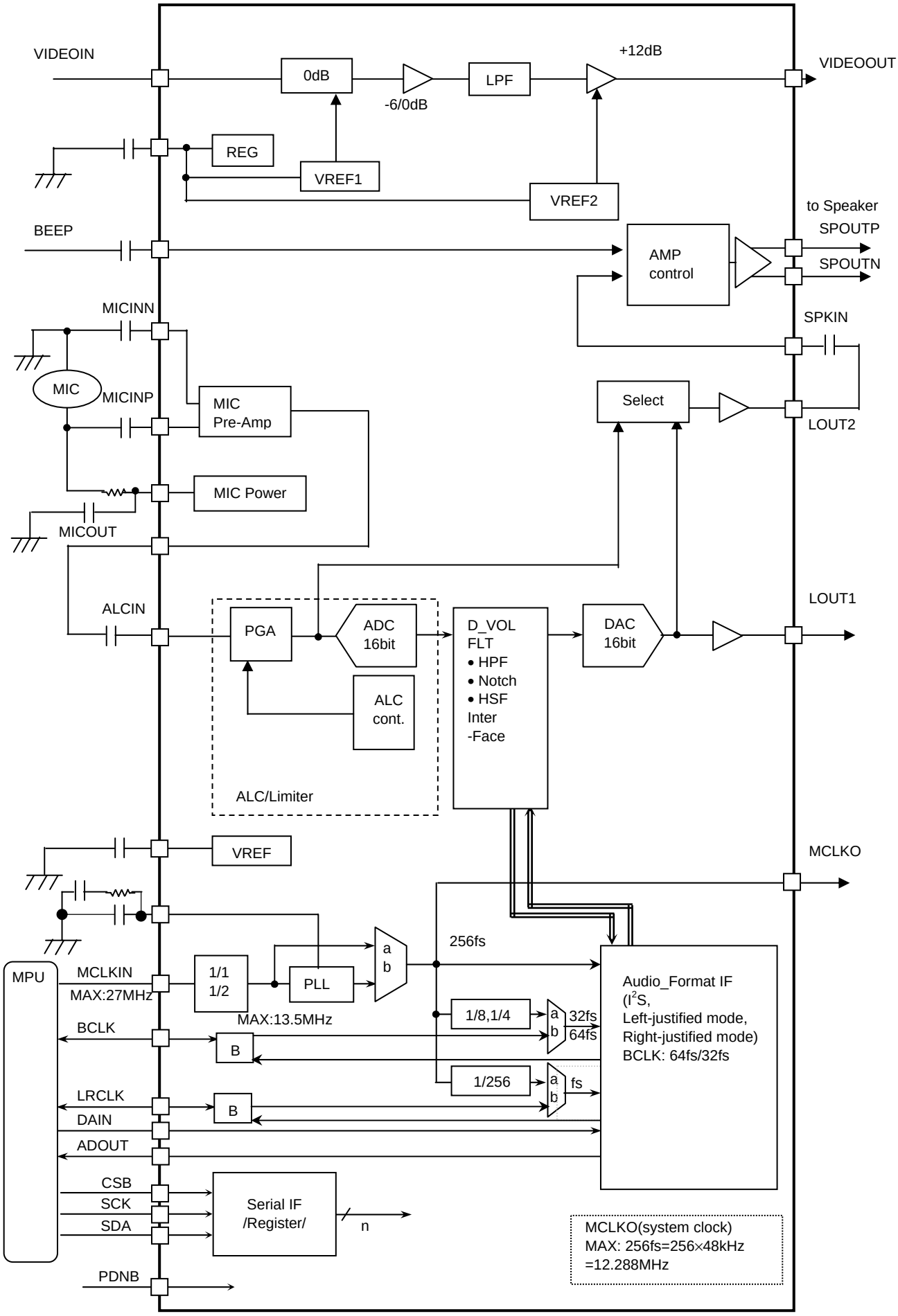
unit : mm (typ)
3302A



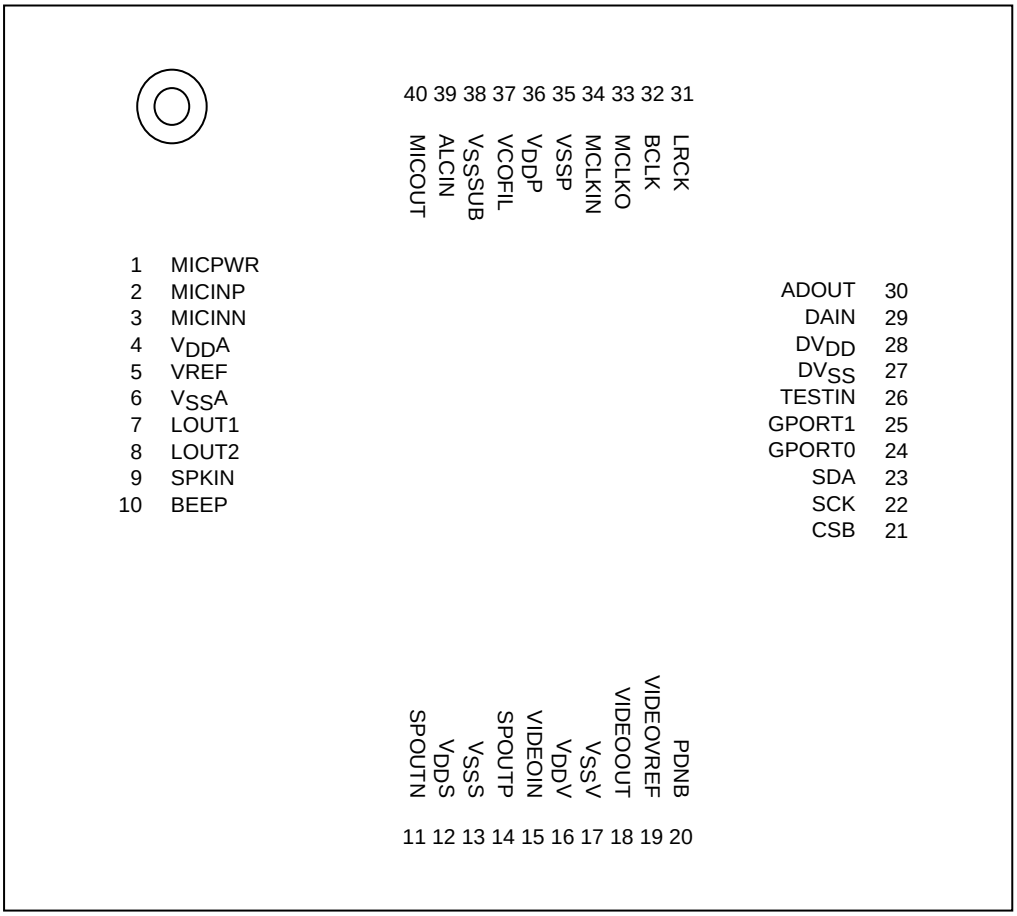
Sample Application Circuit



Circuit Block Diagram



Pin Assignment



Pin Description

(Note) I/O: I=> input, Is=> Schmitt input, O=> output, IOs=> input/output

PIN No	I/O	Symbol	Conditions
Digital system			
20	Is	PDNB	Reset (negative polarity)
21	I	CSB	Chip select (negative polarity) Microcontroller IF
22	Is	SCK	Serial clock Microcontroller IF
23	Is	SDA	Serial data input Microcontroller IF
24	IOs	GPORT0	For IC testing (open in normal operation)
25	IOs	GPORT1	For IC testing (open in normal operation)
26	Is	TESTIN	Test input (V_{SS} fixed in normal operation)
29	Is	DACIN	DAC serial data input
30	O	ADOUT	ADC serial data output
31	IOs	LRCK	LR clock input
32	IOs	BCLK	Bit clock input
33	O	MCLKO	Master clock output (Default: Set to Low, serial setting enables output/Add; 0Dh)
34	I	MCLKIN	Master clock input

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PIN No	I/O	Symbol	Conditions
Analog system			
11	O	SPOUTN	Speaker output (-)
14	O	SPOUTP	Speaker output (+)
15	I	VIDEOIN	Video signal input
18	O	VIDEOOUT	Video signal output
19	O	VIDEOVREF	Video VREF
37	O	VCOFIL	VCO filter pin
39	I	ALCIN	ALC amplifier input
40	O	MICOUT	Microphone amplifier output
1	O	MICPWR	Microphone power supply output (2.3V)
2	I	MICINP	Microphone amplifier input (+ side)
3	I	MICINN	Microphone amplifier input (- side)
5	O	VREF	3V analog power supply reference voltage output
7	O	LOUT1	Line output 1
8	O	LOUT2	Line output 2
9	I	SPKIN	Speaker amplifier input
10	I	BEEP	BEEP signal input, mixed to speaker amplifier
Power supply			
12	-	$V_{DD}S$	Speaker analog power supply
13	-	$V_{SS}S$	Speaker analog ground
16	-	$V_{DD}V$	Video driver analog power supply
17	-	$V_{SS}V$	Video driver ground
27	-	DV_{SS}	Digital ground (0V)
28	-	DV_{DD}	Digital power supply (3V)
35	-	$V_{SS}P$	PLL ground (0V)
36	-	$V_{DD}P$	PLL power supply (3V)
38	-	$V_{SS}SUB$	Subground (0V)
4	-	$V_{DD}A$	Analog block power supply (3V)
6	-	$V_{SS}A$	Analog block ground (0V)

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	unit
Maximum supply voltage (5V system)	$V_{DD}5$ max		-0.3 to 7.0	V
Maximum supply voltage (3V system)	$V_{DD}3$ max		-0.3 to 4.0	
Input voltage	V_{IN} max		-0.3 to 4.0	V
Output voltage	V_{OUT} max		-0.3 to 4.0	V
Input/output voltage	V_{IO} max		-0.3 to 4.0	V
Allowable operating voltage range	V_{RANGE}	Other than $V_{DD}S$	2.7 to 3.6	V
	$V_{DD}Srange$		2.7 to 5.5	
Allowable power dissipation	Pd max	* Ta=80°C	TBD	mW
Operating ambient temperature	Topr		-15 to +80	°C
Storage ambient temperature	Tstg		-55 to +125	°C

* Mounted on a specified board: 40mm×50mm×0.8mm, glass epoxy board 2S2P (4-layer board)

Recommended Operating Range at $V_{SS}V=DV_{SS}=V_{SS}P=V_{SS}A=V_{SS}SUB=0V$

Parameter	Symbol	Conditions	Specification			
			min	typ	max	unit
Supply voltage	DV_{DD}	DV_{DD} pin	2.7	3.0	3.6	V
	$V_{DD}ana$	$V_{DD}V$, $V_{DD}P$, $V_{DD}A$, pin	2.7	3.0	3.6	V
	$V_{DD}S$	$V_{DD}S$ pin	2.7	3.0/5.0	5.5	V
Inpupt high level voltage	V_{IH}	(*1)	$0.8*DV_{DD}$		DV_{DD}	V
Input low voltage level voltage	V_{IL}	(*1)	V_{SS}		$0.2*DV_{DD}$	V
Input clock frequency	fMCLK	MCLKIN pin			27	MHz
Input clock duty	DutyMCLK	MCLKIN pin	0.45	0.50	0.55	%

(*1) Applicable pins: PDNB, CSB, SCK, SDA, GPORT0, GPORT1, TESTIN, DAIN, LRCK, BCLK, MCLK
BCLK, LRLK (in input mode), GPORT1-0 (in input mode, only output mode during normal operation)

Electrical Characteristics at $Ta=25\pm2°C, V_{DD}ana=DV_{DD}=V_{DD}S=2.7$to $3.6V, V_{SS}V=DV_{SS}=V_{SS}P=V_{SS}A=V_{SS}SUB=0V$

Parameter	Symbol	Conditions	Specification			
			min	typ	max	unit
Input high level current	I_{IH}	$V_I=DV_{DD}$(*1)			+1	µA
Inputp low level current	I_{IL}	$V_I=DV_{SS}$(*1)	-1			µA
Output high level voltage	$V_{OH}1$	I_{OH}=-1mA(*2)	$0.8*DV_{DD}$			V
Output low level voltage	$V_{OL}1$	I_{OL}=1mA(*2)			$0.2*DV_{DD}$	V

(*1) Applicable pins: MCLKIN, TESTIN, PDNB, CSB, SCK, SDA, BCLK, LRCK (in input mode),
GPORT1-0 (in input mode, only output mode during normal operation)
(*2) Applicable pins: ADOUT, BCLK, LRCK (in output mode),
GPORT1-0 (in input mode, only output mode during normal operation)

Analog Characteristics at $Ta=+25°C, V_{DD}A=DV_{DD}=V_{DD}S=V_{DD}V=V_{DD}P=3.0V$, fs=48kHz

Parameter	Symbol	Conditions	Specification			
			min	typ	max	unit
Current drain						
REC time analog system	$I_{DD}RA1$	$V_{DD}A+V_{DD}P+V_{DD}S$, no input signal		TBD		mA
REC time digital system	$I_{DD}RD1$	DV_{DD}		TBD		mA
PB(LINE) time analog system	$I_{DD}PA2$	$V_{DD}A+V_{DD}P+V_{DD}S$, no input signal		TBD		mA
PB(LINE) time digital system	$I_{DD}PD2$	DV_{DD}		TBD		mA
PB(SPK) time analog system	$I_{DD}PA3$	$V_{DD}A+V_{DD}P+V_{DD}S$, no input signal		TBD		mA
PB(SPK) time digital system	$I_{DD}PD3$	DV_{DD}		TBD		mA
Video block 1	$I_{DD}A1$	$V_{DD}V$, no input signal		TBD		mA
Video block 2	$I_{DD}D1$	$V_{DD}V$, Video in=white50%		TBD		mA
Power down time current	$I_{DD}PD$	$V_{DD}A+V_{DD}S+V_{DD}V+DV_{DD}+V_{DD}P$, clock stopped			10	µA
MIC						
MIC amplifier gain	VGmic	MGAIN[1:0]=01 MGAIN[1:0]=10 MGAIN[1:0]=11		0 20 26		dB
MIC amplifier output THD+N	THDNmic	V_{IN}=-30dBV, MGAIN[1:0]=11		-80	-70	dB
MIC amplifier output noise voltage	VNOmic	MIC IN no signal, A-weighted, MGAIN[1:0]=11		-88		dBV
MIC bias output voltage	Vmicpwr	R_L=5kΩ		2.3		V
ALC						
Gain change	DGalc			1		dB
Gain control range	VGalc		-14		+34	dB
ADC ALCIN input, ALCOFF Gain=0dB						
Analog input voltage	Vinad	0dBFS, 1kHz		$0.6V_{DD}A$		Vpp
THD+N	THDNad	-1dBFS, 1kHz		80		dB
Dynamic range	DRad	-60dBFS, A-weighted		86		dB
S/N ratio	SNad	ALCIN no signal, A-weighted		86		dB

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Parameter	Symbol	Conditions	Specification			
			min	typ	max	unit
DAC						
Digital volume change	DGvol1	+12dB to -10dB		0.5		dB
	DGvol2	-11dB to -42dB		1		dB
	DGvol3	-44dB to -64dB		2		dB
LINE DAC→LINE Gain=0dB, DVOL=0dB						
Analog output voltage	Voutda	0dBFS, 1kHz		$0.6V_{DD}A$		Vp-p
THD+N	THDNda	0dBFS, 1kHz		85		dB
Dynamic range	DRda	-60dBFS, A-weighted		88		dB
S/N ratio	SNda	A-weighted		88		dB
SPK						
SPK amplifier gain	VGsp	BTL, R_L=8Ω		12		dB
SPK output distortion	HDsp	SPKIN=-9dBV		0.2	1	%
SPK output noise voltage	VNOsp	SPKIN no signal, R_L=8Ω		-86		dBV
SPK maximum rated output	VOMsp	R_L=8Ω, THD=3%		350		mW
BEEP gain	VGbp	BTL, R_L=8Ω BPVOL[1:0]=00 BPVOL[1:0]=01 BPVOL[1:0]=10 BPVOL[1:0]=11		-12 -15 -18 -21		dB
Video driver						
Video amplifier gain	VGvideo	VGAIN[1:0]=00, Video in=1Vp-p100% white VGAIN[1:0]=10, Video in=0.5Vp-p100% white		6 12		dB
Frequency characteristics	Fva	f=6MHz/100kHz f=20MHz/100kHz	-1	0 -45	+1	dB
Input impedance	Rvin		100	120		kΩ
Input sync-tip level	Vsync			0	50	mV

ADC Filter Characteristics (fs=48kHz)

Parameter	Conditions	Specification				Remarks
		min	typ	max	unit	
Resolution			16		Bit	
Passband	±0.04dB	0		19.6	kHz	
	±0.06dB	0		20.7	kHz	
	±0.09dB	0		21.8	kHz	0.4535fs
Stopband		24			kHz	0.5fs
Passband ripple	0to 20kHz		±0.09		dB	
Stopband attenuation		-60			dB	
Output data delay			40		1/fs	
HPF cutoff frequency	-3dB		0.94		Hz	1st order IIR high pass filter

DAC Filter Characteristics (fs=48kHz)

Parameter	Conditions	Specification				Remarks
		min	typ	max	unit	
Resolution			16		Bit	
Passband	Note 1	0		21.8	kHz	0.4535fs
Stopband		26.2			kHz	0.5465fs
Passband ripple			±0.002		dB	
Stopband attenuation		-80			dB	
Output data delay			31		1/fs	
HPF cutoff frequency	-3dB		0.94		Hz	1st order IIR high pass filter

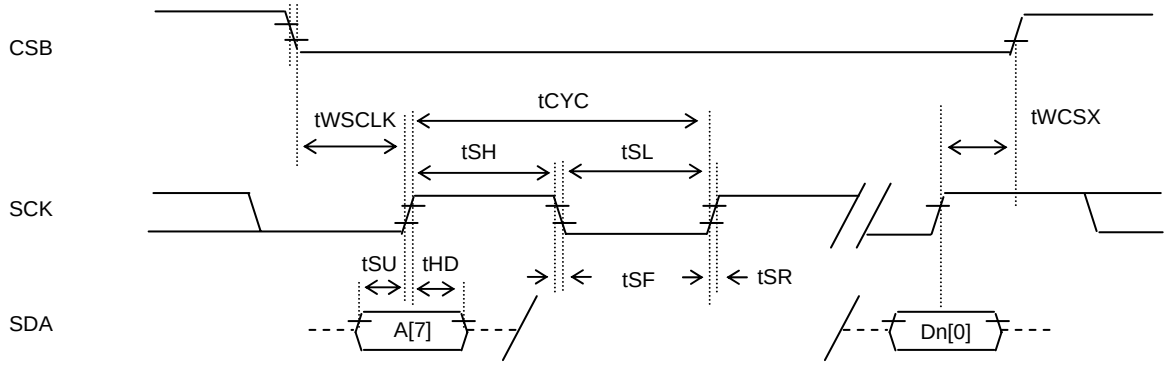
Switching Characteristics

Parameter	Symbol	Conditions	Specification			
			min	typ	max	unit
PLL						
CKIN frequency	fCKI	PLL used	12		27	MHz
		EXT input present	2.048		24.576	MHz
BCLK frequency	fBCK	FBCK=0		64fs		
		FBCK=1		32fs		
BCLK duty cycle	dtBK		45	50	55	%
LRCK frequency	fLR		8		48	kHz
LRCK duty cycle	dtLR		45	50	55	%
CLK transition time ↑	trCK	Rise time, CKIN/BCLK/LRCK inputs present			10	ns
CLK transition time ↓	tfCK	Fall time, CKIN/BCLK/LRCK inputs present			10	ns

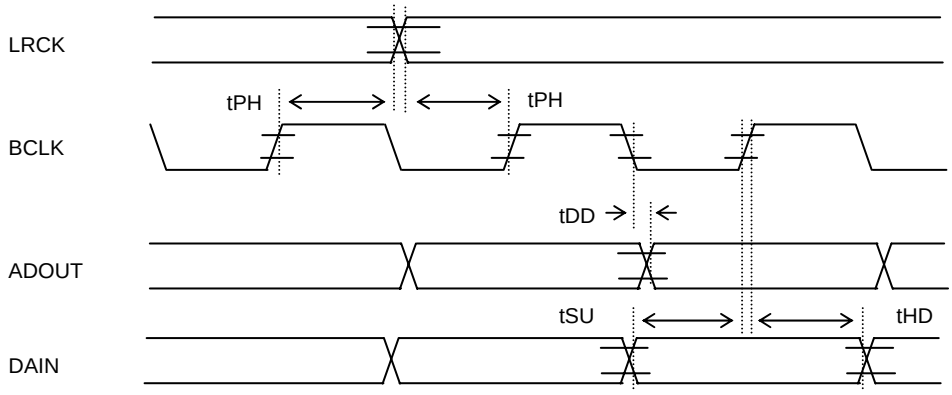
Parameter	Symbol	Specification			
		min	typ	max	unit
Microcontroller serial interface timing					
SCLK cycle time	tCYC	4T	8T		ns
SCLK High period	tSH	2T	4T		ns
SCLK Low period	tSL	2T	4T		ns
Data setup time	tSU	2T	4T		ns
Data hold time	tHD	2T	4T		ns
CSX rise to SCLK wait time	tWSCLK	0T	2T		ns
SCLK to CSX rise wait time	tWCSX	4T	6T		ns
Rise time	tSR			50	ns
Fall time	tSF			50	ns
Audio data timing					
Clock phase (Note 2)	tPH	75			ns
Clock phase (Note 3)	tPH		1/(128fs)		ns
Data delay time	tDD	0		75	ns
Data setup time	tSUA	TBD			ns
Data hold time	tHDA	TBD			ns

Note 1: T=1/fMCLK, fMCLK: Frequency of MCLKIN pin; example: when fMCLK=10MHz, T=100ns, 2T=200ns
Note 2: LRCK and BCLK are inputs in Slave mode.
The MCLK timing needs only to be synchronized with LRCK and BCLK and its phase is irrelevant.
Note 3: In master mode, LRCK and BCLK are output in master mode and fs is the sampling frequency.
Note 4: The load of output pin: 30pF.

Microcontroller Serial Interface Timing Diagram

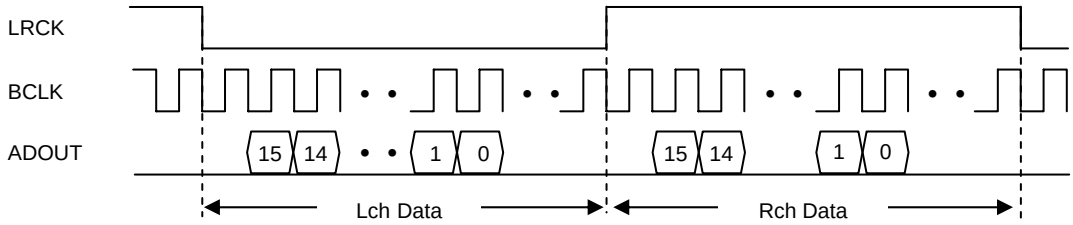


Audio Data Timing Diagram

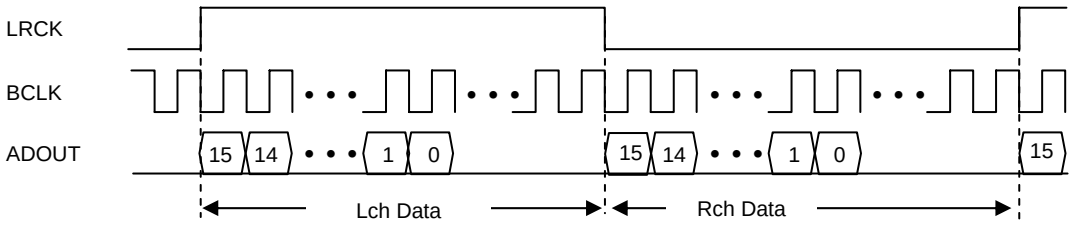


Audio Data Formats

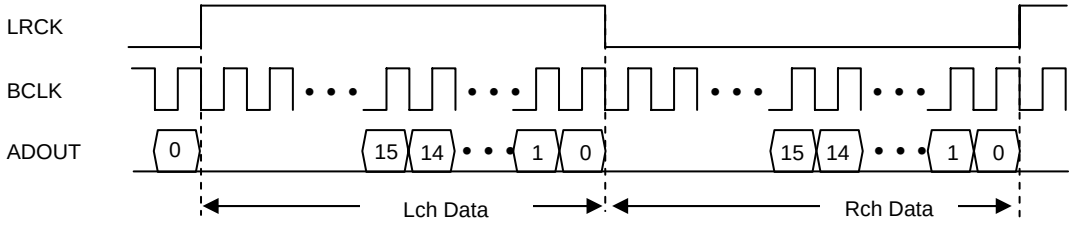
• I^2S mode



• Left-justified mode



• Right-justified mode

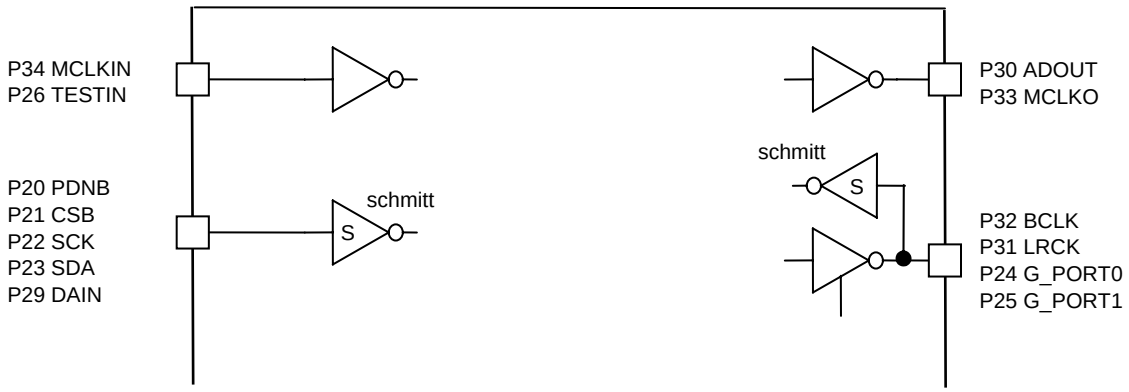


Pin Name	PIN No.	Slave Mode (PLL: OFF)	Master Mode (PLL: ON)
MCLKIN	34	Input	Input
MCLKO	33	Output (through)	Output (PLL=256fs)

Pin Name	PIN No.	Slave Mode	Master Mode
LRCK	31	Input	Input
BCLK	32	Output	Output

Pins' Internal Equivalent Circuits

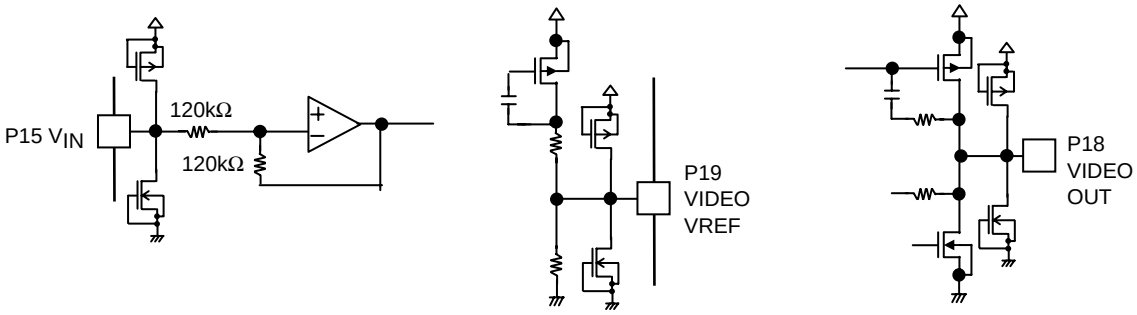
• Digital pins



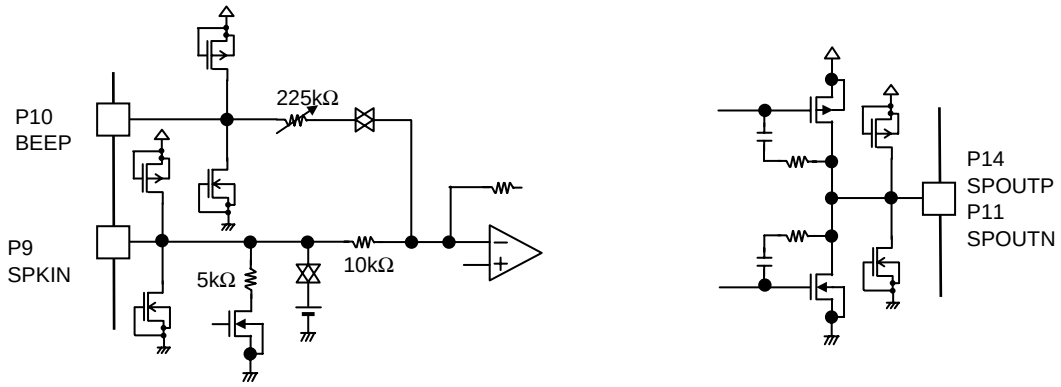
• Analog pins

Note: All resistance values are typical values.

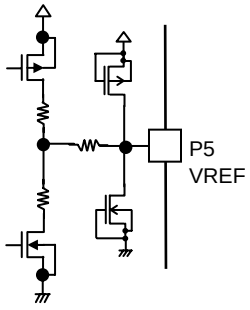
Video driver related pins



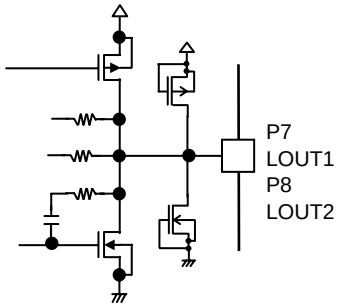
Speaker input/output pins



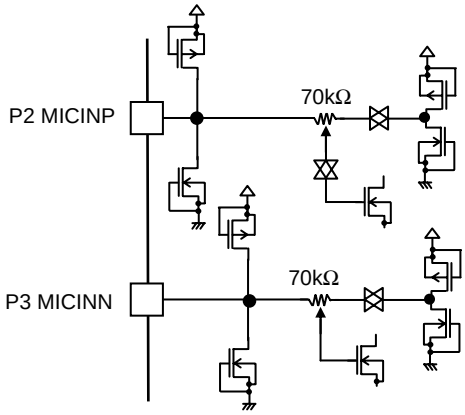
VREF



LINE_OUT



MIC input



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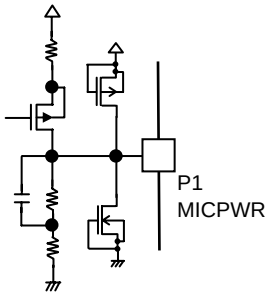
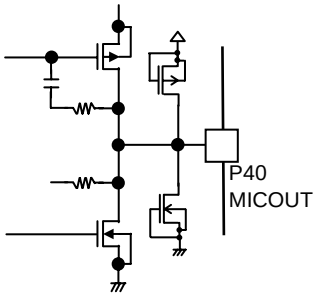
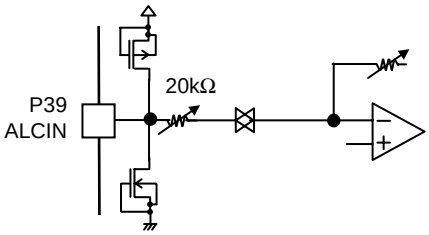
MIC power supply



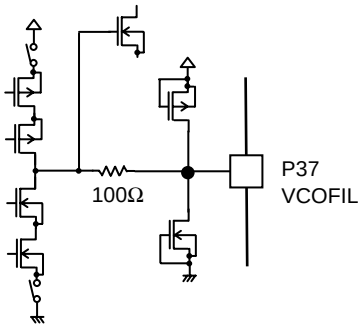
MIC output



ALC input



PLL detector



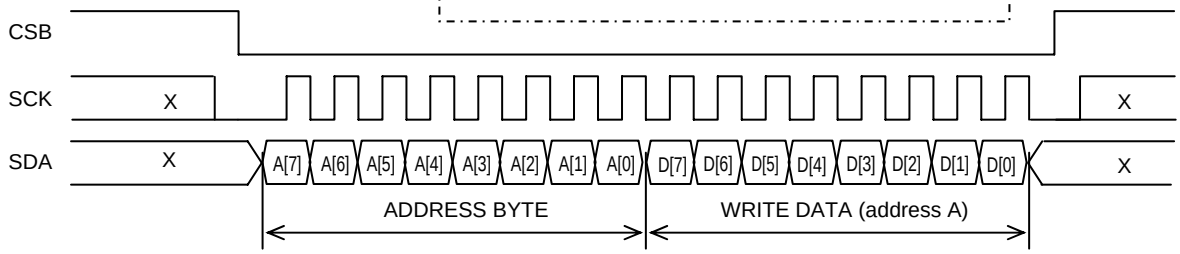
Microcontroller Serial Interface

The internal registers values are written by the serial interface consisting of the three CSB, SCK, and SDA lines. When the CSB pin is set low, the LC074146LP is switched into the mode that enables operation. The data is received on a byte basis with MSB first.

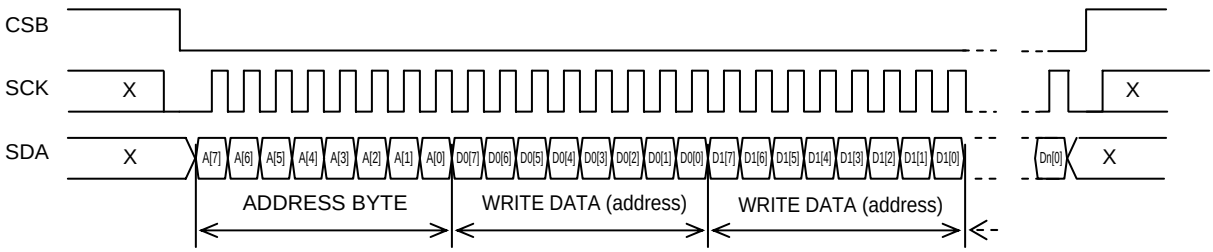
Continuous access (burst access) is also possible, and the addresses incremented by 1 are accessed in sequence with each byte following access to the register specified by the address byte. If the size of data exceeding the highest address (0E) is accessed in this process, the data concerned is treated as invalid. In other word, the address never wraps around to 00 (HEX).

Transferring data to one address

A[7:0] : Designated address
D[7:0] : Register data
X : Invalid



Transferring data to contiguous addresses



Register Table

ADRS (Address): displayed in hexadecimal notation,
Init (initial value): displayed in hexadecimal notation
Register bits indicated by "0" must be set to 0 and those indicated by "1" must be set to 1.
Registers indicated with a gray background are for IC testing and their initial values are fixed.
All registers (addresses: 00 to 25h) must be loaded with write data (including test registers).

Functions	ADRS [7:0]	Init	Register Data D[7:0]							
			7	6	5	4	3	2	1	0
PM1	00h	00h	MIC_PDX	MIC_PWR_PDX	PGA_PDX	ADC_PDX	DAC_PDX	SEL_PDX	LO_PDX	SP_PDX
PM2	01h	00h	SYNC_CLR	0	VREF_BIAS[1]	VREF_BIAS[0]	0	PLL_PDX	0	VD_PDX
MIC/SEL	02h	11h	0	0	MIC_GAIN[1]	MIC_GAIN[0]	0	SEL_GAIN	SEL_IN[1]	SEL_IN[0]
ALC1	03h	3Dh	ALC_VAL[2]	ALC_VAL[1]	ALC_VAL[0]	ALC_FA[1]	ALC_FA[0]	ALC_FR[2]	ALC_FR[1]	ALC_FR[0]
ALC2	04h	46h	ALC_FULLEN	ALC_ZCD	ALC_ZCDTM[1]	ALC_ZCDTM[0]	ALC_TLIM[1]	ALC_TLIM[0]	ALC_RWT[1]	ALC_RWT[0]
ALC3	05h	0Eh	0	0	ALC_VMAX[5]	ALC_VMAX[4]	ALC_VMAX[3]	ALC_VMAX[2]	ALC_VMAX[1]	ALC_VMAX[0]
ALC4	06h	0Eh	0	0	ALC_GAIN[5]	ALC_GAIN[4]	ALC_GAIN[3]	ALC_GAIN[2]	ALC_GAIN[1]	ALC_GAIN[0]
TEST0	07h	04h	0	0	0	0	0	1	0	0
CODEC1	08h	02h	HSF_ON	NOTCH_ON	WIND_CUT[1]	WIND_CUT[0]	AD_MUTE	FBCLK	REC_ALC	PB_ALC
CODEC2	09h	00h	0	0	0	ADF_MASTER	ADF_DAC_INV	ADF_ADC_INV	ADF_MODE[1]	ADF_MODE[0]
CODEC3	0Ah	00h	0	0	0	0	0	0	SEL_USE_DSP[1]	SEL_USE_DSP[0]
EVR1	0Bh	80h	EVR_MUTE	EVR_GAIN[6]	EVR_GAIN[5]	EVR_GAIN[4]	EVR_GAIN[3]	EVR_GAIN[2]	EVR_GAIN[1]	EVR_GAIN[0]
EVR2	0Ch	54h	0	EVR_ZCD	EVR_ZCDTM[1]	EVR_ZCDTM[0]	0	EVR_SOFTSW	EVR_SSC[1]	EVR_SSC[0]
MCLK	0Dh	00h	0	0	0	0	SEL_MCLKO[1]	SEL_MCLKO[0]	0	0
LO/SPK1	0Eh	E0h	LO_MUTE	LO_VREFSW	LO_GAIN[1]	LO_GAIN[0]	0	0	0	SP_OUT_EN
SPK2	0Fh	88h	SP_TSD_EN	SP_EXTBP_EN	SP_EXTBP_G[1]	SP_EXTBP_G[0]	SP_IDL[1]	SP_IDL[0]	SP_BIAS[1]	SP_BIAS[0]
VIDEO	10h	02h	0	0	VD_GAIN	VD_DCTL2[1]	VD_DCTL2[0]	VD_DCTL1[2]	VD_DCTL1[1]	VD_DCTL1[0]
FS	11h	08h	0	0	0	FS[4]	FS[3]	FS[2]	FS[1]	FS[0]
PLL	12h	00h	0	0	0	0	0	PLL_FCKI[2]	PLL_FCKI[1]	PLL_FCKI[0]
LPF_HSF	13h	00h	0	0	0	0	0	LPF_HSF[2]	LPF_HSF[1]	LPF_HSF[0]
Notch_1	14h	00h	A[15]	A[14]	A[13]	A[12]	A[11]	A[10]	A[9]	A[8]
Notch_1	15h	00h	A[7]	A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]
Notch_2	16h	00h	B[15]	B[14]	B[13]	B[12]	B[11]	B[10]	B[9]	B[8]
Notch_2	17h	00h	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
Notch_3	18h	00h	C[15]	C[14]	C[13]	C[12]	C[11]	C[10]	C[9]	C[8]
Notch_3	19h	00h	C[7]	C[6]	C[5]	C[4]	C[3]	C[2]	C[1]	C[0]
TEST1	1Ah	00h	0	0	0	0	0	0	0	0
TEST2	1Bh	01h	0	0	0	0	0	0	0	1
TEST3	1Ch	00h	0	0	0	0	0	0	0	0
TEST4	1Dh	02h	0	0	0	0	0	0	1	0
TEST5	1Eh	03h	0	0	0	0	0	0	1	1
TEST6	1Fh	18h	0	0	0	1	1	0	0	0
TEST7	20h	00h	0	0	0	0	0	0	0	0
TEST8	21h	B0h	1	0	1	1	0	0	0	0
TEST9	22h	21h	0	0	1	0	0	0	0	1
TEST10	23h	00h	0	0	0	0	0	0	0	0
TEST11	24h	00h	0	0	0	0	0	0	0	0
TEST12	25h	00h	0	0	0	0	0	0	0	0

Register Description

* Bold letters indicate initial settings.

ADRS	Bit	Name	Init	Description
00h	[7]	MIC_PDX	0b	MIC amplifier circuit, power down 1:OFF (normal operation) **0:ON**
	[6]	MIC_PWR_PDX	0b	MIC power circuit (MIC_PWR pin), power down 1:OFF (normal operation) **0:ON**
	[5]	PGA_PDX	0b	PGA circuit, power down 1:OFF (normal operation) **0:ON**
	[4]	ADC_PDX	0b	ADC circuit, power down 1:OFF (normal operation) **0:ON**
	[3]	DAC_PDX	0b	DAC circuit, power down 1:OFF (normal operation) **0:ON**
	[2]	SEL_PDX	0b	Selector (ALC or DAC) circuit, power down 1:OFF (normal operation) **0:ON**
	[1]	LO_PDX	0b	Line out circuit, power down 1:OFF (normal operation) **0:ON**
	[0]	SP_PDX	0b	Speaker amplifier circuit, power down 1:OFF (normal operation) **0:ON**
01h	[7]	SYNC_CLR	0b	Internal logic clear 1:ON **0:OFF** (normal operation)
	[5:4]	VREF_BIAS	00b	Reference voltage circuit (VREF pin) setting **00**: Power down 11: Normal operation 10: Quick rise to reference voltage 01:IREF ON/VREF OFF
	[2]	PLL_PDX	0b	PLL circuit, power down 1:OFF (normal operation) **0:ON**
	[0]	VD_PDX	0b	Video driver circuit, power down 1:OFF (normal operation) **0:ON**
02h	[5:4]	MIC_GAIN	01b	MIC amplifier circuit, gain setting 11: 26dB 10: 20dB **01: 0dB** 00: Inhibited
	[3]	SEL_GAIN	0b	Selector circuit, gain setting 1: 6dB **0: 0dB**
	[1:0]	SEL_IN	01b	Selector circuit, input setting 11, 00: Inhibited 10: ALC **01: DAC**
03h	[7:5]	ALC_VAL	001b	ALC circuit, ALC value (limiter level) setting
	[4:3]	ALC_FA	11b	ALC circuit, attack coefficient setting
	[2:0]	ALC_FR	101b	ALC circuit, recovery coefficient setting
04h	[7]	ALC_FULLEN	0b	ALC circuit, full scale detection mode setting 1: ON **0: OFF**
	[6]	ALC_ZCD	1b	ALC circuit, zerocross timing gain change **1: ON** 0: OFF
	[5:4]	ALC_ZCDTM	00b	ALC circuit, zerocross detection timeout time setting
	[3:2]	ALC_ATLIM	01b	ALC circuit, inter-zerocross attack limit setting
	[1:0]	ALC_RWT	10b	ALC circuit, setting wait time when recovery
05h	[5:0]	ALC_VMAX	0Eh	ALC circuit, PGA(REC)/digital volume (PB) maximum gain setting **0Eh: 0dB** 3Fh to 31h: Inhibited, 30h: +34dB to 00h: -14dB, 1dB step
06h	[5:0]	ALC_GAIN	0Eh	ALC circuit, manual mode PGA gain setting **0Eh: 0dB** 3Eh to 31h: Inhibited, 30h: +34dB to 00h: -14dB, 1dB step 3Fh: MUTE
08h	[7]	HSF_ON	0b	HSF filter (high frequency shelf filter) attenuation side only **0: OFF** 1: ON
	[6]	NOTCH_ON	0b	Notch filter **0: OFF** 1: ON
	[5:4]	WIND_CUT	00b	Wind cut function(HPF f, operation) 11: 400Hz 10: 300Hz 01: 200Hz **00: OFF**
	[3]	AD_MUTE	0b	ADOUT output mute **0: OFF** 1: ON
	[2]	FBCLK	0b	BCLK FS setting **0: 64fs** 1: 32fs
	[1:0]	REC_ALC PB_ALC	10b	ALC mode setting **10: REC_ALC**, **PB manual gain** 01: PB_**ALC**, REC manual gain 00/11: **ALCOFF**, REC, PB manual gain
09h	[4]	ADF_MASTER	0b	ADF circuit, BCLK, LRCLK setting 1: Master mode 0: Slave mode
	[3]	ADF_DAC_INV	0b	ADF circuit, DAC input data setting 1: Inverted **0**: Non-inverted
	[2]	ADF_ADC_INV	0b	ADF circuit, ADC output data setting 1: Inverted **0**: Non-inverted
	[1:0]	ADF_MODE	00b	ADF circuit, format setting 11, 10: Right-justified 01: Left justified **00: I^2S**
0Ah	[1:0]	SEL_USE_DSP	00b	ADC/DAC path select, 11: Inhibited 10: ADC DSP absent, DAC DSP present (ADC→ADOUT, DAIN→DSP→DAC) 01: Internal loopback (analog input/output) (ADC→DSP→ADOUT/DAC) **00: ADC DSP** present, **DAC DSP** absent (ADC→DSP→ADOUT, DAIN→DAC)
0Bh	[7]	EVR_MUTE	1b	EVR circuit, mute setting **1: ON** 0: OFF
	[6:0]	EVR_GAIN	00h	EVR circuit, gain setting **00h: MUTE** 3Fh: 0dB 57h: +12dB to 2Ch: -9.5dB, 0.5dB step 2Bh: -10dB to 0Ch: -41dB, 1.0dB step 0Bh: -42dB to 00h: -64dB, 2.0dB step

Continued on next page

Continued from precceding page.

ADRS	Bit	Name	Init	Description
0Ch	[6]	EVR_ZCD	1b	EVR circuit, gain change at zerocross timing **1: ON** 0: OFF
	[5:4]	EVR_ZCDTM	01b	EVR circuit, zerocross detection time timeout time setting
	[2]	EVR_SOFTSW	1b	EVR circuit, soft switch function **1: ON** 0: OFF
	[1:0]	EVR_SSC	00b	EVR circuit, Soft switch function time setting Value in parentheses ( ) denotes+12dB⇔MUTE time. 11, 10: Inhibited 01: 2.278ms/step(200ms) **00: 1.142ms/step(100ms)**
0Dh	[3:2]	SEL_MCLKO	00b	MCLK output select (MCLKO pin) **00: "L"**10: "H" 01, 11: MCLKIN or PLL [ADRS: 01h, D2 PLL_PDX: PLL prioritized output when set to 1]
0Eh	[7]	LO_MUTE	1b	Line out circuit, mute setting **1: ON** 0: OFF
	[6]	LO_VREFSW	1b	Line out circuit, connection to VREF setting **1: ON** 0: OFF
	[5:4]	LO_GAIN	10b	Line out circuit, gain select 11: 8dB **10: 6dB** 01: 4dB 00: 0dB
	[0]	SP_OUT_EN	0b	Speaker amplifier circuit, output enable 1: ON **0: OFF**
0Fh	[7]	SP_TSD_EN	1b	Speaker amplifier circuit, thermal shutdown enable **1: ON** 0: OFF
	[6]	SP_EXTBP_EN	0b	Speaker amplifier circuit, external input BEEP enable 1: ON **0: OFF**
	[5:4]	SP_EXTBP_G	00b	Speaker amplifier circuit, external input BEEP gain select 11: -21dB 10: -18dB 01: -15dB **00: -12dB**
	[3:2]	SP_IDL	10b	Speaker amplifier circuit, idling current setting 11: 2.0mA **10: 1.0mA** 01: 0.67mA 00: 0.5mA
	[1:0]	SP_BAIS	00b	Speaker amplifier circuit, bias voltage control setting 11: 0.833 10: 0.766 01: 0.666 **00: 0.5** (*V_{DD}ana)
10h	[5]	VD_GAIN	0b	VIDEO GAIN 1: +12dB **0: +6dB**
	[4:3]	VD_CTL2	00b	VIDEO input sync DC OFFSET setting (settings other than those listed below are disallowed.) **00**/01/10: **0mV**/62.5mV/125mV
	[2:0]	VD_CTL1	010b	VIDEO input sync DC OFFSET setting (settings other than those listed below are disallowed.) 001/**010**/011/100/101: -12.5mV/**0mV**/12.5mV/25mV/37.5mV
11h	[4:0]	FS	01000b	PLL FS setting (settings other than those listed below are disallowed.) **01000: 48 kHz/00111**: 44.1kHz/00110: 32 kHz/00101: 24kHz/ 00100: 22.05kHz/00011: 16kHz/00010: 12 kHz/00001: 11.025kHz/ 00000: 8kHz/10000: 7.86113kHz/ to 11010: 7.87113kHz (+0.001kHz Step)
12h	[2:0]	PLL_FCKI	000b	PLL input clock setting (settings other than those listed below are disallowed.) **000: 12MHz**, 001: 24MHz, 100: 13.5MHz, 101: 27MHz
13h	[2:0]	HPF_HSF	000b	Gain setting **000**/001/010/011/100/101/110/111: **0(OFF)**/-2/-4/-6/-7/-8/-10/-12dB
14h	[7:0]	Notch_1[15:8]	00h	Notch filter coefficient setting
15h	[7:0]	Notch_1[7:0]	00h	Notch filter coefficient setting
16h	[7:0]	Notch_2[15:8]	00h	Notch filter coefficient setting
17h	[7:0]	Notch_2[7:0]	00h	Notch filter coefficient setting
18h	[7:0]	Notch_3[15:8]	00h	Notch filter coefficient setting
19h	[7:0]	Notch_3[7:0]	00h	Notch filter coefficient setting

PM : Power Management
MIC : Microphone Amp
ALC : Automatic Level Control
ADC : AD Converter
DAC : DA Converter
EVR : Electronic Variable Resistor
ADF : Audio Data Format

PGA : Programmable Gain Amplifier
ADRS : Address
Init : Initial Value
Lch : Left Channel
Rch : Right Channel
2^n : 2^n (ex.2^10=1024)
Nh : N denotes a hexadecimal number.
Nb : N denotes a binary number.

Register Details

Reference voltage generator circuit

VREF_BIAS: Voltage Reference Bias

ADRS	Bit	Name	Init	Description
01h	[5:4]	VREF_BIAS	00b	Sets the reference voltage circuit (VREF pin). 11: Normal operation (standard resistor value) 10: Quick rise to reference voltage <*1> 01: Activates IREF bias, VREF OFF 00: Power down

<*1> The target voltage is reached quickly by connecting a low-resistance element in the "reference voltage generation circuit." During normal operation, a standard resistance is recommended in order to save power.

Logic synchronous clear

SYNC_CLR: Synchronus Clear

ADRS	Bit	Name	Init	Description
01h	[7]	SYNC_CLR	0b	Clears the internal logic circuit. 1: ON 0: OFF (normal operation) Used only when the operation of the logic circuit is unstable. Not used in normal operation.

Power down circuit

MIC_PDX : Mic Amp Power Down
MIC_PWR_PDX : Microphone Power Power Down
PGA_PDX : Pga Power Down
ADC_PDX : Adc Power Down
DAC_PDX : Dac Power Down
SEL_PDX : Selcter Power Down
LO_PDX : Line-Out buffer Power Down
SP_PDX : Speaker Amp Power Down
PLL_PDX : Pll Power Down
VD_REG_OFF : Video Driver Power Down
VD_PDX : Video Power Down

ADRS	Bit	Name	Init	Description
00h	[7]	MIC_PDX	0b	MIC amplifier circuit, power down function 1: OFF (normal operation) 0: ON
	[6]	MIC_PWR_PDX	0b	MIC power supply circuit (MIC_Power pin), Power down function 1: OFF (normal operation) 0: ON
	[5]	PGA_PDX	0b	PGA circuit, power down function 1: OFF (normal operation) 0: ON
	[4]	ADC_PDX	0b	ADC circuit, power down function 1: OFF (normal operation) 0: ON
	[3]	DAC_PDX	0b	DAC circuit, power down function 1: OFF (normal operation) 0: ON
	[2]	SEL_PDX	0b	Selector (ALC or DAC) circuit, Power down 1: OFF (normal operation) 0: ON
	[1]	LO_PDX	0b	Line out circuit, power down function 1: OFF (normal operation) 0: ON
	[0]	SP_PDX	0b	Speaker amplifier circuit, power down function 1: OFF (normal operation) 0: ON
01h	[2]	PLL_PDX	0b	PLL circuit, power down function 1: OFF (normal operation) 0: ON
	[0]	VD_PDX	0b	Video driver circuit, power down function 1: OFF (normal operation) 0: ON

In order to power save a relevant circuit that is not to be used, activate the power down mode.

Microphone circuit

MIC_GAIN: Microphone Amp Gain

ADRS	Bit	Name	Init	Description
02h	[5:4]	MIC_GAIN	01b	Set the gain of the MIC amplifier circuit. 11: 26dB 10: 20dB 01: 0dB 00: Inhibited

Recording System ALC Circuit Setting

ALC_VAL : Alc Value
ALC_FA : Alc Factor Attack
ALC_FR : Alc Factor Recovery
ALC_FULLEN : Alc Full Scale Detect Enable
ALC_ZCD : Alc Zero Cross Detect
ALC_ZCDTM : Alc Zero Cross Detect Time Out
ALC_ATLIM : Alc Attack Limit
ALC_RWT : Alc Recovery Waiting Time
ALC_VMAX : Value Max
ALC_GAIN : Pga Gain at Manual Mode
ALC_MODE : Alc_Mode

<table>
<tr><th>ADRS</th><th>Bit</th><th>Name</th><th>Init</th><th>Description</th></tr>
<tr><td rowspan="20">03h</td><td>[7: 5]</td><td>ALC_VAL</td><td>001b</td><td>Set the ALC limiter level of the ALC circuit.
000: -3dBFS 001: -4dBFS 010: -5dBFS 011: -6dBFS
100: -7dBFS 101: -8dBFS 110: -9dBFS 111: -10dBFS</td></tr>
<tr><td rowspan="5">[4: 3]</td><td rowspan="5">ALC_FA</td><td rowspan="5">11b</td><td><table><tr><th>FA[1:0]</th><th>1dB attenuation time</th><th>fs=8kHz</th><th>fs=48kHz</th><th>@fs</th></tr><tr><td>00</td><td>1/fs</td><td>125µs</td><td>20.83µs</td><td>-1dB</td></tr><tr><td>01</td><td>2/fs</td><td>250µs</td><td>41.67µs</td><td>-0.5dB</td></tr><tr><td>10</td><td>4/fs</td><td>500µs</td><td>83.33µs</td><td>-0.25dB</td></tr><tr><td>11</td><td>8/fs</td><td>1ms</td><td>166.7µs</td><td>-0.125dB</td></tr></table></td></tr>
<tr><td rowspan="10">[2:0]</td><td rowspan="10">ALC_FR</td><td rowspan="10">101b</td><td><table><tr><th>FR[2:0]</th><th>1dB boost time</th><th>fs=8kHz</th><th>fs=48kHz</th><th>@fs</th></tr><tr><td>000</td><td>128/fs</td><td>16ms</td><td>2.67ms</td><td>-2^{-7}dB</td></tr><tr><td>001</td><td>256/fs</td><td>32ms</td><td>5.33ms</td><td>-2^{-8}dB</td></tr><tr><td>010</td><td>512/fs</td><td>64ms</td><td>10.67ms</td><td>-2^{-9}dB</td></tr><tr><td>011</td><td>1024/fs</td><td>128ms</td><td>21.33ms</td><td>-2^{-10}dB</td></tr><tr><td>100</td><td>2048/fs</td><td>256ms</td><td>42.67ms</td><td>-2^{-11}dB</td></tr><tr><td>101</td><td>4096/fs</td><td>512ms</td><td>85.33ms</td><td>-2^{-12}dB</td></tr><tr><td>110</td><td>8192/fs</td><td>1024ms</td><td>170.7ms</td><td>-2^{-13}dB</td></tr><tr><td>111</td><td>16384/fs</td><td>2048ms</td><td>341.3ms</td><td>-2^{-14}dB</td></tr></table></td></tr>
<tr><td rowspan="20">04h</td><td>[7]</td><td>ALC_FULLEN</td><td>0b</td><td>Sets the full scale detection mode of the ALC circuit.
1: Performs attack operation regardless of the ALCZCD setting when a full scale is detected.
0: Normal operation</td></tr>
<tr><td>[6]</td><td>ALC_ZCD</td><td>1b</td><td>Controls the gain change operation of the ALC circuit at zerocross timing.
1: Changes the gain at zerocross timing.
0: Changes the gain without waiting for a zerocross timing.</td></tr>
<tr><td>[5:4]</td><td>ALC_ZCDTM</td><td>00b</td><td>Set the zerocross detection timeout time of the ALC circuit.
11: 8192/fs 10: 4096/fs 01: 2048/fs 00: 1024/fs
Valid when [ALC_ZCD]=1.</td></tr>
<tr><td rowspan="8">[3: 2]</td><td rowspan="8">ALC_ATLIM</td><td rowspan="8">01b</td><td>Set the limit number of attack operation of the ALC circuit during the zerocross interval.<table><tr><th></th><th></th><th colspan="4">Limit attenuation</th></tr><tr><th>ATLIM[1:0]</th><th>Number</th><th>FA=00</th><th>FA=01</th><th>FA=10</th><th>FA=11</th></tr><tr><td>00</td><td>2</td><td>2dB</td><td>1dB</td><td>0.5dB</td><td>0.25dB</td></tr><tr><td>01</td><td>4</td><td>4dB</td><td>2dB</td><td>1dB</td><td>0.5dB</td></tr><tr><td>10</td><td>8</td><td>8dB</td><td>4dB</td><td>2dB</td><td>1dB</td></tr><tr><td>11</td><td>16</td><td>16dB</td><td>8dB</td><td>4dB</td><td>2dB</td></tr></table></td></tr>
<tr><td>Valid when [ALC_ZCD]=1.</td></tr>
<tr><td rowspan="6">[1:0]</td><td rowspan="6">ALC_RWT</td><td rowspan="6">10b</td><td>Set the recovery operation wait time of the ALC circuit<table><tr><th>RWT[1:0]</th><th>Wait time</th><th>fs=8kHz</th><th>fs=48kHz</th></tr><tr><td>00</td><td>256/fs</td><td>32ms</td><td>5.33ms</td></tr><tr><td>01</td><td>512/fs</td><td>64ms</td><td>10.67ms</td></tr><tr><td>10</td><td>1024/fs</td><td>128ms</td><td>21.33ms</td></tr><tr><td>11</td><td>2048/fs</td><td>256ms</td><td>42.67ms</td></tr></table></td></tr>
</table>

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ADRS	Bit	Name	Init	Description
05h	[5:0]	ALC_VMAX	0Eh	Set the maximum PGA gain of the ALC circuit (Init value = 0Eh: 0dB). 3Fh to 31h: Inhibited 30h: +34dB 2Fh: +33dB : : <== 1dB increment 01h: -13dB 00h: -14dB
06h	[5:0]	ALC_GAIN	0Eh	Set the manual mode PGA gain of the ALC circuit (Init value = 0Eh: 0dB). 3Fh: MUTE 3Eh to 31h: Inhibited 30h: +34dB 2Fh: +33dB : : <== 1dB increment 01h: -13dB 00h: -4dB
08h	[1:0]	REC_ALC PB_ALC	10h	Set the ALC mode. 10: REC ALC, PB manual gain setting 01: PB ALC, REC manual gain setting 00/11: ALC OFF, REC, PB manual gain setting

See the section on "Description of ALC Operation."

ALC Circuit Gain Setting Table ALC_VMAX[5:0]/ALC_GAIN[5:0]

[5:0]	GAIN	[5:0]	GAIN	[5:0]	GAIN	[5:0]	GAIN	[5:0]	GAIN
00H	-14dB	0AH	-4dB	14H	6dB	1EH	16dB	28H	26dB
01H	-13dB	0BH	-3dB	15H	7dB	1FH	17dB	29H	27dB
02H	-12dB	0CH	-2dB	16H	8dB	20H	18dB	2AH	28dB
03H	-11dB	0DH	-1dB	17H	9dB	21H	19dB	2BH	29dB
04H	-10dB	0EH	0dB	18H	10dB	22H	20dB	2CH	30dB
05H	-9dB	0FH	1dB	19H	11dB	23H	21dB	2DH	31dB
06H	-8dB	10H	2dB	1AH	12dB	24H	22dB	2EH	32dB
07H	-7dB	11H	3dB	1BH	13dB	25H	23dB	2FH	33dB
08H	-6dB	12H	4dB	1CH	14dB	26H	24dB	30H	34dB
09H	-5dB	13H	5dB	1DH	15dB	27H	25dB		

Digital EVR Circuit Setting

EVR_MUTE : Evr Mute
EVR_GAIN : Evr Gain
EVR_ZCD : Evr Zero Cross Detect
EVR_ZCDTM : Evr Zero Cross Detect Time Out
EVR_SOFTSW : Evr Soft Switch
EVR_SSC : Evr Soft Switch Time Control

ADRS	Bit	Name	Init	Description
0Bh	[7]	EVR_MUTE	1b	Controls the mute function of the EVR (digital) circuit. 1: ON 0: OFF
	[6:0]	EVR_GAIN	00h	Set the gain of the EVR (digital) circuit. 3Fh: 0dB 57h: +12dB to 2Ch: -9.5dB/0.5dB step 2Bh: -10dB to 0Ch: -41dB/1.0dB step 0Bh: -42dB to 00h: -64dB/2.0dB step
0Ch	[6]	EVR_ZCD	1b	Controls the gain change operation of the EVR (digital) circuit at zerocross timing. 1: Changes the gain at the zerocross timing. 0: Changes the gain without waiting for a zerocross timing.
	[5:4]	EVR_ZCDTM	01b	Set the zerocross detection timeout time of the EVR (digital) circuit. 11: 8192/fs 10: 4096/fs 01: 2048/fs 00: 1024/fs Valid when [ALC_ZCD]=1
	[2]	EVR_SOFTSW	1b	Controls the soft switch function of the EVR (digital) circuit. 1: ON 0: OFF
	[1:0]	EVR_SSC	00b	Set the time of the soft switch function of the EVR (digital) circuit (dos not depend on fs). 11, 10: Inhibited 01: 2.278ms/step, (200ms: When +12dB⇔MUTE) 00: 1.142ms/step, (100ms: When +12dB⇔MUTE)

Digital EVR Circuit Gain Setting Table EVR_GAIN [6:0]

[6:0]	GAIN	[6:0]	GAIN	[6:0]	GAIN	[6:0]	GAIN	[6:0]	GAIN
00H	-64dB	12H	-35dB	24H	-17dB	36H	-4.5dB	48H	+4.5dB
01H	-62dB	13H	-34dB	25H	-16dB	37H	-4dB	49H	+5dB
02H	-60dB	14H	-33dB	26H	-15dB	38H	-3.5dB	4AH	+5.5dB
03H	-58dB	15H	-32dB	27H	-14dB	39H	-3dB	4BH	+6dB
04H	-56dB	16H	-31dB	28H	-13dB	3AH	-2.5dB	4CH	+6.5dB
05H	-54dB	17H	-30dB	29H	-12dB	3BH	-2dB	4DH	+7dB
06H	-52dB	18H	-29dB	2AH	-11dB	3CH	-1.5dB	4EH	+7.5dB
07H	-50dB	19H	-28dB	2BH	-10dB	3DH	-1dB	4FH	+8dB
08H	-48dB	1AH	-27dB	2CH	-9.5dB	3EH	-0.5dB	50H	+8.5dB
09H	-46dB	1BH	-26dB	2DH	-9dB	3FH	+0dB	51H	+9dB
0AH	-44dB	1CH	-25dB	2EH	-8.5dB	40H	+0.5dB	52H	+9.5dB
0BH	-42dB	1DH	-24dB	2FH	-8dB	41H	+1dB	53H	+10dB
0CH	-41dB	1EH	-23dB	30H	-7.5dB	42H	+1.5dB	54H	+10.5dB
0DH	-40dB	1FH	-22dB	31H	-7dB	43H	+2dB	55H	+11dB
0EH	-39dB	20H	-21dB	32H	-6.5dB	44H	+2.5dB	56H	+11.5dB
0FH	-38dB	21H	-20dB	33H	-6dB	45H	+3dB	57H	+12dB
10H	-37dB	22H	-19dB	34H	-5.5dB	46H	+3.5dB		
11H	-36dB	23H	-18dB	35H	-5dB	47H	+4dB		

Audio Data Formats

FBCLK : Audio Data Format BCLK
ADF_MASTER : Audio Data Format Master Mode
MCLK_DIV : Master Clock Divide
ADF_DAC_INV : Audio Data Format Dac Data Invert
ADF_ADC_INV : Audio Data Format Adc Data Invert
ADF_MODE : Audio Data Format Mode

ADRS	Bit	Name	Init	Description
08h	[2]	FBCLK	0b	Sets the BCLK frequency of the ADF circuit. 1: 32fs 0: 64fs
09h	[4]	ADF_MASTER	0b	ADF circuit 1: Master mode, BCLK and LRCLK pins are set for output. 0: Slave mode, BCLK and LRCLK pins are set for input.
	[3]	ADF_DAC_INV	0b	Sets the DAC input data of the ADF circuit. 1: Inverted 0: Non-inverted
	[2]	ADF_ADC_INV	0b	Sets the ADC output data of the ADF circuit. 1: Inverted 0: Non-inverted
	[1:0]	ADF_MODE	00b	Define the data format of the ADF circuit. 11, 10: Right justification 01: Left justification 00: I^2S

See the section on "Audio Data Formats."

DSP Related Settings

HSF_ON : High Frequency Shelf Filter ON
NOTCH_ON : Notch Filter ON
WIND_CUT : Wind_Cut Filter
NOTCH_1 : Notch Factor 1
NOTCH_2 : Notch Factor 2
NOTCH_3 : Notch Factor 3

ADRS	Bit	Name	Init	Description
08h	[7]	HSF_ON	0b	HSF circuit attenuation side only 1: ON 0: OFF
	[6]	NOTCH_ON	0b	Sets the notch filter. 1: ON 0: OFF
	[5:4]	WIND_CUT	00b	WIND_CUT function (HPF fc setting) 11: 400Hz 10: 300Hz 01: 200Hz 00: OFF
13h	[2:0]	HPF_HSF	000b	Set the HSF gain (gain at the 1/2fs point). 000: 0dB/001: -2dB/010: -4dB/011: -6dB/ 100: -7dB/101: -8dB/110: -10dB/111: -12dB
14h	[7:0]	Notch_1[15:8]	00h	Notch filter coefficient setting
15h	[7:0]	Notch_1[7:0]	00h	Notch filter coefficient setting
16h	[7:0]	Notch_2[15:8]	00h	Notch filter coefficient setting
17h	[7:0]	Notch_2[7:0]	00h	Notch filter coefficient setting
18h	[7:0]	Notch_3[15:8]	00h	Notch filter coefficient setting
19h	[7:0]	Notch_3[7:0]	00h	Notch filter coefficient setting

Line Out Circuit

LO_MUTE : Line Out Mute LO_GAIN : Line Out Gain
LO_VREFSW : Line Out Voltage Reference Switch

ADRS	Bit	Name	Init	Description
0Eh	[7]	LO_MUTE	1b	Controls the mute function of the line out circuit. 1: Enables MUTE function. 0: Disables MUTE function.
	[6]	LO_VREFSW	1b	Sets the line out circuit. 1: Connects to the reference power source(VREF). 0: Does not connect to the reference power source (VREF).
	[5:4]	LO_GAIN	10b	Select the gain of the line out circuit. 11: 8dB 10: 6dB 01: 4dB 00: 0dB

Speaker Amplifier Circuit

SP_OUT_EN : Speaker Out Enable SP_EXTBP_G : Speaker External Beep Gain
SP_TSD_EN : Speaker Tsd Enable SP_IDL : Speaker Idle Current
SP_EXTBP_EN : Speaker External Beep Enable SP_BIAS : Speaker Bias

ADRS	Bit	Name	Init	Description
0Eh	[0]	SP_OUT_EN	0b	Enables or disables the speaker amplifier circuit. 1: ON 0: OFF
0Fh	[7]	SP_TSD_EN	1b	Enables or disables the thermal shutdown function of the speaker amplifier circuit. 1: ON 0: OFF
	[6]	SP_EXTBP_EN	0b	Enables or disables the external input beep function of the speaker amplifier circuit. 1: ON 0: OFF
	[5:4]	SP_EXTBP_G	00b	Select the external input beep gain of the speaker amplifier circuit. 11: -21dB 10: -18dB 01: -15dB 00: -12dB
	[3:2]	SP_IDL	10b	Set the idling current of the speaker amplifier circuit. 11: 2.0mA 10: 1.0mA 01: 0.67mA 00: 0.5mA
	[1:0]	SP_BIAS	00b	Set the bias of the speaker amplifier circuit. 11: 0.833*AV_{DD} 10: 0.766*AV_{DD} 01: 0.666*AV_{DD} 00: 0.5*AV_{DD}

See the section on "Speaker Amplifier (SP_AMP) Start/Stop Sequence."

Video Circuit

- See the section on the video circuit.

VD_GAIN: Video Driver Gain VD_CTL: Video Driver Control

ADRS	Bit	Name	Init	Description
10h	[5]	VD_GAIN	0b	Selects the driver gain of the video circuit. 0: 6dB 1: 12dB
	[4:3]	VD_CTL2	00b	Select the Input Sync Level DC OFFSET2 of the video circuit. 00: 0mV/01: 62.5mV/10: 125mV 11: Inhibited
	[2:0]	VD_CTL1	010b	Select the Input Sync Level DC OFFSET1 of the video circuit. 001: -12.5mV/010: 0mV/011: 12.5mV/100: 25mV/101: 37.5mV 000/110: Inhibited

Video Driver Sync DC Level Adjustment Table

VD_CTL2[1]	VD_CTL2[0]	VD_CTL1[2]	VD_CTL1[1]	VD_CTL1[0]	Input_Sync_Dc	Output_Sync_Dc
0	0	0	0	1	-12.5mV	100mV
0	0	0	1	0	0mV	100mV
0	0	0	1	1	12.5mV	100mV
0	0	1	0	0	25.0mV	100mV
0	0	1	0	1	37.5mV	100mV
0	1	0	0	1	50.0mV	100mV
0	1	0	1	0	62.5mV	100mV
0	1	0	1	1	75.0mV	100mV
0	1	1	0	0	87.5mV	100mV
0	1	1	0	1	100.0mV	100mV
1	0	0	0	1	112.5mV	100mV
1	0	0	1	0	125.0mV	100mV
1	0	0	1	1	137.5mV	100mV
1	0	1	0	0	150.0mV	100mV
1	0	1	0	1	162.5mV	100mV

Loopback Circuit

SEL_USE_DSP: Select Use Dsp

ADRS	Bit	Name	Init	Description
0Ah	[1:0]	SEL_USE_DSP	00b	Set the DSP path of the loopback circuit. 11: Inhibited 10: ADC through, DSP exists in the DAC path (ADC→ADOUT, DAIN→DSP→DAC) 01: Internal loopback (analog input/output) (ADC→DSP→ADOUT/DAC) 00: DSP exists in the ADC path, DAC through (ADC→DSP→ADOUT, DAIN→DAC)

See the section on the loopback.

PLL Circuit

SEL_MCLKO : Select Mclk Output PLL_FS : Pll Frequency Sampling
MCLKDIV : Mclk Divide PLL_FCKI : Pll

ADRS	Bit	Name	Init	Description
0Dh	[3:2]	SEL_MCLKO	00b	Select the output (MCLKO pin) of the PLL circuit. 00: "L" 10: "H" 01/11: MCLKIN or DIV2(PLL) [ADRS01h, D2 PLL_PDX: DIV2 (PLL) output takes precedence when set to 1.]
11h	[4:0]	PLL_FS	01000b	PLL FS setting 01000: 48kHz/00111: 44.1kHz/00110: 32kHz/00101: 24kHz/ 00100: 22.05kHz/00011: 16kHz/00010: 12kHz/00001: 11.025kHz/ 00000: 8kHz/10000: 7.86113kHz/to 11010: 7.87113kHz (+0.001kHz step)
12h	[2:0]	PLL_FCKI	000b	Set the MCLKIN input frequency of the PLL circuit. 000: 12MHz 001: 24MHz 100: 13.5MHz 101: 27MHz

See the section on the PLL configuration.

PLL Sampling Frequency Setting

FS[4:0]	fs(kHz)
00000	8
00001	11.025
00010	12
00011	16
00100	22.05
00101	24
00110	32
00111	44.1
01000	48

FS[4:0]	fs(kHz)
10000	7.86113
10001	7.86213
10010	7.86313
10011	7.86413
10100	7.86513
10101	7.86613
10110	7.86713
10111	7.86813
11000	7.86913
11001	7.87013
11010	7.87113

IC Test Settings

Must always be fixed to initial values. Note: Addresses TEST1-TEST12 must be set in the order of 1Ah to 25h.

ADRS	Bit	Name	Init	Description
1Ah	[7:0]	TEST1[7:0]	00h	For IC testing. Must always be fixed to the initial value.
1Bh	[7:0]	TEST2[7:0]	01h	For IC testing. Must always be fixed to the initial value.
1Ch	[7:0]	TEST3[7:0]	00h	For IC testing. Must always be fixed to the initial value.
1Dh	[7:0]	TEST4[7:0]	02h	For IC testing. Must always be fixed to the initial value.
1Eh	[7:0]	TEST5[7:0]	03h	For IC testing. Must always be fixed to the initial value.
1Fh	[7:0]	TEST6[7:0]	10h	For IC testing. Must always be fixed to the initial value.
20h	[7:0]	TEST7[7:0]	00h	For IC testing. Must always be fixed to the initial value.
21h	[7:0]	TEST8[7:0]	B0h	For IC testing. Must always be fixed to the initial value.
22h	[7:0]	TEST9[7:0]	21h	For IC testing. Must always be fixed to the initial value.
23h	[7:0]	TEST10[7:0]	00h	For IC testing. Must always be fixed to the initial value.
24h	[7:0]	TEST11[7:0]	00h	For IC testing. Must always be fixed to the initial value.
25h	[7:0]	TEST12[7:0]	00h	For IC testing. Must always be fixed to the initial value.

Specification Details

• Power save/system reset

When the PDNB pin is set to 0, all the circuits are set to power down mode regardless of the power down settings for each block. A 0 on the PDNB pin also triggers a system reset.
After the power is first applied, the system must be reset without fail. (Refer to checkpoint (2) on page 30.)
After resetting, the contents of the serial port register are initialized.
The VREF buffer is activated by releasing power down mode by setting the PDNB pin from 0 to 1, and then by setting VREF_BIAS[1:0] to 01. When VREF_BIAS [1:0] is set to 10, VREF starts. Along with the start of VREF, the LINE output pin is biased to $1/2V_{DD}A$. Once the VREF voltage has stabilized, VREF_BIAS [1:0] must be set to 11 (normal state).

• Microphone (MIC) amplifier

The microphone amplifier has a differential input and a gain of +26dB (typ).
Its gain can also be set to +20 dB or 0 dB by register MGAIN [1:0]. Its input resistance is 70kΩ (typ). The MICPWR is a power output pin for the microphone, and its output voltage is 2.3V (typ 0.767*VDDA).
The maximum output current is 20mA.
The microphone amplifier is placed in the power down mode by setting MIC_PDX to 0.
When MIC_PWR_PDX is set to 0, the microphone power supply circuit is placed in the power down mode.

• Recording system automatic level control (ALC)

The amplifier gain of the PGA (Programmable Gain Amplifier) must be automatically adjusted so that the A/D converter output audio level is setup to the predetermined value. The gain can be varied within a range (maximum) of -14dB to +34dB.
When using ALC in the recording system, set REC_ALC to 1 and PB_ALC to 0 (recording system ALC mode).
When REC_ALC is set to 0 and PB_ALC is set to 0 (ALC off mode), the PGA is placed in the manual mode, and the amplifier gain is fixed to the value of the ALC_GAIN register setting.
When PGA_PDX is set to 0, the PGA is placed in the power down mode. During normal use, the state of PGA_PDX must be switched at the same time as ADC_PDX.
For further details on operation, refer to “Description of ALC/limiter (Automatic Level Control) operation.”
Any of eight recording ALC levels (in 1dB steps from -3dBFS to -10dBFS) can be set using the ALC_VAL register.

• A/D converter

This converts the analog PGA output signals into digital data, which is then output as 16-bit serial audio data. Three formats are supported: I^2S, Left-justified mode, Right-justified mode. A 1st order analog low-pass filter is incorporated for anti-aliasing.
When ADC_PDX is set to 0, the A/D converter block is placed in the power down mode.
The 100/fs period following the release of the power down mode is the A/D converter initialization period, and the data are output as 0.
When the power is first applied and when the system clock is switched, the converter must be initialized.
A digital high-pass filter for canceling DC offset is incorporated.
The filter’s cut-off frequency fc is 0.94Hz (at fs=48kHz). 0dBFS is equivalent to 0.6 *VDDA.

• D/A converter

This converts the digital 16-bit serial audio data into analog signals.
Three formats are supported: I^2S, left justification and right justification.
When DAC_PDX is set to 0, the D/A converter block is placed in the power down mode. When the power down mode is released, the converter is initialized.
When the power is first applied and when the system clock is switched, the converter must be initialized.
0dBFS is equivalent to 0.6 *$V_{DD}A$.

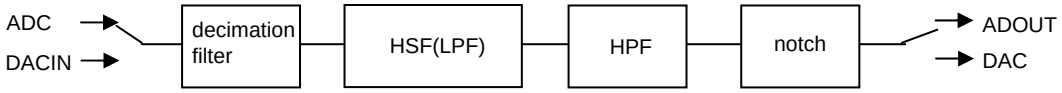
• **Digital volume**

Contained inside the D/A converter is a digital volume control, and by setting EVR_GAIN [6:0], the gain level can be attenuated from +12dB (max) to -64dB or muted.
When EVR_ZCD is 0, the gain is changed immediately after setting EVR_GAIN [6:0].
When EVR_ZCD is 1, after setting EVR_GAIN [6:0] the gain is changed at the zero cross timing of the audio signals. The timeout time for zero cross detection can be set using EVR_ZCDTM [1:0].
When EVR_SOFTSW is 1, the soft switching operation is performed, and after the EVR_GAIN [6:0] setting has been changed, the gain automatically changes in 1-step increments until it arrives at the predetermined value. The period of gain change can be set using EVR_SSC [1:0].
If EVR-SOFTSW is set to 1 and EVR_ZCD is set to 1, the D/A converter, after the lapse of the time defined by EVR_SSC[1:0], repeats the cycle of waiting for the next zero cross point and changing the gain by 1 increment, until the predetermined volume value is reached.

• **Playback system automatic level control (ALC)**

When REC_ALC is set to 0 and PB_ALC is set to 1 (playback system ALC mode), the digital volume control functions as the playback system ALC. Subject the volume value to automatic adjustment so that the digital volume output level is set to the predetermined value.
For further details on operation, refer to “Description of ALC/limiter (automatic level control) operation.”
When REC_ALC is set to 0 and PB_ALC is set to 0 (ALC off mode), the digital volume control is set to manual mode, and the gain is fixed to the EVR_GAIN [6:0] register setting.

Programmable Digital Filter



• **High-pass filter (HPF, 1st order)**

WIND_CUT [5:4] turns off the high-pass filter (through) when initialized to (00).
Regardless of the sampling frequency (fs), the cutoff frequency (fc) is 400 Hz when WIND_CUT [5:4] is set at 11, 300Hz at 10, 200Hz at 01 and OFF at 00.

• **Programmable digital high frequency shelf filter (HSF)**

Attenuation range only of HSF (same as low-pass filter)
This is a 2nd-order biquad type of filter, and its attenuation amount at 1/2fs can be set to 0, -2, -4, -6, -8, -10 or -12dB.

HSF filter	Name	ADRS	bit	Description
HSF filter ON/OFF	HSF_ON	08h	[7]	0: OFF 1: ON
HSF filter gain setting	HPF_HSF	13h	[2:0]	000: 0dB, 001: -2dB, 010: -4dB, 011: -6dB 100: -7dB, 101: -8dB, 110: -10dB, 111: -12dB

• **Notch filter**

This is a 2nd-order biquad type of filter, and its coefficients are set using the register.
Specify the sampling frequency (fs), cut-off frequency (fc) and bandwidth (fd), and load coefficients a, b and c represented in 16-bit 2’s complement format in the register.

Notch filter	Name	ADRS	bit	Description
Notch filter ON/OFF	NOTCH_ON	08h	[6]	0: OFF 1: ON
Notch_1 coefficient setting (1)	Notch_1[15:8]	14h	[7:0]	Coefficient a setting
Notch_1 coefficient setting (2)	Notch_1[7:0]	15h	[7:0]	Coefficient a setting
Notch_2 coefficient setting (1)	Notch_2[15:8]	16h	[7:0]	Coefficient b setting
Notch_2 coefficient setting (2)	Notch_2[7:0]	17h	[7:0]	Coefficient b setting
Notch_3 coefficient setting (1)	Notch_3[15:8]	18h	[7:0]	Coefficient c setting
Notch_3 coefficient setting (2)	Notch_3[7:0]	19h	[7:0]	Coefficient c setting

• Line amplifier

The line amplifier provides a gain of 0, 4, 6 or 6dB.
When LO_MUTE is set to 1, the line output is muted.
When LO_PDX is set to 0, the line amplifier is placed in the power down mode.
If the line output is set to the high-impedance state when the line amplifier is placed in the power down mode, LO_VREFSW must be set to 0.

LINE OUT	Name	ADRS	bit	Description
Power down	LO_PDX	00h	[1]	0: Power down 1: Power up
Mute	LO_MUTE	0Eh	[7]	0: Disables MUTE. 1: Enables MUTE.
Connection to VREF	LO_VREFSW	0Eh	[6]	0: Does not connect to VREF. 1: Connects to VREF*.
Gain select	LO_GAIN	0Eh	[5:4]	00: 0dB, 01: 4dB, 10: 6dB, 11: 8dB

* It is not possible to connect between LINE OUT and VREF by setting LO_VREFSW to 1 even if LO_PDX is set to 1.

• Speaker amplifier

The speaker amplifier must be started after the selector amplifier output (LOUT2) has been activated and the voltage has stabilized. Either 0dB or +6dB can be selected as the selector amplifier gain using the SEL_GAIN setting.
$V_{DD}S$ in the range of 2.7V to 5.5V is supported. (Piezoelectric speaker supported)
The amplifier gain is 6dB (+12dB with the BTL output). (With an 8Ω load)
The SPKIN input resistance is 10 kΩ (type). The gain from the BEEP input to BTL output can be varied within the range of -12dB to -21dB using the SP_EXTBP_G [1:0] setting.
When SP_PDX is set to 0, the speaker amplifier is placed in the power down mode.
Depending on VDDS, one of the four speaker terminal voltages (1.5V, 2V, 2.3V and 2.5V) can be selected using SP_BAIS [1:0] to achieve an optimal dynamic range. (At $V_{DD}A$=3V)

• Thermal shutdown

If a chip temperature of 140°C or higher is detected while SP_TSD_EN is set 1, the speaker amplifier is placed in the power down mode for protection.
The thermal shutdown function is disabled if SP_TSD_EN is set to 0.

SPEAKER AMP	Name	ADRS	bit	Description
Power down mode	SP_PDX	00h	[0]	0: Power down 1: Power up
Output enable	SP_OUT_EN	0Eh	[0]	0: Disable 1: Enable
Thermal shutdown	SP_TSD_EN	0Fh	[7]	0: Disable 1: Enable
External BEEP input	SP_EXTBP_EN	0Fh	[6]	0: Disable 1: Enable
BEEP gain select	SP_EXTBP_G	0Fh	[5:4]	00: -12dB, 01: -15dB, 10: -18dB, 11: -21dB
Idling current setting	SP_IDL	0Fh	[3:2]	00: 0.5mA, 01: 0.67mA, 10: 1.0mA, 11: 2.0mA
Bias voltage setting	SP_BIAS	0Fh	[1:0]	00: 0.5, 01: 0.666, 10: 0.766, 11: 0.833 (*$V_{DD}A$)

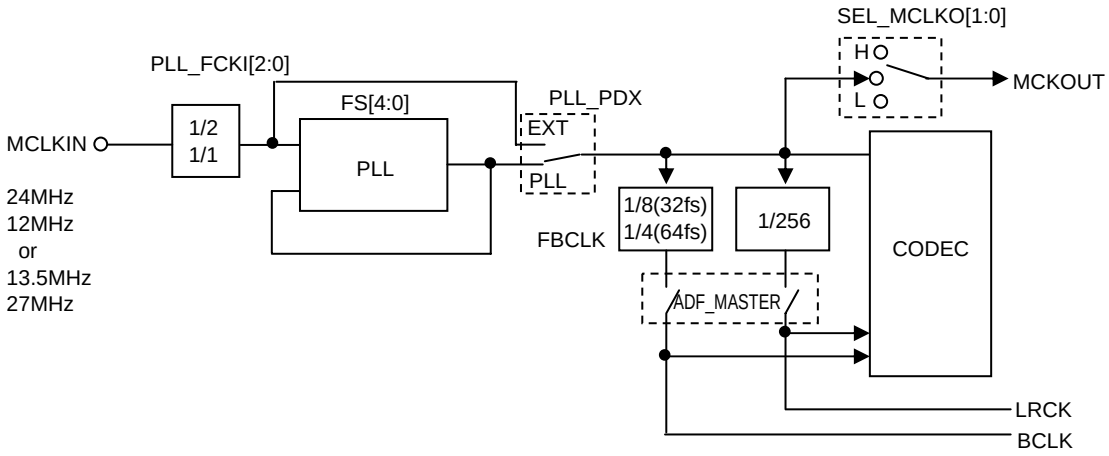
• PLL

(a) PLL mode (PLL_PDX=1)
In this mode, the 256fs clock (MCLK) used by the CODEC block is generated from the clock (12, 13.5, 24 and 27MHz frequencies supported) which is input from MCLK, and BCLK and LRCK are output.
Sampling frequencies (fs) of 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz and 48kHz are supported.

(b) EXT mode (PLL_PDX=0)
In this mode, the 256fs clock (MCLK) from MCLKIN is input and used.
When ADF_MASTER is 1, BCLK and LRCK whose frequency is obtained by dividing the frequency of MCLKIN are output.
When ADF_MASTER is 0, BLCK and LRCK are external inputs.

* In the CODEC block, BCLK and LRCK must be synchronized with MCLK.
In PLL mode (PLL_PDX=1), operation must be performed in BCLK output mode (ADF_MASTER=1). In EXT mode (PLL_PDX=0) and when ADF_MASTER is 0, BCLK and LRCK synchronized with MCLK must be input.

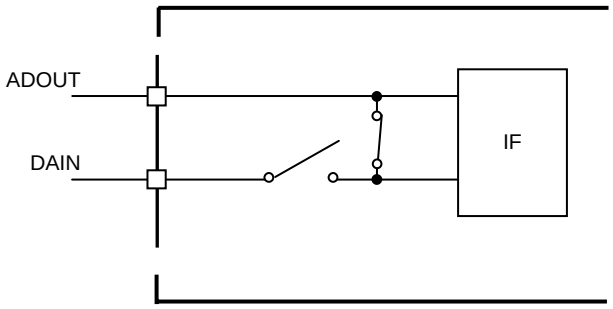
PLL Block Diagram



- **Loopback**

(a) Loopback mode (SEL_USE_DSP [1:0] =01)
Connect between ADOUT and DAIN. This enables the MIC input to be output to the line or speaker without recording or playback operation. In this case, external output through ADOUT is enabled but external input through DAIN is disabled.

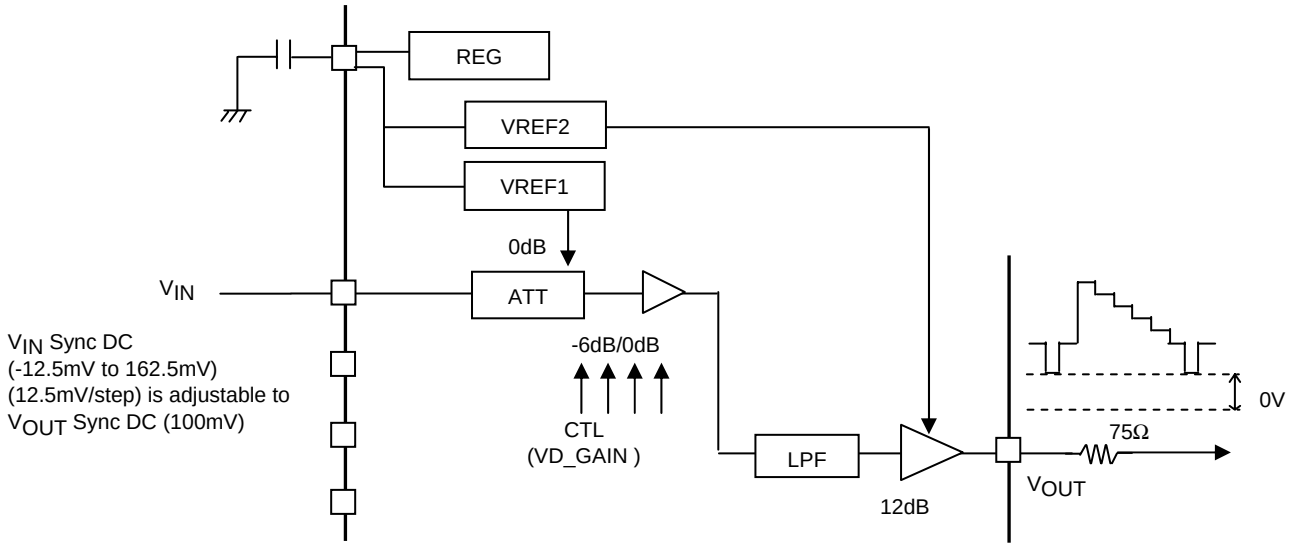
(b) Standard mode (SEL_USE_DSP [1:0] =00 or 10)
The DAIN external input is enabled and the internal switch for ADOUT and DAIN is released.



SEL_USE_DSP[1:0]	Signal Path	Description of Function	Application (Uses)
00	ADC ->DSP ->ADC_Dout DAC_Din ->--->DAC	ADC, DAC parallel operation DSP inserted in REC (ADC) side	DSP function exists in REC (ADC) side
01	ADC ->DSP ->ADC_Dout ADC ->DSP ->DAC	ADC, DAC loopback operation DAC_Din input disabled	Analog input/output, DSP function test
10	ADC ->--->ADC_Dout ADC ->DSP ->DAC	ADC, DAC parallel operation DSP inserted in PB (DAC) side	SDP function exists in PB(DAC) side
11	-	-	Inhibited

Note: The LPF, wind cut and notch functions serve as the DSP functions.

• **Video driver**



Either 6dB or 12dB can be selected as the total gain of the video amplifier using the internal register setting (VD_GAIN). When the input sync level is within the -12.5mV to 162.5mV range, the output sync level can be adjusted to 0.1V using the internal register settings (VD_CTL1 [2:0] and VD_CTL2 [1:0]).

Description of ALC/Limiter (automatic level control) operation

Note: [xxxx] denotes a register name, and whatever is contained inside the parentheses “ ” is applicable in the PB-ALC mode.

The amplifier gain “digital volume value” of the PGA (programmable gain amplifier) is automatically adjusted so that the A/D converter output audio level “digital volume output” is set to the ALC value [ALC_VAL [2:0]]. The PGA “digital volume” gain can be varied in the -14dB to +34dB range. The maximum value [ALC_VMAX [5:0]] can be set in this variable range.

=> If [ALC_VMAX [5:0]] is set to the maximum value of +34dB, the ALC functions can be used to the maximum.

=> If [ALC_VMAX [5:0]] is set to +0dB, it will no longer be possible to increase the gain in the “+” direction so the ALC function will work in the same way as a limiter.

• **ALC settings**

(a) Power-saving function

When [PGA_PDX] is 0, the ALC circuit and PGA circuit are set to power down mode.

(b) Manual function

When both [REC_ALC] and [PB_ALC] are 0, manual mode is established.

In the REC_ALC mode, the PGA gain is fixed at the manual mode value [ALC_GAIN [5:0]].

In the PB_ALC mode, the digital volume level is fixed at [EVR_GAIN [6:0]].

(c) System operation

ALC is performed by feeding back the A/D converter “digital volume” data. Accordingly, configure the settings as shown in the table below in order for the ALC functions to be activated.

	REC-ALC	PB-ALC
PGA_PDX	1	0
ALCOFF	0	0
ADC_PDX	1	x
DAC_PDX	x	1
REC_ALC	1	0
PB_ALC	0	1

• Description of ALC operation

The ALC has two types of operation, “attack” and “recovery.” Refer to the operation diagrams on the next page.

(1) Attack operation

When the A/D converter “digital volume” output exceeds the ALC value [ALC_VAL [2:0]], the PGA gain “digital volume value” is reduced at a rate determined by the attack coefficient [ALC_FA [1:0]].

When zero cross detection [ALC_ZCD] is set to 1, the gain attenuation from zero cross to zero cross is limited by the limit value [ALC_ATLIM [1:0]].

(2) Recovery operation

When the A/D converter “digital volume” output is within 2 dB of the ALC value [ALC_VAL[1:0]] and this status continues for the recovery wait time [ALC_RWT [1:0]], the PGA gain “digital volume value” is increased at a rate determined by the recovery coefficient [ALC_FR [2:0]]. This increase in the PGA gain “digital volume value” continues while the output remains within 2dB of the ALC value [ALC_VAL [1:0]]. The maximum increase in the PGA gain “digital volume value” from zero cross to zero cross is 1dB.

Functions common to (1) and (2)

- Zero cross detection

  When [ALC_ZCD] is set to 0, the PGA gain “digital volume value” changes regardless of the zero cross timing of the A/D converter “digital volume” output.

  When [ALC_ZCD] is set to 1, the PGA gain “digital volume value” changes at the zero cross timing of the A/D converter “digital volume” output.

- Zero cross timeout

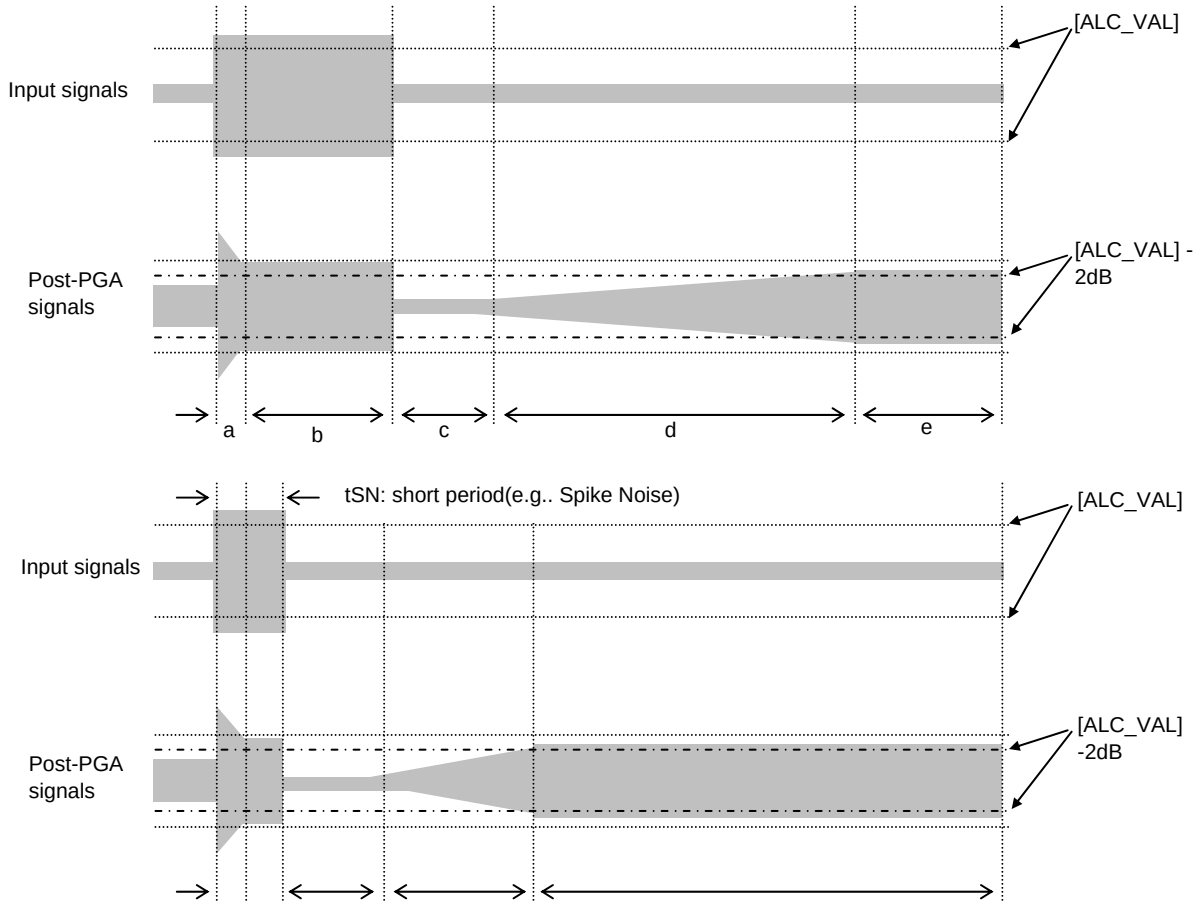
  A zero cross signal is generated internally if there is no zero cross signal during the zero cross timeout value [ALC_ZCDTM [1:0]] even when the PGA gain “digital volume” output is not zero-crossed.

- Average output amplitude control

  The average output amplitude is reduced by spike and other noises in an attach operation.

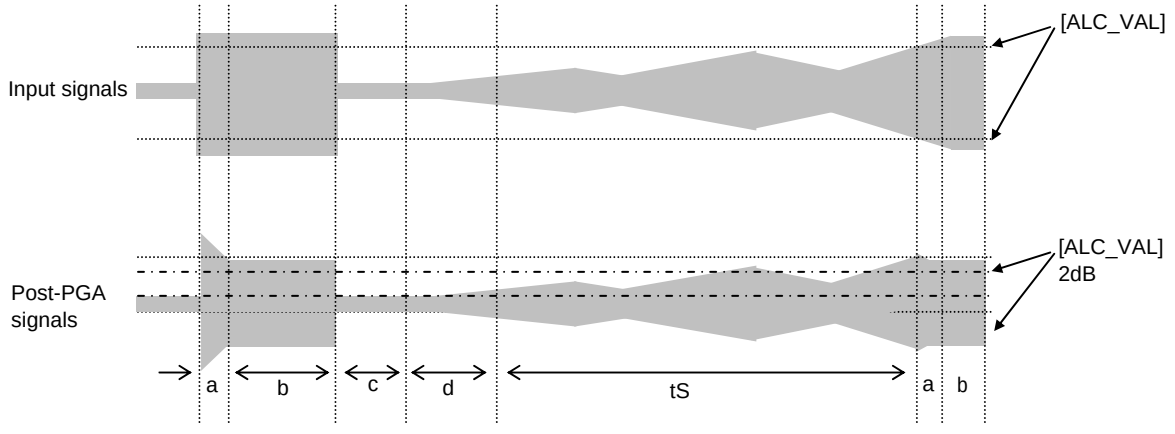
  To prevent this, the recovery rate is automatically increased above the [ALC_FR [2:0]] setting value when there is an excessively high input in a short period of time.

ALC Wave Forms



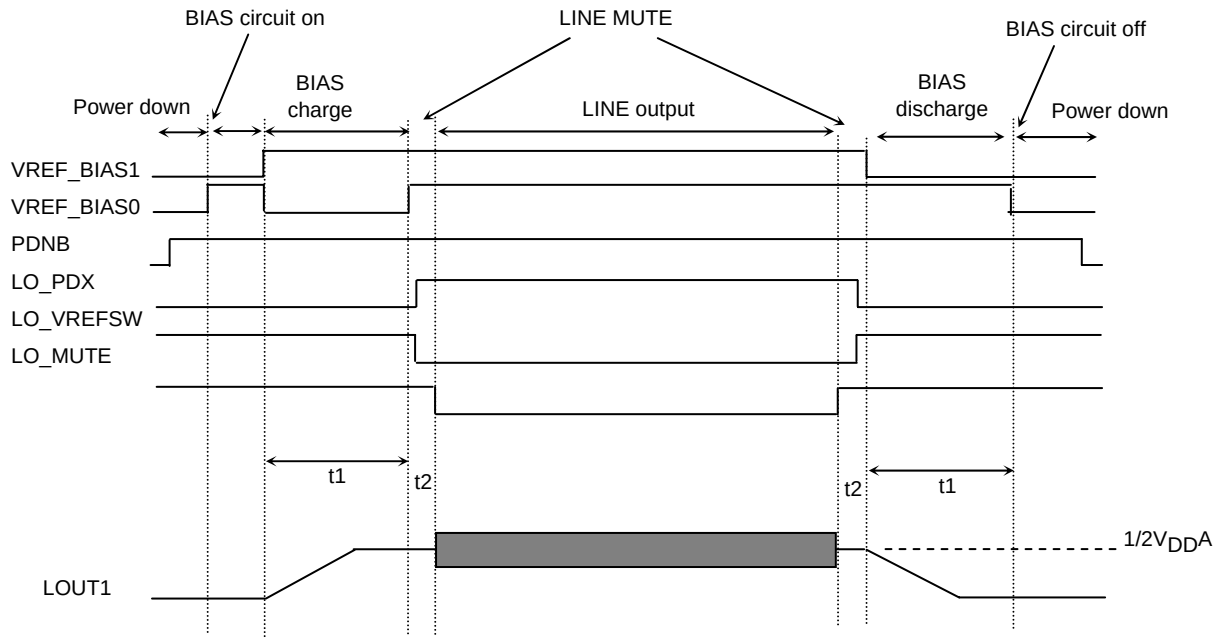
Region	Operation	PGA Gain	Related Registers
a, A	Attack	Sudden attenuation	[ALC_FA] attack coefficient
b, B	Stable	Constant	[ALC_VAL] ALC value
c, C	Wait for recovery	Constant	[ALC_RWT] recovery wait time
d,	Recovery	Slow increase	[ALC_FR] recovery coefficient
, D	Recovery	Faster increase than d	-
e, E	Stable	Constant	[ALC_VMAX] PGA gain maximum value

Limiter operation (maximum gain value [ALC_VMAX] set to 0dB)



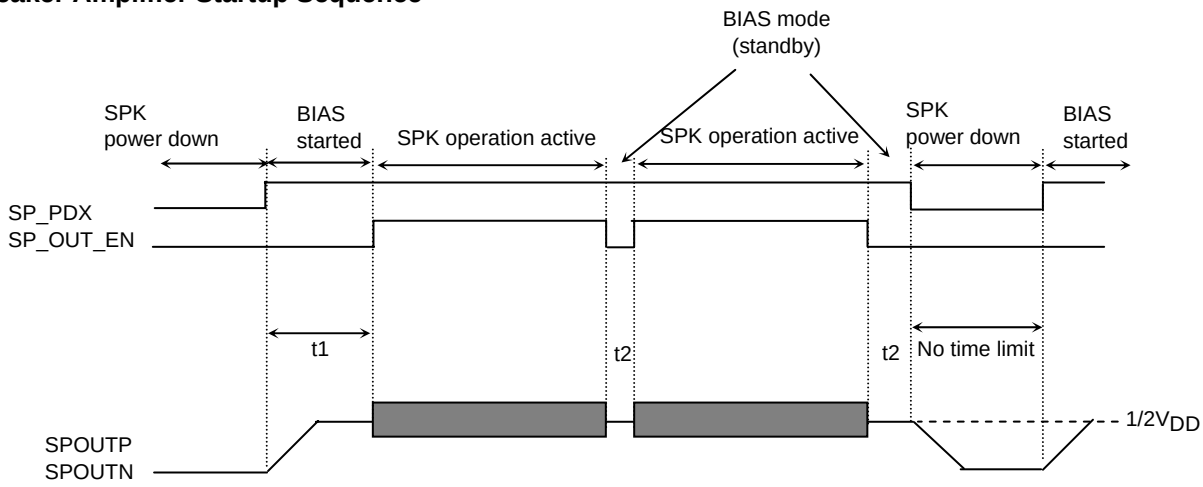
In the tS region, the “input” and “post-PGA” signal levels are the same. (Signal level through)

VREF/line out start/stop sequence



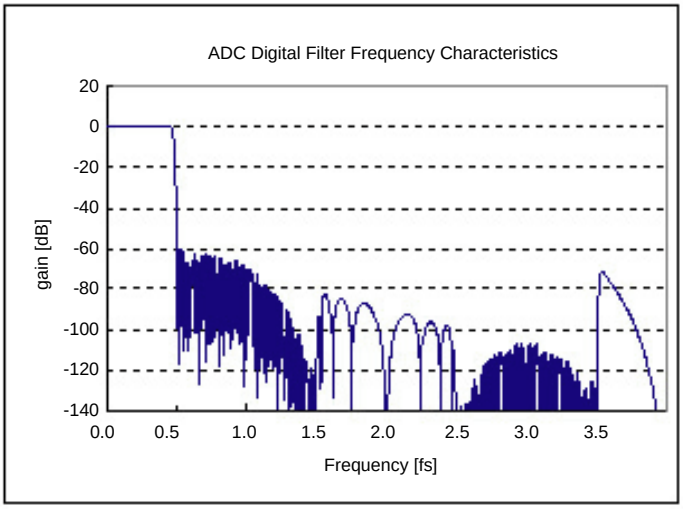
- Recommended values
  t1 = 300ms or more (when external capacitance connected to VREF is 1µF)
  t2 = 1ms or more

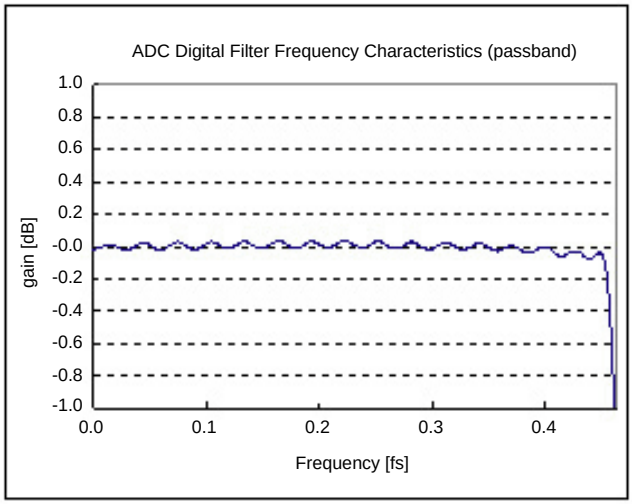
Speaker Amplifier Startup Sequence



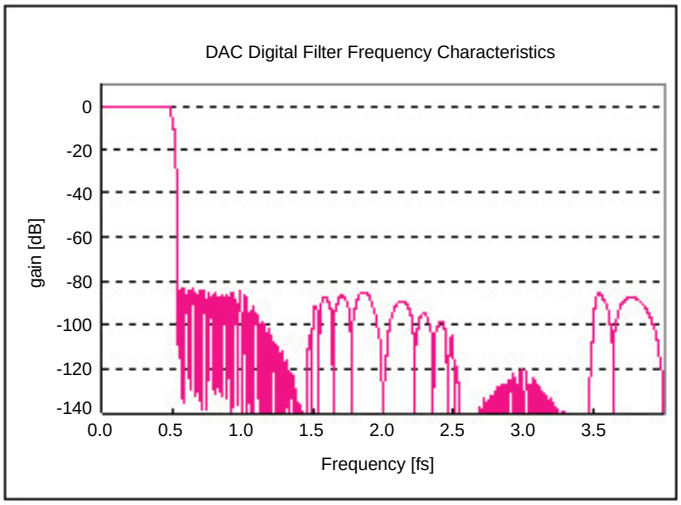
- Recommended values
  t1 = 40ms or more (when external capacitance connected to SPKIN is 0.1µF)
  t2 = 10ms or more
- SP_OUT_EN, SPK_PDX must be set to 0 when the SPK is placed in the power down mode.

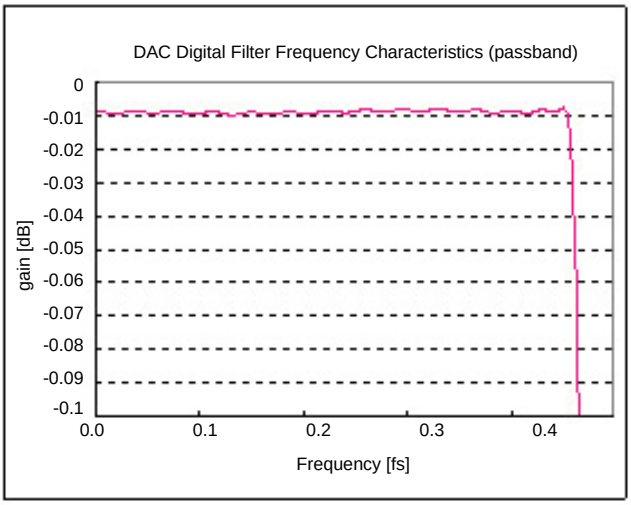
ADC Decimation Filter



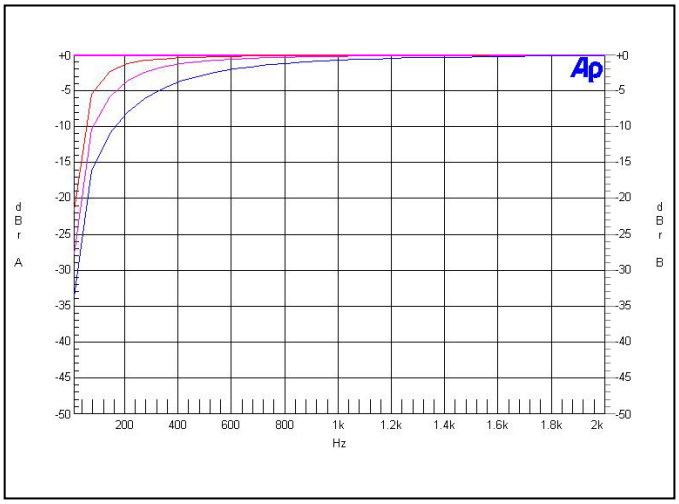


DAC Interpolation Filter

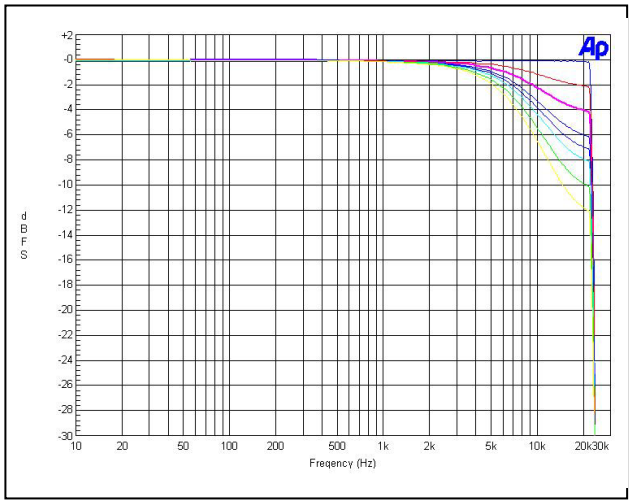




High_Pass_Filter



HSF_Filter



Checkpoints

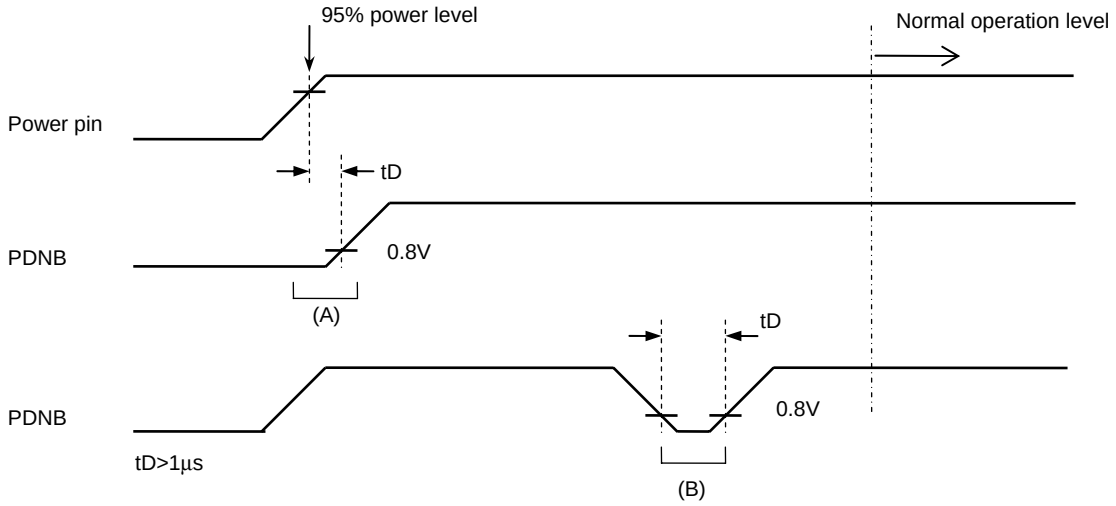
The user is responsible for ascertaining whether this IC can be adopted for the set to be mass production by the user, including the various condition for mounting in the set.

1) Power supply

- The 3.0V type and 3.0V/5.0V type are available as the power supply pins.
  3.0V type: Digital power supply (V_{DD}), analog power supplies ($V_{DD}A$, $V_{DD}V$, $V_{DD}P$)
  3.0V/5.0V type: Analog power supply ($V_{DD}S$)
- The power-on sequence is such that the power is first applied in sequence starting with the circuits that operate using a high voltage and the power is turned off in sequence starting with the circuits that operate using a low voltage.

2) Resetting

- At power-on, the PDNB pin must be set to low without fail.
  (A) or (B) is executed as shown in the figure below.

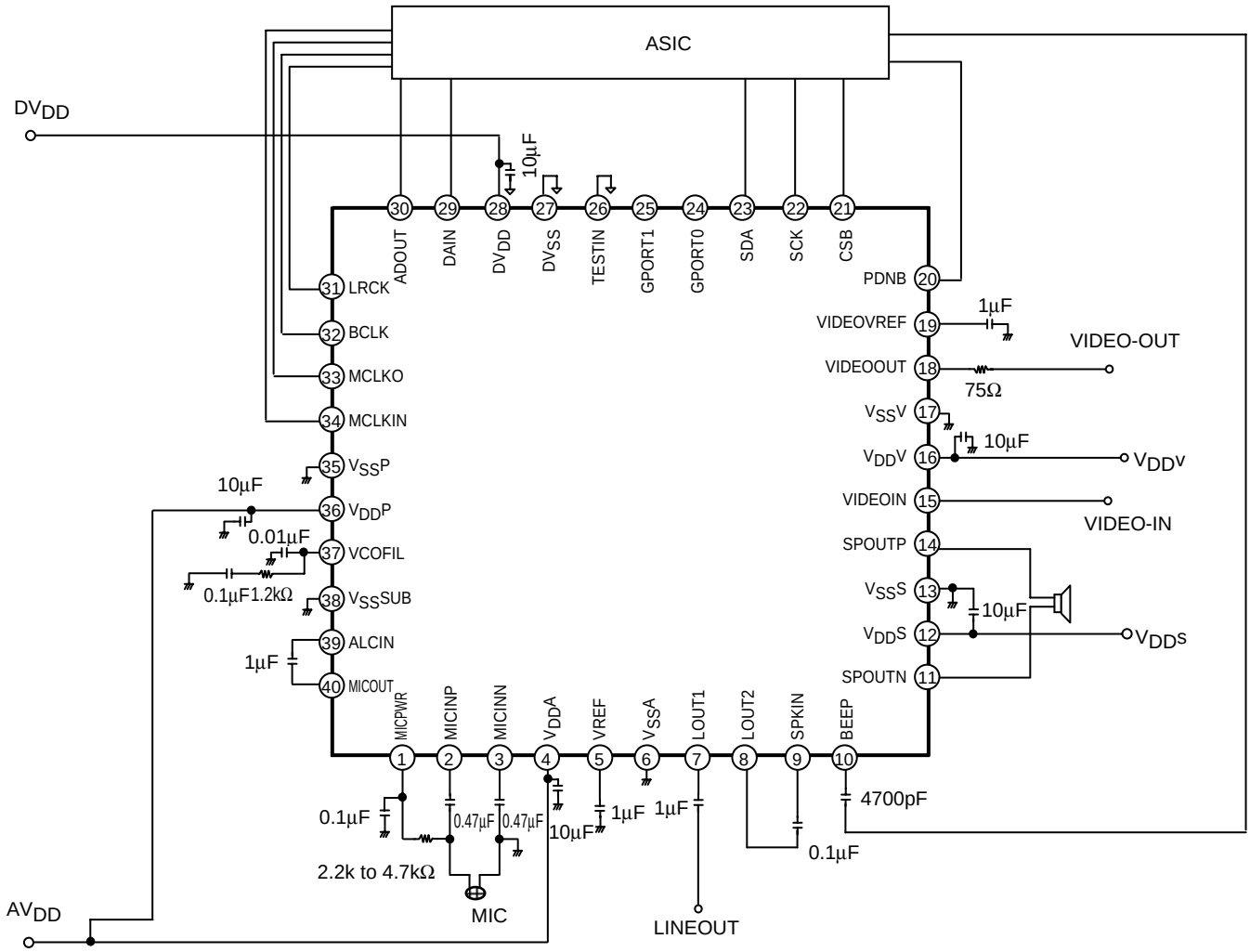


Notes: (A) is reset at the same time as the power is first applied.
(B) is reset immediately after the power is first applied.
The MCLKIN pin clock input must be provided without fail during either the (A) or (B) period.

3) 3-line serial setting

- Whenever 3-line serial setting is to be performed, it must be done where the MCLKIN input has stabilized without fail.
- If garbled data is found, restart the IC (switching the state of the PDNB pin from low to high) and perform 3-line serial setting again.

Sample Application Circuit



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