

Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	60	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10$ V	0.050
Q_g (Max.) (nC)	46	
Q_{gs} (nC)	11	
Q_{gd} (nC)	22	
Configuration	Single	

FEATURES

- Advanced Process Technology
- Surface Mount
- Low-Profile Through-Hole (IRFZ34L/SiHFZ34L)
- 175 °C Operating Temperature
- Fast Switching
- Lead (Pb)-free Available



Available
RoHS*
COMPLIANT

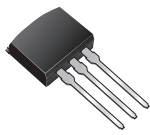
DESCRIPTION

Third generation Power MOSFETs from Vishay utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

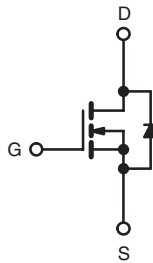
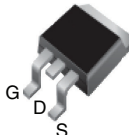
The D²PAK is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2 W in a typical surface mount application.

The through-hole version (IRFZ34L/SiHFZ34L) is available for low-profile applications.

I²PAK (TO-262)



D²PAK (TO-263)



N-Channel MOSFET

ORDERING INFORMATION

Package	D ² PAK (TO-263)	D ² PAK (TO-263)	D ² PAK (TO-263)	I ² PAK (TO-263)
Lead (Pb)-free	IRFZ34SPbF	IRFZ34STRRPbF ^a	IRFZ34STRLPbF ^a	IRFZ34LPbF
	SiHFZ34S-E3	SiHFZ34STRPbF ^a	SiHFZ34STLPbF ^a	SiHFZ34L-E3
SnPb	IRFZ34S	IRFZ34STRR ^a	IRFZ34STRL ^a	IRFZ34L
	SiHFZ34S	SiHFZ34STR ^a	SiHFZ34STL ^a	SiHFZ34L

Note

- a. See device orientation.

ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	V_{GS} at 10 V	$T_C = 25$ °C	30
		$T_C = 100$ °C	21
Pulsed Drain Current ^{a, e}	I_{DM}	120	A
Linear Derating Factor		0.59	W/°C
Single Pulse Avalanche Energy ^{b, e}	E_{AS}	200	mJ
Maximum Power Dissipation	P_D	$T_C = 25$ °C	88
		$T_A = 25$ °C	3.7
Peak Diode Recovery dV/dt ^{c, e}	dV/dt	4.5	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature)		for 10 s	

Notes


- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
 b. $V_{DD} = 25$ V, Starting $T_J = 25$ °C, $L = 260$ μ H, $R_G = 25$ Ω , $I_{AS} = 30$ A (see fig. 12).
 c. $I_{SD} \leq 30$ A, $dI/dt \leq 200$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 175$ °C.
 d. 1.6 mm from case.
 e. Uses IRFZ34/SiHFZ34 data and test conditions.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mount) ^a	R_{thJA}	-	40	°C / W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.7	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}^c$	-	0.065	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$	-	-	25	μA
		$V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 18\text{ A}^b$	-	-	0.05	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 25\text{ V}, I_D = 18\text{ A}^b$	9.3	-	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$, see fig. 5 ^c	-	1200	-	μF
Output Capacitance	C_{oss}		-	600	-	
Reverse Transfer Capacitance	C_{rss}		-	100	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}, I_D = 30\text{ A}, V_{DS} = 48\text{ V}$, see fig. 6 and 13 ^{b, c}	-	-	46	nC
Gate-Source Charge	Q_{gs}		-	-	11	
Gate-Drain Charge	Q_{gd}		-	-	22	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30\text{ V}, I_D = 30\text{ A}, R_G = 12\text{ }\Omega, R_D = 1.0\text{ }\Omega$, see fig. 10 ^{b, c}	-	13	-	ns
Rise Time	t_r		-	100	-	
Turn-Off Delay Time	$t_{d(off)}$		-	29	-	
Fall Time	t_f		-	52	-	
Internal Source Inductance	L_S	Between lead, and center of die contact	-	7.5	-	nH
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	30	A
Pulsed Diode Forward Current ^a	I_{SM}		-	-	120	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 30\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.6	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 30\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b, c$	-	120	230	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	700	1400	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- c. Uses IrFZ34/SiHFZ34 data and test conditions.



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

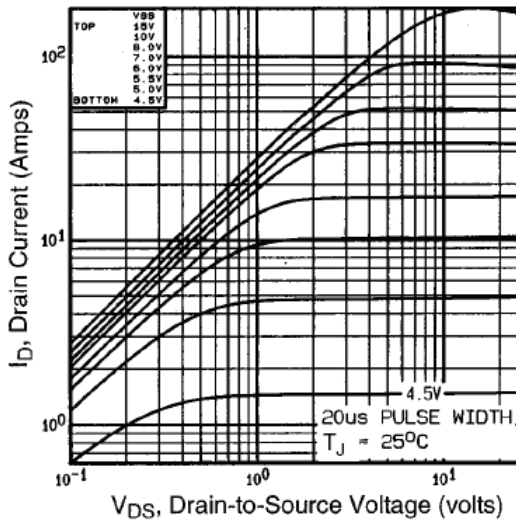


Fig. 1 - Typical Output Characteristics

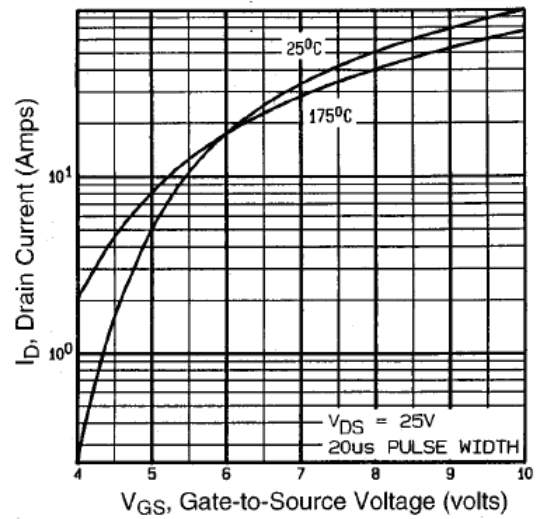


Fig. 3 - Typical Transfer Characteristics

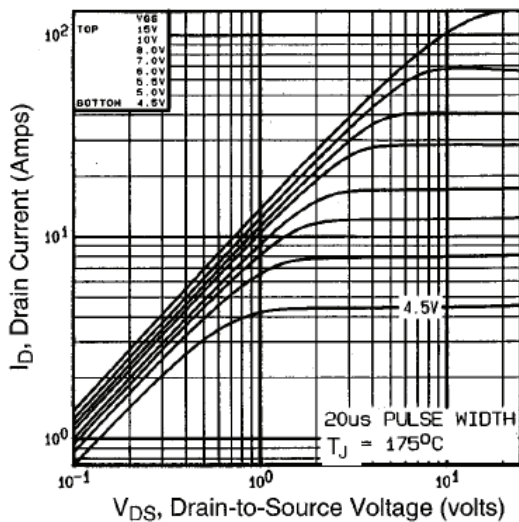


Fig. 2 - Typical Output Characteristics

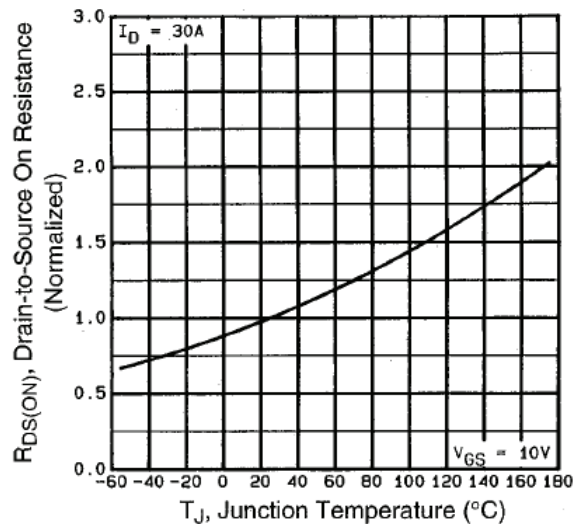


Fig. 4 - Normalized On-Resistance vs. Temperature

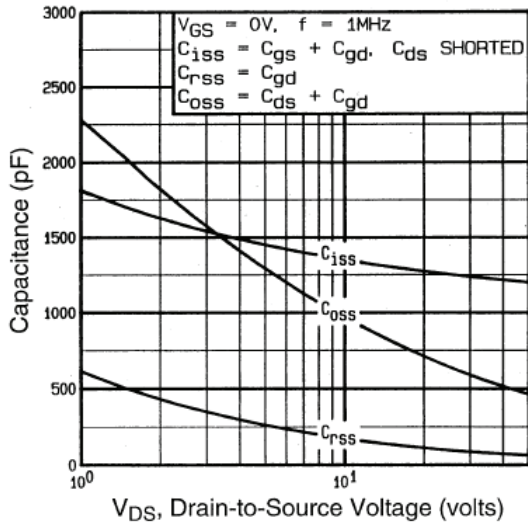


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

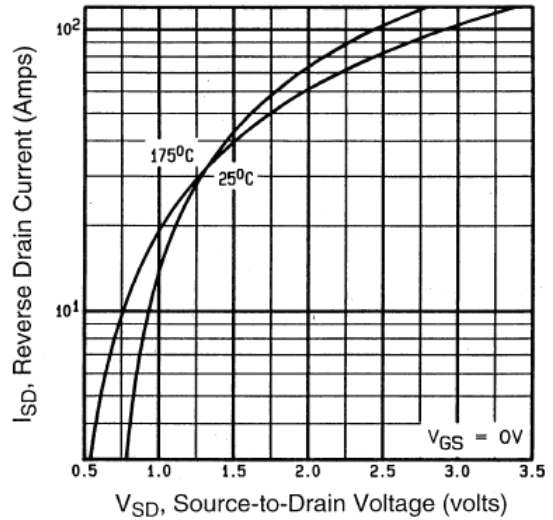


Fig. 7 - Typical Source-Drain Diode Forward Voltage

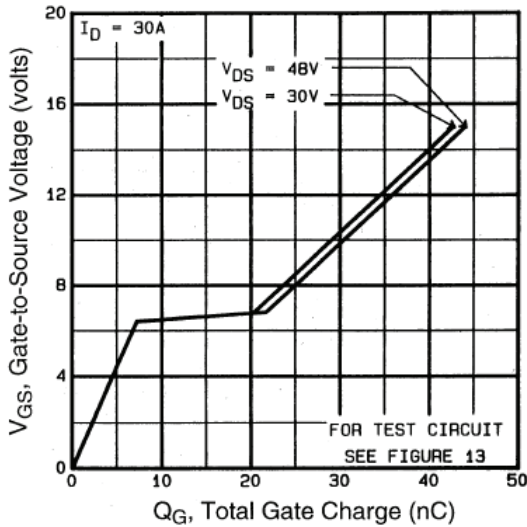


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

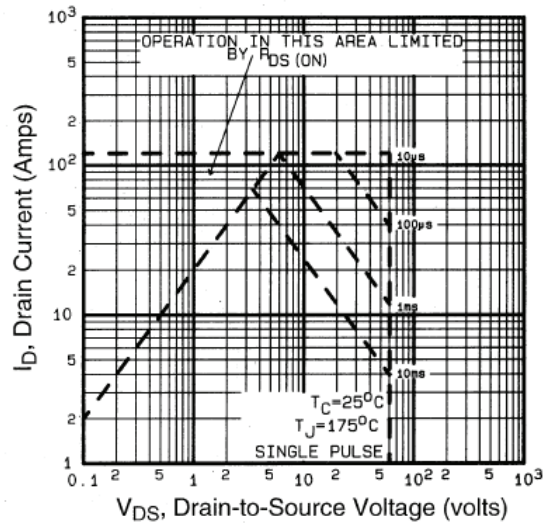


Fig. 8 - Maximum Safe Operating Area

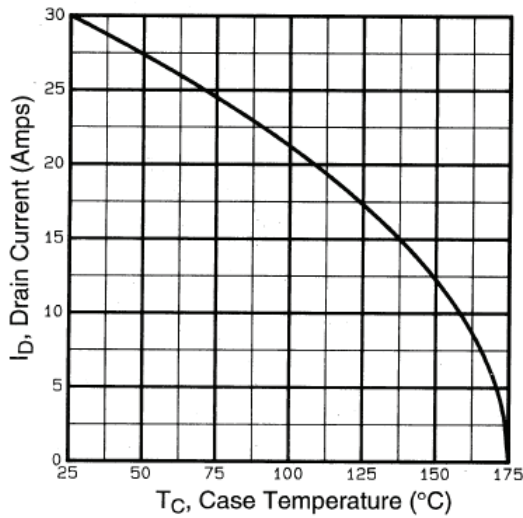


Fig. 9 - Maximum Drain Current vs. Case Temperature

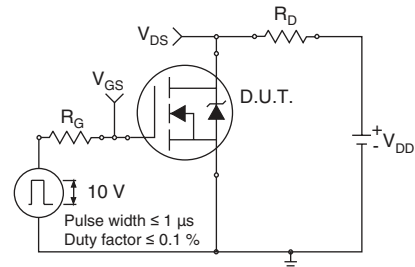


Fig. 10a - Switching Time Test Circuit

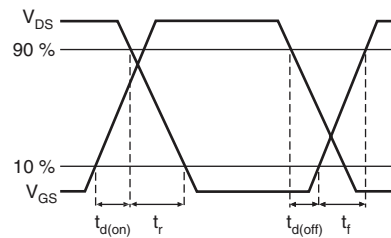


Fig. 10b - Switching Time Waveforms

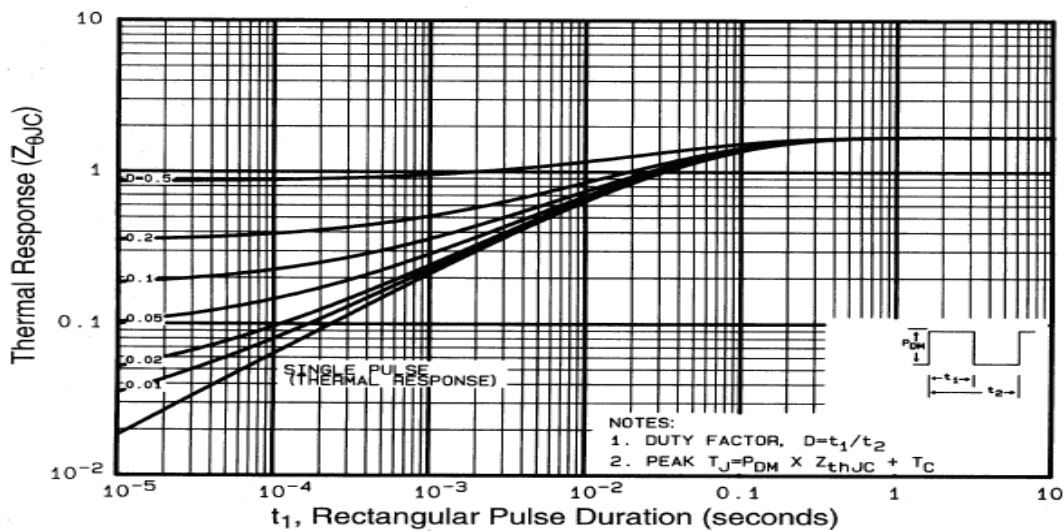


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

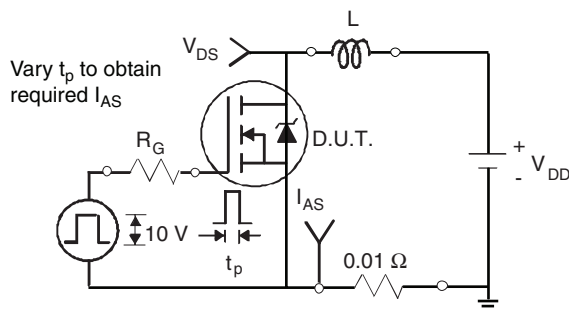


Fig. 12a - Unclamped Inductive Test Circuit

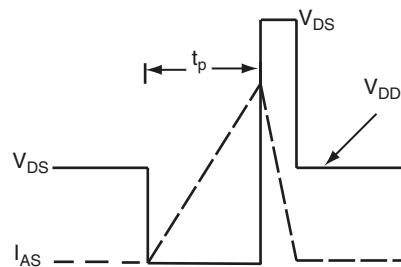


Fig. 12b - Unclamped Inductive Waveforms

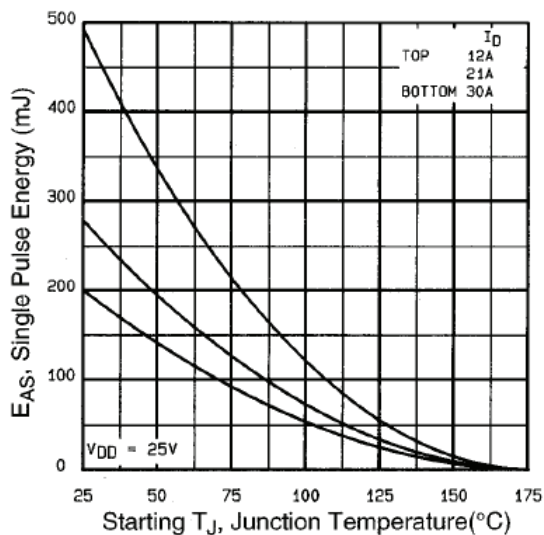


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

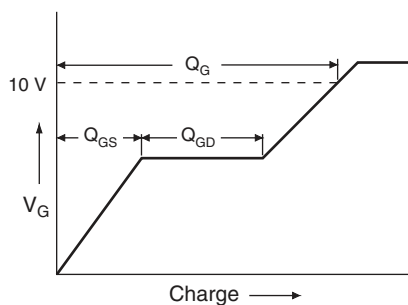


Fig. 13a - Maximum Avalanche Energy vs. Drain Current

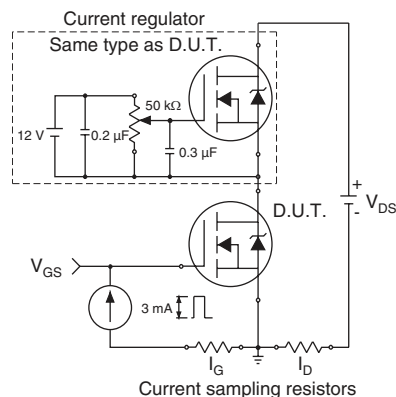


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

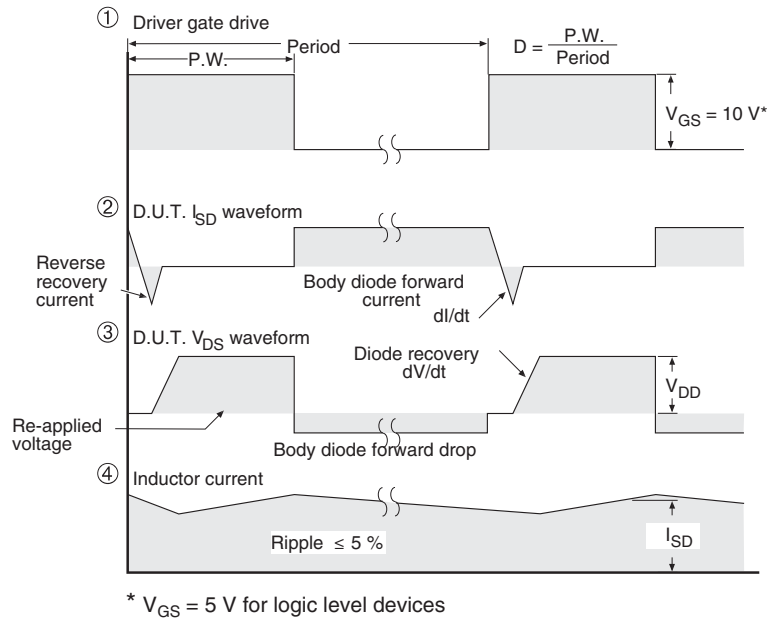
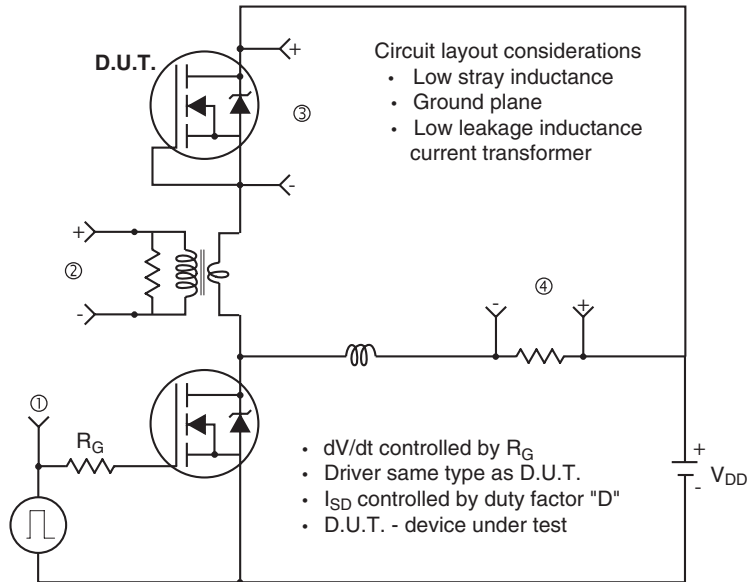


Fig. 14 - For N-Channel

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