

RD74VT1G86

2-input Exclusive-OR Gate / Dual Supply Voltage Translator

REJ03D0516-0100

Rev.1.00

Apr. 15, 2005

Description

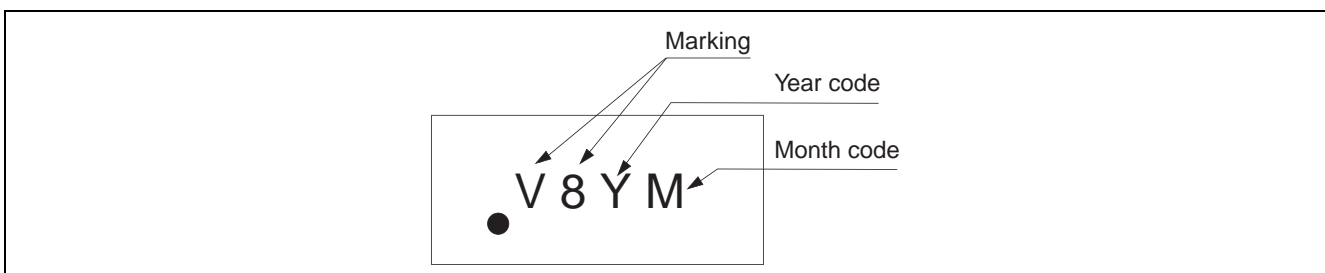
The RD74VT1G86 performs the Boolean functions $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$ in positive logic. A common application is as a true / complement element. If one of the inputs is low, the other input will be reproduced in true form at the output. If one of the inputs is high, the signal on the other input will be reproduced inverted form at the output. The input is designed to track V_{CCIN} , which accepts voltage from 1.2V to 3.6V, and the output is designed to track V_{CCOUT} , which operates at 1.2V to 3.6V. Low voltage and high-speed operation is suitable for the battery powered products (e.g., notebook computers), and the low power consumption extends the battery life.

Features

- This product function as level shift that change V_{CCIN} input level to V_{CCOUT} output level by providing different supply voltage to V_{CCIN} and V_{CCOUT} .
- The basic gate function is lined up as Renesas uni logic series.
- Supplied on emboss taping for high-speed automatic mounting.
- Supply voltage range: $V_{CCIN} = 1.2 \text{ V to } 3.6 \text{ V}$
 $V_{CCOUT} = 1.2 \text{ V to } 3.6 \text{ V}$
Operating temperature range: $-40 \text{ to } +85^\circ\text{C}$
- All inputs $V_{IH} (\text{Max.}) = 3.6 \text{ V} (@V_{CCIN} = 0 \text{ V to } 3.6 \text{ V})$
Outputs $V_O (\text{Max.}) = 3.6 \text{ V} (@V_{CCOUT} = 0 \text{ V})$
- Output current $\pm 2 \text{ mA} (@V_{CCOUT} = 1.2 \text{ V})$
 $\pm 4 \text{ mA} (@V_{CCOUT} = 1.4 \text{ V to } 1.6 \text{ V})$
 $\pm 6 \text{ mA} (@V_{CCOUT} = 1.65 \text{ V to } 1.95 \text{ V})$
 $\pm 18 \text{ mA} (@V_{CCOUT} = 2.3 \text{ V to } 2.7 \text{ V})$
 $\pm 24 \text{ mA} (@V_{CCOUT} = 3.0 \text{ V to } 3.6 \text{ V})$
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
RD74VT1G86CLE	WCSP-6 pin	SXBG0006KB-A (TBS-6AV)	CL	E (3,000 pcs/reel)

Article Indication

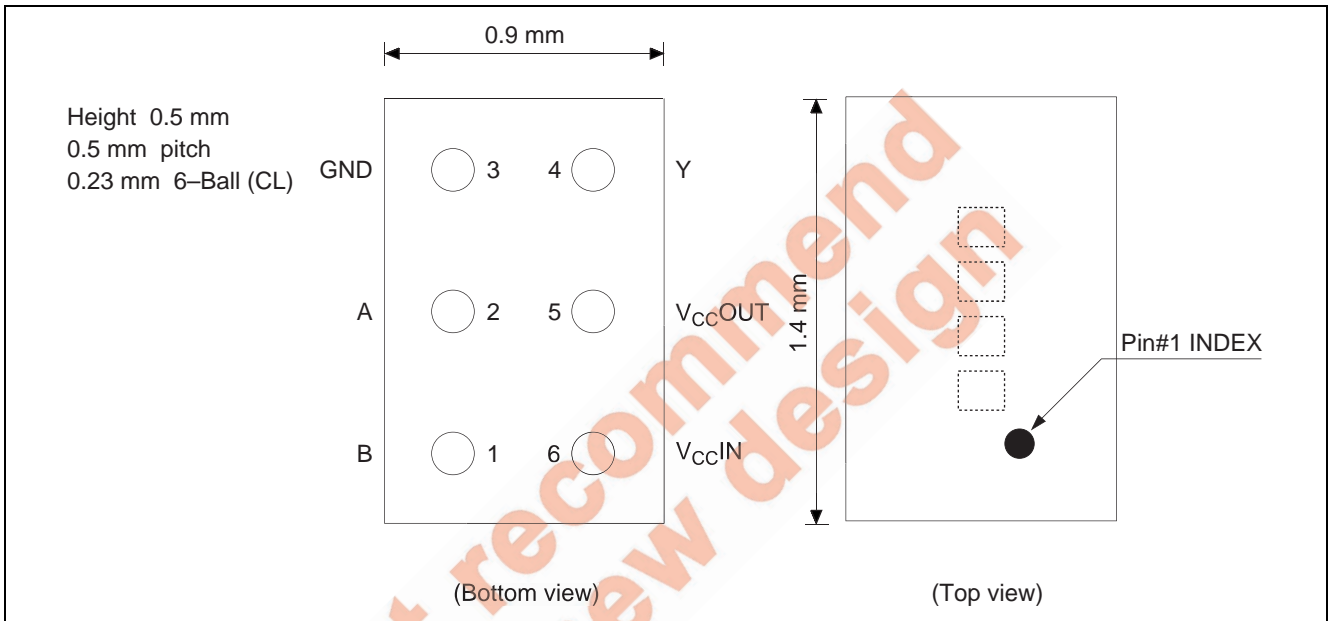


Function Table

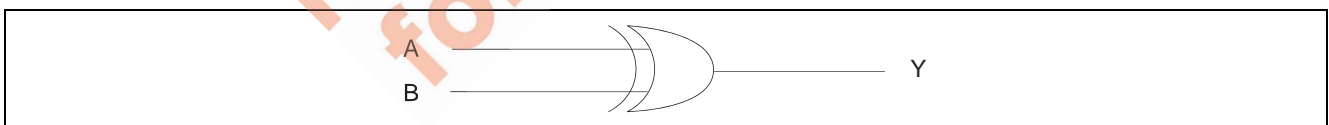
Inputs		Output Y
A	B	
L	L	L
L	H	H
H	L	H
H	H	L

H: High level
L: Low level

Pin Arrangement



Logic Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CCIN}, V_{CCOUT}	-0.5 to 4.6	V	
Input voltage range ^{*1}	V_I	-0.5 to 4.6	V	
Output voltage range ^{*1, 2}	V_O	-0.5 to $V_{CCOUT}+0.5$	V	Output: "H" or "L"
		-0.5 to 4.6		V_{CCOUT} : OFF
Input clamp current	I_{IK}	-50	mA	$V_I < 0$
Output clamp current	I_{OK}	-50	mA	$V_O < 0$
		50		$V_O > V_{CC}+0.5$
Continuous output current	I_O	± 50	mA	
Continuous output current V_{CC} or GND	$I_{CCIN}, I_{CCOUT}, I_{GND}$	± 100	mA	
Package Thermal impedance	θ_{ja}	123	$^{\circ}C/W$	
Storage temperature	Tstg	-65 to 150	$^{\circ}C$	

Notes: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

- The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- This value is limited to 4.6 V maximum.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CCIN}	1.2 to 3.6	V	
	V_{CCOUT}	1.2 to 3.6		
Input/Output voltage	V_I	0 to 3.6	V	
	V_O	0 to V_{CCOUT}	V	Output: "H" or "L"
0 to 3.6		V_{CCOUT} : OFF		
Output current	I_{OH}	-2	mA	$V_{CCOUT} = 1.2$ V
		-4		$V_{CCOUT} = 1.5 \pm 0.1$ V
		-6		$V_{CCOUT} = 1.8 \pm 0.15$ V
		-18		$V_{CCOUT} = 2.5 \pm 0.2$ V
		-24		$V_{CCOUT} = 3.3 \pm 0.3$ V
	I_{OL}	2	mA	$V_{CCOUT} = 1.2$ V
		4		$V_{CCOUT} = 1.5 \pm 0.1$ V
		6		$V_{CCOUT} = 1.8 \pm 0.15$ V
		18		$V_{CCOUT} = 2.5 \pm 0.2$ V
		24		$V_{CCOUT} = 3.3 \pm 0.3$ V
Input transition rise or fall time	$\Delta t / \Delta v$	10	ns / V	
Operation free-air temperature	Ta	-40 to 85	$^{\circ}C$	

Electrical Characteristics

(Ta = -40 to 85°C)

Item	Symbol	V _{CCIN} (V) *	V _{CCOUT} (V) *	Min	Typ	Max	Unit	Test conditions
Input voltage	V _{IH}	1.2	1.2 to 3.6	V _{CCIN} ×0.75	—	—	V	
		1.5±0.1		V _{CCIN} ×0.70	—	—		
		1.8±0.15		V _{CCIN} ×0.65	—	—		
		2.5±0.2		1.6	—	—		
		3.3±0.3		2.0	—	—		
	V _{IL}	1.2	1.2 to 3.6	—	—	V _{CCIN} ×0.25	V	
		1.5±0.1		—	—	V _{CCIN} ×0.30		
		1.8±0.15		—	—	V _{CCIN} ×0.35		
		2.5±0.2		—	—	0.7		
		3.3±0.3		—	—	0.8		
Output voltage	V _{OH}	1.2 to 3.6	1.2 to 3.6	V _{CCOUT} -0.2	—	—	V	I _{OH} = -100 μA
			1.2	0.9	—	—		I _{OH} = -2 mA
			1.5±0.1	1.1	—	—		I _{OH} = -4 mA
			1.8±0.15	1.25	—	—		I _{OH} = -6 mA
			2.5±0.2	1.7	—	—		I _{OH} = -18 mA
			3.3±0.3	2.2	—	—		I _{OH} = -24 mA
	V _{OL}	1.2 to 3.6	1.2 to 3.6	—	—	0.2	V	I _{OL} = 100 μA
			1.2	—	—	0.3		I _{OL} = 2 mA
			1.5±0.1	—	—	0.3		I _{OL} = 4 mA
			1.8±0.15	—	—	0.3		I _{OL} = 6 mA
			2.5±0.2	—	—	0.6		I _{OL} = 18 mA
			3.3±0.3	—	—	0.55		I _{OL} = 24 mA
Input current	I _{IN}	3.6	3.6	-1.0	—	1.0	μA	V _{IN} = GND or V _{CCIN}
Output leakage current	I _{OFF}	0	0	—	—	1.5	μA	V _{IN} , V _{OUT} = 0 to 3.6 V
Quiescent supply current	I _{CCIN}	1.2 to 3.6	1.2 to 3.6	-3.0	—	3.0	μA	I _{O(Y port)} = 0 V _{IN} = V _{CCIN} or GND
	I _{CCOUT}	1.2 to 3.6	1.2 to 3.6	-3.0	—	3.0		I _{O(Y port)} = 0 V _{IN} = V _{CCIN} or GND
Increase in I _{CC} per input	ΔI _{CC}	3.6	3.6	—	—	250	μA	A or B port V _{CCIN} -0.6 (1 input)
Input capacitance	C _{IN}	3.3	3.3	—	3.5	—	pF	V _{IN} = V _{CC} or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

$V_{CCIN} = 3.3 \pm 0.3 \text{ V}$

Item	Symbol	FROM (Input)	TO (Output)	Ta = -40 to 85°C								Unit	Test Conditions		
				V _{CC} OUT= 1.2V		V _{CC} OUT= 1.5±0.1V		V _{CC} OUT= 1.8±0.15V		V _{CC} OUT= 2.5±0.2V				V _{CC} OUT= 3.3±0.3V	
				Typ	Min	Max	Min	Max	Min	Max	Min			Max	Min
Propagation delay time	t _{PLH}	A or B	Y	8.6	2.0	8.4	1.5	5.8	1.0	4.4	1.0	3.9	ns	C _L = 15 pF R _L = 2.0 kΩ	
	t _{PHL}			8.6	2.0	8.4	1.5	5.8	1.0	4.4	1.0	3.9			

$V_{CCIN} = 2.5 \pm 0.2 \text{ V}$

Item	Symbol	FROM (Input)	TO (Output)	Ta = -40 to 85°C								Unit	Test Conditions		
				V _{CC} OUT= 1.2V		V _{CC} OUT= 1.5±0.1V		V _{CC} OUT= 1.8±0.15V		V _{CC} OUT= 2.5±0.2V				V _{CC} OUT= 3.3±0.3V	
				Typ	Min	Max	Min	Max	Min	Max	Min			Max	Min
Propagation delay time	t _{PLH}	A or B	Y	8.7	2.0	8.8	1.5	6.2	1.0	4.7	1.0	4.5	ns	C _L = 15 pF R _L = 2.0 kΩ	
	t _{PHL}			8.7	2.0	8.8	1.5	6.2	1.0	4.7	1.0	4.5			

$V_{CCIN} = 1.8 \pm 0.15 \text{ V}$

Item	Symbol	FROM (Input)	TO (Output)	Ta = -40 to 85°C								Unit	Test Conditions		
				V _{CC} OUT= 1.2V		V _{CC} OUT= 1.5±0.1V		V _{CC} OUT= 1.8±0.15V		V _{CC} OUT= 2.5±0.2V				V _{CC} OUT= 3.3±0.3V	
				Typ	Min	Max	Min	Max	Min	Max	Min			Max	Min
Propagation delay time	t _{PLH}	A or B	Y	9.8	2.0	9.8	1.5	7.4	1.0	6.4	1.0	6.2	ns	C _L = 15 pF R _L = 2.0 kΩ	
	t _{PHL}			9.8	2.0	9.8	1.5	7.4	1.0	6.4	1.0	6.2			

$V_{CCIN} = 1.5 \pm 0.1 \text{ V}$

Item	Symbol	FROM (Input)	TO (Output)	Ta = -40 to 85°C								Unit	Test Conditions		
				V _{CC} OUT= 1.2V		V _{CC} OUT= 1.5±0.1V		V _{CC} OUT= 1.8±0.15V		V _{CC} OUT= 2.5±0.2V				V _{CC} OUT= 3.3±0.3V	
				Typ	Min	Max	Min	Max	Min	Max	Min			Max	Min
Propagation delay time	t _{PLH}	A or B	Y	10.5	2.0	11.2	1.5	10.0	1.0	9.0	1.0	8.8	ns	C _L = 15 pF R _L = 2.0 kΩ	
	t _{PHL}			10.5	2.0	11.2	1.5	10.0	1.0	9.0	1.0	8.8			

$V_{CCIN} = 1.2 \text{ V}$

Item	Symbol	FROM (Input)	TO (Output)	Ta = -40 to 85°C					Unit	Test Conditions
				V _{CC} OUT= 1.2V	V _{CC} OUT= 1.5±0.1V	V _{CC} OUT= 1.8±0.15V	V _{CC} OUT= 2.5±0.2V	V _{CC} OUT= 3.3±0.3V		
				Typ	Typ	Typ	Typ	Typ		
Propagation delay time	t _{PLH}	A or B	Y	12.0	10.5	9.5	9.5	9.5	ns	C _L = 15 pF R _L = 2.0 kΩ
	t _{PHL}			12.0	10.5	9.5	9.5	9.5		

Operating Characteristics

Item	Symbol	V _{CC} IN (V)	V _{CC} OUT (V)	Ta = 25°C			Unit	Test Conditions
				Min	Typ	Max		
Power dissipation capacitance	C _{PD}	3.3	3.3	—	12	—	pF	f = 10 MHz C _L = 0

Power-up Considerations

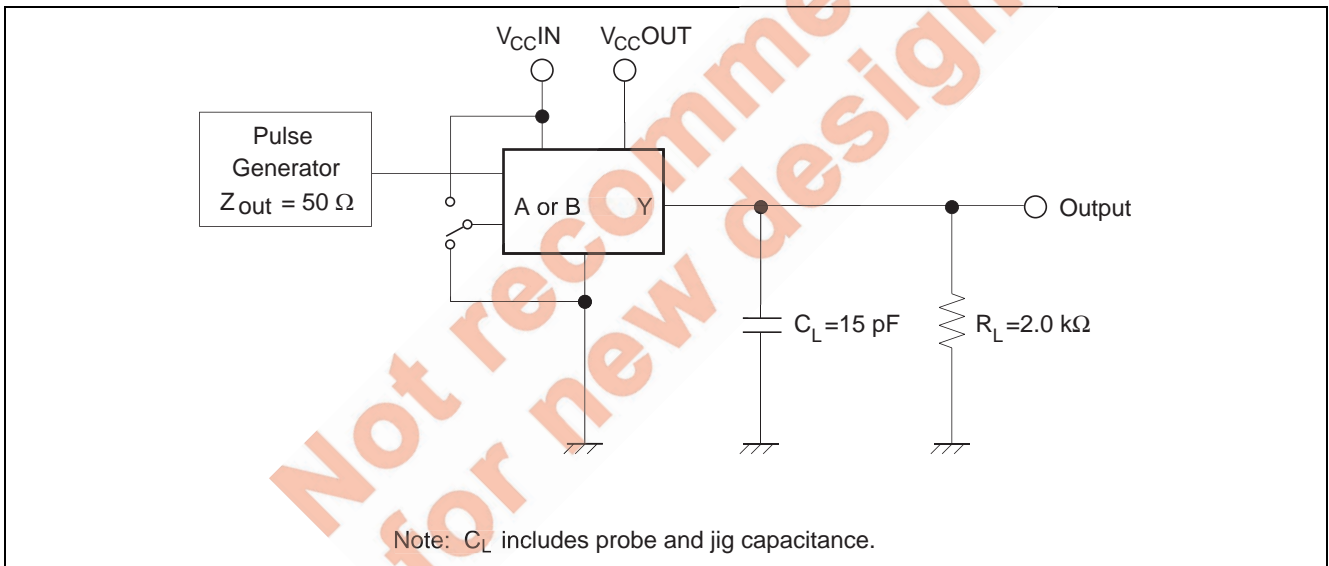
Level-translation devices offer an opportunity for successful mixed-voltage signal design.

A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device pins.

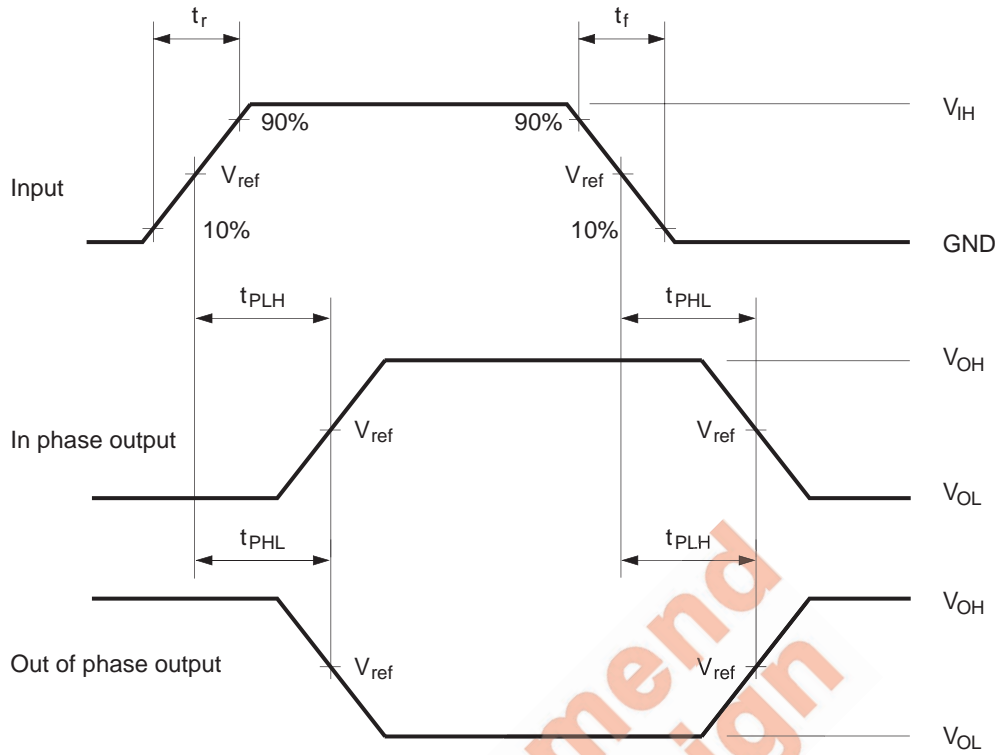
Take these precautions to guard against such power-up problems.

1. Connect ground before any supply voltage is applied.
2. Next, power up the input side of the device.
(Power up of V_{CC}IN is first. Next power up is V_{CC}OUT)

Test Circuit



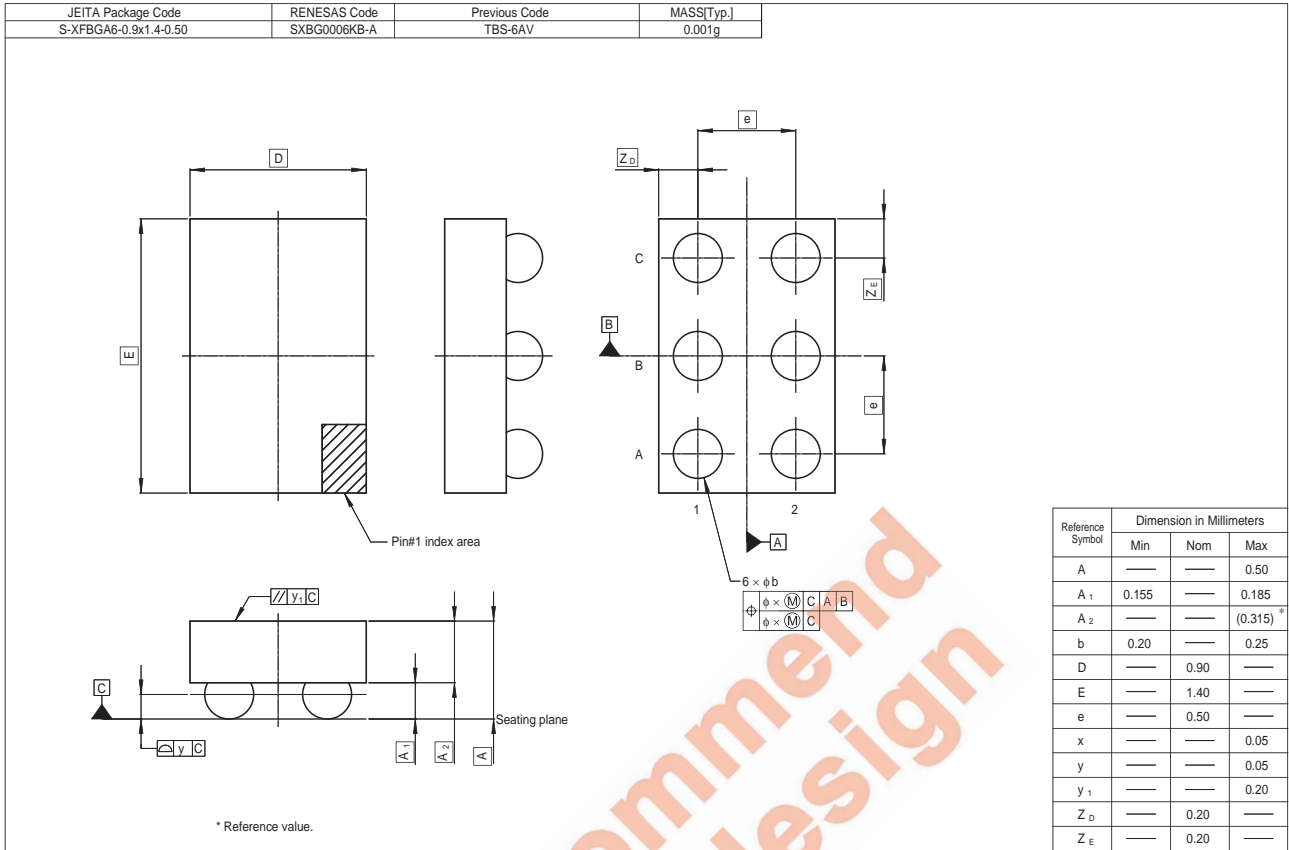
• Waveforms



Symbol	$V_{CC} = 1.2V$ to $3.6V$
t_r / t_f	2.0 ns
V_{IH}	V_{CC}
V_{ref}	$1/2 V_{CC}$

Note: Input waveform : PRR \leq 10 MHz, $Z_O = 50 \Omega$, duty cycle 50%

Package Dimensions



Not recommended for new design

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