

M62370GP

3 V Type 8-bit 36ch Selector SW Built-in D/A Converter with Buffer Amplifiers

REJ03D0879-0300 Rev.3.00 Mar 25, 2008

Description

The M62370GP is a CMOS semiconductor IC, containing 36 channels of 8-bit D/A converters. It is operable with a low supply voltage between 2.7 to 3.6 V, and is easy to use due to serial data input, and 3-pin (DI, CLK, LD) connection with microcomputer.

The IC also contains D_0 pin terminal, enabling cascade connection, and therefore is suitable for automatic control in combination with a microcomputer.

Features

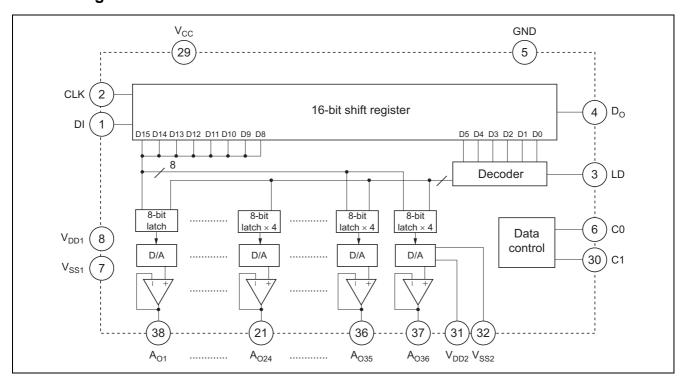
- Operable with a low voltage between 2.7 to 3.6 V
- 16-bit serial data input (connected via 3 pins: DI, CLK, LD)
- 36 channels built-in of 8-bit D/A converter
- 6 channels of D/A converters capable of selecting and outputting 4 data stored in each converter, through 2 control terminals

Application

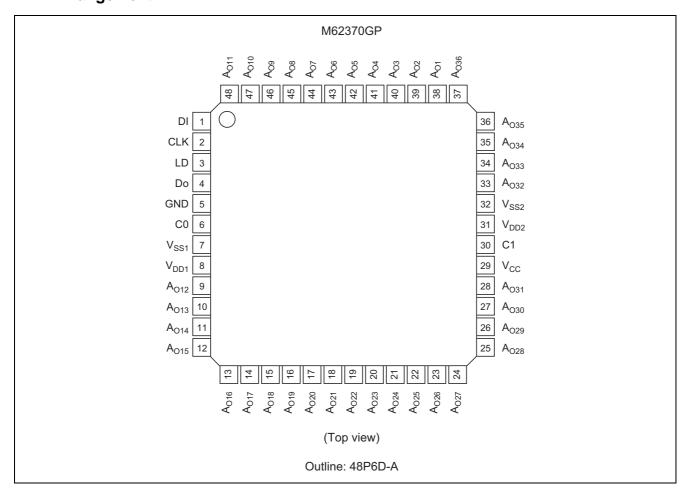
Digital/analog conversion in industrial or home-use electronic equipment.

Automatic control in combination with EEPROM and microcomputer (Substitute for conventional semi-fixed resistor).

Block Diagram



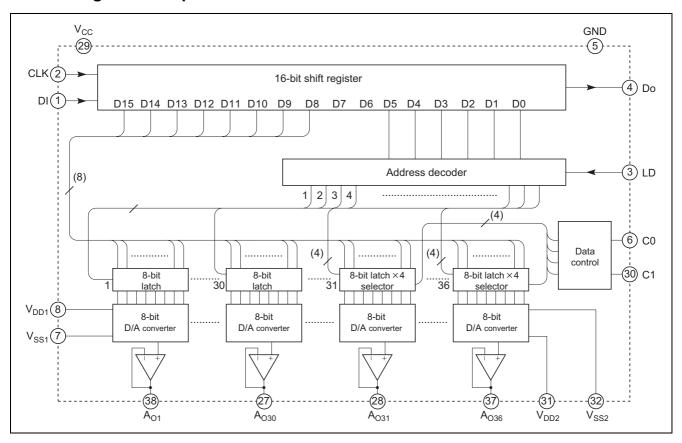
Pin Arrangement



Pin Description

Pin No.	Pin Name	Function
1	DI	Serial data input terminal to input serial data of 16-bit length
4	Do	Terminal to output MSB data of 16-bit shift register
2	CLK	Shift clock input terminal. Input signal at DI pin is input to 16-bit shift register at rise of shift clock pulse
3	LD	When H-level signal is input to this terminal, the value stored in 16-bit shift register is loaded in decoder and D/A converter output register.
38 to 48	A _{O1} to A _{O11}	8-bit D/A converter output terminal
9 to 28	A _{O12} to A _{O31}	
33 to 37	A _{O32} to A _{O36}	
29	V _{CC}	Power supply terminal
5	GND	GND terminal
6	C0	Data select signal input terminal 1 for channel No.31 through 36
30	C1	Data select signal input terminal 2 for channel No.31 through 36
8	V_{DD1}	Upper reference voltage input terminal and power supply to operational amplifier for channel No.1 through 24
7	V _{SS1}	Lower reference voltage input terminal for channel No.1 through 24
31	V_{DD2}	Upper reference voltage input terminal and power supply to operational amplifier for channel No.25 through 36
32	V _{SS2}	Lower reference voltage input terminal for channel No.25 through 36

Block Diagram for Explanation of Terminals



Absolute Maximum Ratings

(Ta = 25° C, unless otherwise noted.)

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V _{CC}	-0.3 to +7.0	V	
Upper reference voltage of D/A converter	V_{DD}	-0.3 to +7.0	V	
Input voltage	V _{IN}	-0.3 to $V_{CC} + 0.3$	V	
Output voltage	Vo	-0.3 to $V_{CC} + 0.3$	V	
Power dissipation	Pd	400	mW	
Terminal derating	Κθ	4	mW/°C	Ta ≥ 25°C
Operating temperature	Topr	-20 to +85	°C	
Storage temperature	Tstg	-40 to +125	°C	

Electrical Characteristics

<Digital Part>

(V_{CC} = +3 V \pm 10%, V_{CC} = V_{DD}, Ta = -20 to +85°C, unless otherwise noted.)

			Limits			
Item	Symbol	Min	Тур	Max	Unit	Conditions
Supply voltage	Vcc	2.7	3.0	5.5	V	
Circuit current	Icc	_	1.0	_	mA	CLK = 1 MHz operation,
						$V_{CC} = 3 \text{ V}, I_{AO} = 0 \mu\text{A}$
Input leak current	I _{ILK}	-10	_	10	μΑ	
Input low voltage	V _{IL}	_	_	0.6	V	
Input high voltage	V _{IH}	2.4	_	_	V	
Output low voltage	V _{OL}	_	_	0.4	V	I _{OL} = 2.5 mA
Output high voltage	V _{OH}	V _{CC} - 0.4	_	_	V	$I_{OH} = -400 \mu A$

Note: Standard value is at Ta = 25°C

<Analog Part>

(V_{CC} = +3 V \pm 10%, V_{CC} = V_{DD}, Ta = -20 to +85°C, unless otherwise noted.)

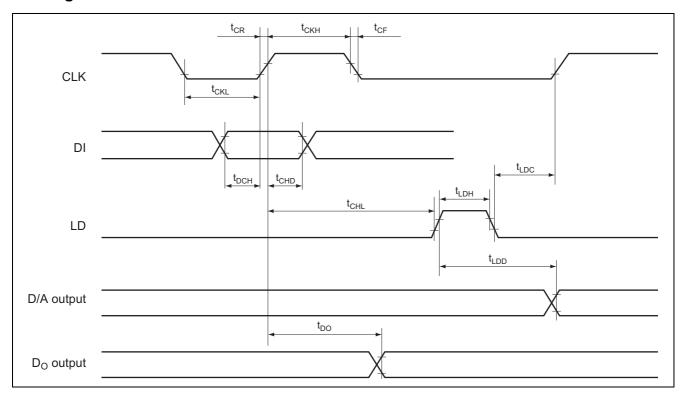
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			Limits			
Item	Symbol	Min	Тур	Max	Unit	Conditions
Current dissipation	I _{DD}	_	5.0	_	mA	
D/A converter upper	V_{DD}	2.7	3.0	5.5	V	
reference voltage range						
D/A converter lower	Vss	GND	_	V _{DD} – 2	V	
reference voltage range						
Buffer amplifier output	V _{AO}	0.1	_	$V_{DD} - 0.1$	V	$I_{AO} = \pm 100 \mu A$
voltage range		0.2	_	$V_{DD} - 0.2$	V	I _{AO} = +300 μA
						–200 μΑ
Buffer amplifier output	I _{AO}	-300	_	500	μΑ	Upper saturation voltage = 0.4 V
driving range						Lower saturation voltage = 0.3 V
Differential nonlinearity	S _{DL}	-1.0	_	1.0	LSB	V _{CC} = 2.700 V
error						$V_{DD} = 2.700 \text{ V}$
Nonlinearity error	S _L	-1.5	_	1.5	LSB	V _{SS} = 0.050 V
Zero code error	S _{ZERO}	-2	_	2	LSB	No load $(I_{AO} = \pm 0)$
Full scale error	S _{FULL}	-2	_	2	LSB	
Output capacitive load	Co	_	_	0.1	μF	
Buffer amplifier output impedance	R _O	_	50	_	Ω	

AC Characteristics

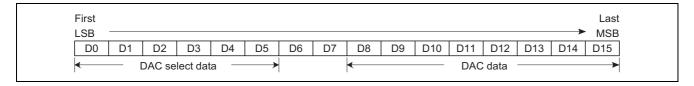
 $(V_{CC} = V_{DD}, Ta = -20 \text{ to } +85^{\circ}\text{C}, \text{ unless otherwise noted.})$

			Limits			
Item	Symbol	Min	Тур	Max	Unit	Conditions
Clock "L" pulse width	t _{CKL}	200	_	_	ns	
Clock "H" pulse width	t _{CKH}	200	_	1	ns	
Clock rise time	t _{CR}	_	_	200	ns	
Clock fall time	t _{CF}	_	_	200	ns	
Data setup time	t _{DCH}	30	_	_	ns	
Data hold time	t _{CHD}	60	_	_	ns	
LD setup time	t _{CHL}	200	_	_	ns	
LD hold time	t _{LDC}	100	_	_	ns	
LD "H" pulse duration time	t _{LDH}	100	_	_	ns	
Data output delay time	t _{DO}	70	_	350	ns	C _L = 100 pF
D/A converter output setting	t _{LDD}	_	_	100	μS	$C_L \le 100 \text{ pF}, \text{ V}_{AO}: 0.3 \leftrightarrow 2.7 \text{ V}$
time						This time until the output becomes the final value of ±2 LSB

Timing Chart



Digital Data Format



DAC Data

D8	D9	D10	D11	D12	D13	D14	D15	D/A Output
0	0	0	0	0	0	0	0	(VrefU – VrefL) / 256 × 1 + VrefL
1	0	0	0	0	0	0	0	(VrefU – VrefL) / 256 × 2 + VrefL
0	1	0	0	0	0	0	0	(VrefU – VrefL) / 256 × 3 + VrefL
1	1	0	0	0	0	0	0	(VrefU – VrefL) / 256 × 4 + VrefL
:	:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	1	(VrefU – VrefL) / 256 × 255 + VrefL
1	1	1	1	1	1	1	1	VrefU

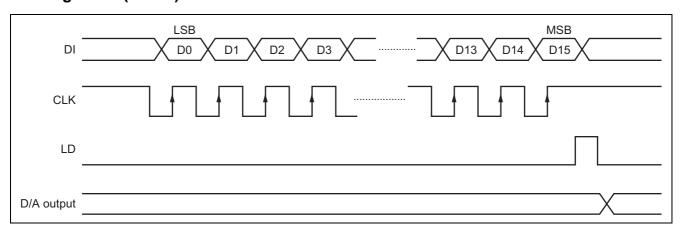
Note: $VrefU = V_{DD1}, V_{DD2}, VrefL = V_{SS1}, V_{SS2}$

DAC Select Data

D5	D4	D3	D2	D1	D0	DAC Selection
0	0	0	0	0	0	Don't care
0	0	0	0	0	1	A _{O1} selection
0	0	0	0	1	0	A _{O2} selection
:	:	• •	:	:	:	:
0	1	1	1	1	0	A _{O30} selection
0	1	1	1	1	1	A _{O31 (0)} selection
1	0	0	0	0	0	A _{O32 (0)} selection
:	:	• •	:	:	:	:
1	0	0	1	0	0	A _{O36 (0)} selection
1	0	0	1	0	1	A _{O31 (1)} selection
:	:	• •	:	:	:	:
1	0	1	0	1	0	A _{O36 (1)} selection
1	0	1	0	1	1	A _{O31 (2)} selection
:	:	• •	:	:	:	:
1	1	0	0	0	0	A _{O36 (2)} selection
1	1	0	0	0	1	A _{O31 (3)} selection
:	:	:			:	:
1	1	0	1	1	0	A _{O36 (3)} selection
1	1	0	1	1	1	Don't care
:	:	:			:	:
1	1	1	1	1	1	Don't care

CO	C1	A _{O31} Through A _{O36} Data Selected
0	0	Address 0 selected
0	1	Address 1 selected
1	0	Address 2 selected
1	1	Address 3 selected

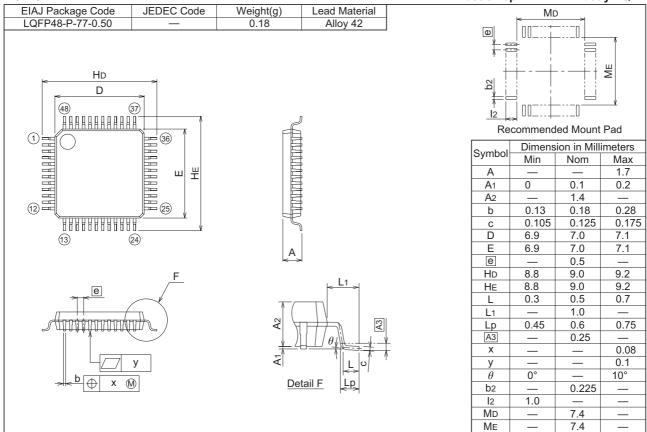
Timing Chart (Model)



Package Dimensions

48P6D-A

Plastic 48pin $7 \times 7mm$ body LQFP



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