

Silicon NPN Power Transistors

2SC2122

DESCRIPTION

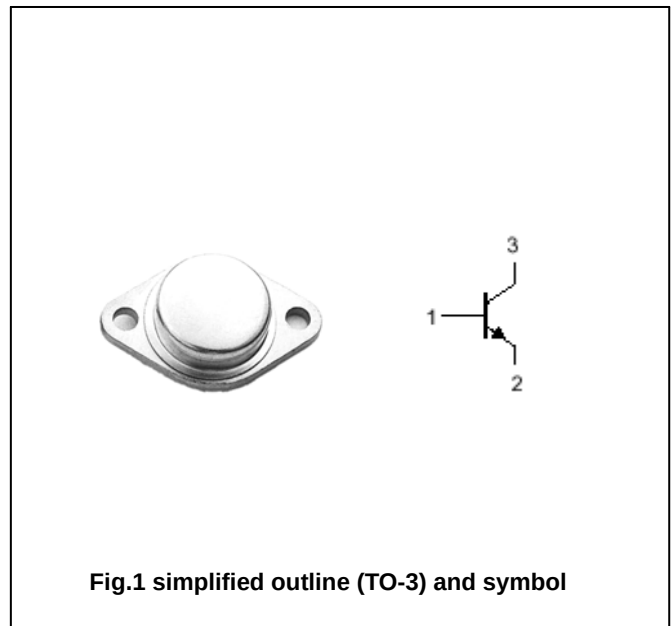
- With TO-3 package
- Short switching times.
- High dielectric strength.

APPLICATIONS

- For use in TV horizontal deflection stage

PINNING(see fig.2)

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

Absolute maximum ratings($T_a = ^\circ\text{C}$)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	800	V
V_{CEO}	Collector-emitter voltage	Open base	325	V
V_{EBO}	Emitter-base voltage	Open collector	7	V
I_C	Collector current		10	A
P_T	Total power dissipation	$T_C = 25^\circ\text{C}$	50	W
T_j	Junction temperature		175	$^\circ\text{C}$
T_{stg}	Storage temperature		-55~175	$^\circ\text{C}$

Silicon NPN Power Transistors**2SC2122****CHARACTERISTICS**T_j=25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =50mA; I _B =0;	325			V
V _{(BR)EBO}	Emitter-base breakdown voltage	I _E =1mA; I _C =0;	7			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =8A; I _B =2.5 A			3.3	V
V _{BEsat}	Base-emitter saturation voltage	I _C =8A; I _B =2.5 A			2.2	V
I _{CBO}	Collector cut-off current	V _{CB} =800V; I _E =0			1.0	mA
I _{EBO}	Emitter cut-off current	V _{EB} =7V; I _C =0			1.0	mA
h _{FE}	DC current gain	I _C =2.5A ; V _{CE} =10V	15			
f _T	Transition frequency	I _C =0.1A ; V _{CE} =10V		6		MHz

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PACKAGE OUTLINE

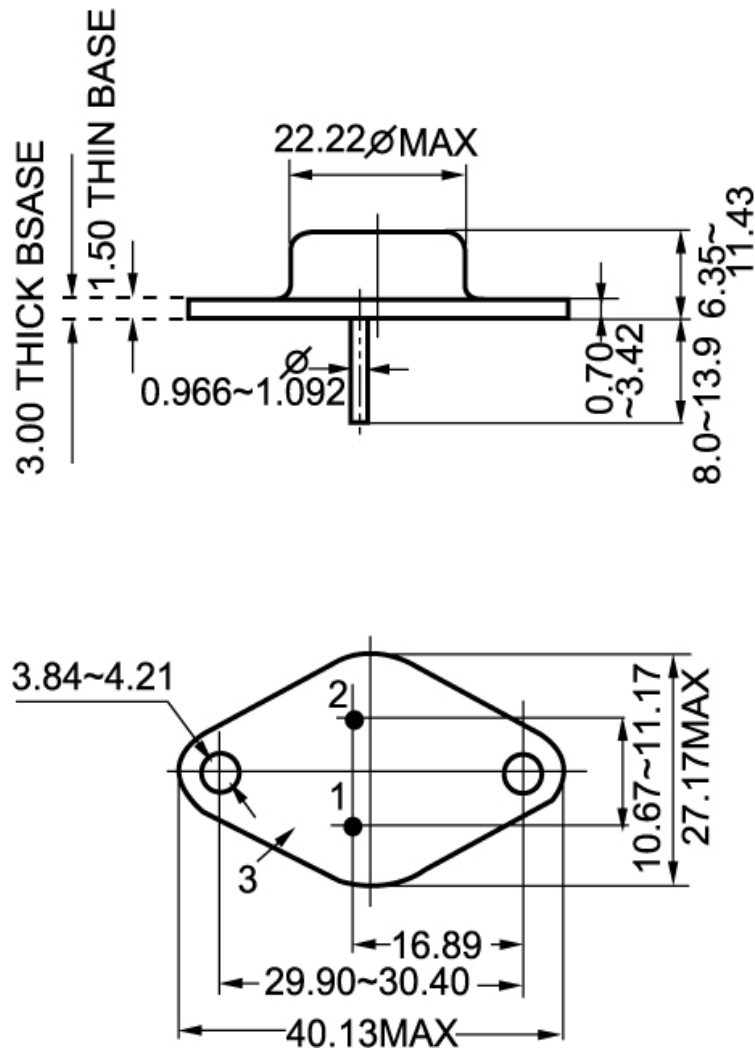


Fig.2 Outline dimensions