TOSHIBA Diode Silicon Epitaxial Planar Type

HN2D01FU

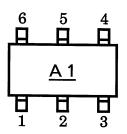
Ultra High Speed Switching Application

• HN2D01FU is composed of 3 independent diodes.

Pin Assignment (Top View)

$\begin{array}{c|c} 6 & 5 & 4 \\ \hline \end{array}$ $\begin{array}{c|c} Q1 & Q3 \\ \hline \end{array}$

Marking



Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Maximum (peak) reverse Voltage	V_{RM}	85	V
Reverse voltage	V _R	80	V
Maximum (peak) forward current	I _{FM}	240 *	mA
Average forward current	Io	80 *	mA
Surge current (10ms)	I _{FSM}	1 *	Α
Power dissipation	Р	200	mW
Junction temperature	Tj	125	°C
Storage temperature	T _{stg}	−55~125	°C

2.1±0.1 2.1±0.1 1. CATHODE 2. CATHODE 3. CATHODE 4. ANODE 5. ANODE 6. ANODE DEDEC EIAJ TOSHIBA 1-2T1C

Weight: 6.2mg

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

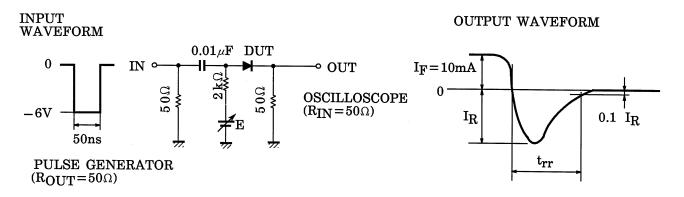
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

*: This is absolute maximum rating of single diode (Q1 or Q2 or Q3). In the case of using 2 ro 3 diodes, the absolute maximum ratings per diodes is 75 % of the single diode one.

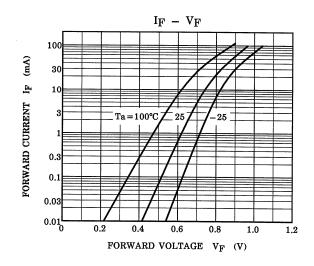
Electrical Characteristics (Q1 Q2 Q3 Common, Ta = 25°C)

Characteristic	Symbol	Test Circuit	Test Condition	Min	Тур.	Max	Unit
Forward voltage	V _{F (1)}	_	I _F = 1mA	_	0.62	_	٧
	V _{F (2)}	_	I _F = 10mA	_	0.75	_	
	V _{F (3)}	_	I _F = 100mA	_	0.98	1.20	
Reverse current	I _{R (1)}	_	V _R = 30V	_	_	0.1	μΑ
	I _{R (2)}	_	V _R = 80V	_	_	0.5	
Total capacitance	СТ	_	V _R = 0, f = 1MH _z	_	0.5	3.0	pF
Reverse recovery time	t _{rr}	_	I _F = 10mA (Fig.1)	_	1.6	4.0	ns

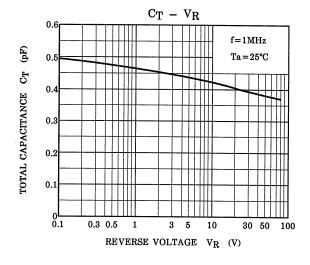
Fig.1 Reverse Recovery Time (trr) Test Circuit



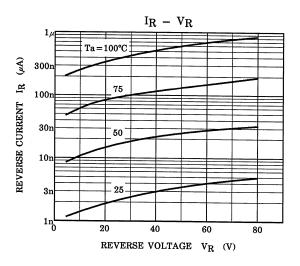
Q1, Q2, Q3 Common



Q1, Q2, Q3 Common



Q1, Q2, Q3 Common



3

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20070701-EN GENERAL

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