



Accutek Microcircuit Corporation

AK632256BZ 262,144 x 32 Bit CMOS/BiCMOS Static Random Access Memory

DESCRIPTION

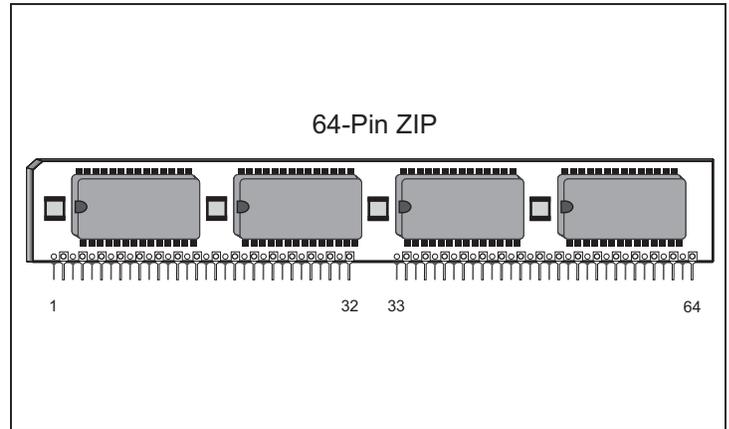
The Accutek AK632256BZ SRAM Module consists of fast high performance SRAMs mounted on a low profile, 64 pin SIM or ZIP Board. The module utilizes four 28 pin 256K x 4 SRAMs in 300 mil SOJ packages and four decoupling capacitor chips mounted on each side of a printed circuit board.

The SRAMs used have common I/O functions and single output enable functions. Also, four separate chip select (\overline{CE}) connections are used to independently enable the four bytes. The modules can be supplied in a variety of access time values from 12 nSEC to 45 nSEC in CMOS or BiCMOS technology.

The Accutek module is designed to have a maximum seated height of 0.500 inch to provide for the lowest height off the board. The modules conform to JEDEC standard sizes and pin-out configurations. Using two pins for module memory density identification, PD₀ and PD₁, minimizes interchangeability and design considerations when changing from one module size to another in customer applications.

FEATURES

- 262,144 x 32 bit organization
- JEDEC Standardized 64 pin SIM format
- Presence Detect PD₀ and PD₁ for identifying module density
- Common I/O, single \overline{OE} functions with four separate chip selects (\overline{CE})
- Low height 0.500 inch maximum
- Downward compatible with 128K x 32 (AK632128), 64K x 32 (AK63264) and 32K x 32 (AK63232)
- TTL-compatible inputs and outputs



- Upward compatible with 512K x 32 (AK632512) and 1 Meg x 32 (AK6321024)
- Fast access times range from 12 nSEC BiCMOS to 45 nSEC CMOS
- TTL-compatible inputs and outputs
- Single 5 volt power supply - AK632256BZ
- Single 3.3 volt power supply - AK632256BZ/3.3
- Operating temperature range in free air, 0°C to 70°C

ELECTRICAL SPECIFICATIONS

Timing diagrams and basic electrical characteristics are those of the standard 256K x 4 SRAMs used to construct these modules. Accutek's module design allows the flexibility of selecting industry-compatible 256K x 4 SRAMs from several semiconductor manufacturers.

PIN NOMENCLATURE

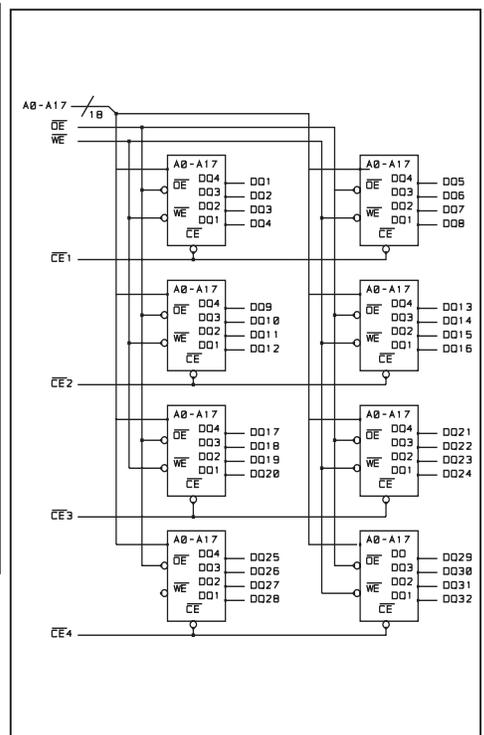
A ₀ - A ₁₇	Address Inputs
\overline{CE}_1 - \overline{CE}_4	Chip Enable
DQ ₁ - DQ ₃₂	Data In/Data Out
\overline{OE}	Output Enable
PD ₀ - PD ₁	Presence Detect
V _{cc}	5v Supply
V _{ss}	Ground
\overline{WE}	Write Enable

PIN ASSIGNMENT

PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	V _{ss}	17	A ₂	33	\overline{CE}_4	49	A ₄
2	PD ₀	18	A ₉	34	\overline{CE}_3	50	A ₁₁
3	PD ₁	19	DQ ₁₃	35	A ₁₇	51	A ₅
4	DQ ₁	20	DQ ₅	36	A ₁₆	52	A ₁₂
5	DQ ₉	21	DQ ₁₄	37	\overline{OE}	53	V _{cc}
6	DQ ₂	22	DQ ₆	38	V _{ss}	54	A ₁₃
7	DQ ₁₀	23	DQ ₁₅	39	DQ ₂₅	55	A ₆
8	DQ ₃	24	DQ ₇	40	DQ ₁₇	56	DQ ₂₁
9	DQ ₁₁	25	DQ ₁₆	41	DQ ₂₆	57	DQ ₂₉
10	DQ ₄	26	DQ ₈	42	DQ ₁₈	58	DQ ₂₂
11	DQ ₁₂	27	V _{ss}	43	DQ ₂₇	59	DQ ₃₀
12	V _{cc}	28	\overline{WE}	44	DQ ₁₉	60	DQ ₂₃
13	A ₀	29	A ₁₅	45	DQ ₂₈	61	DQ ₃₁
14	A ₇	30	A ₁₄	46	DQ ₂₀	62	DQ ₂₄
15	A ₁	31	\overline{CE}_2	47	A ₃	63	DQ ₃₂
16	A ₈	32	\overline{CE}_1	48	A ₁₀	64	V _{ss}

PD₀ = V_{ss}
PD₁ = V_{ss}

FUNCTIONAL DIAGRAM



MODULE OPTIONS

Leaded ZIP: AK632256BZ

