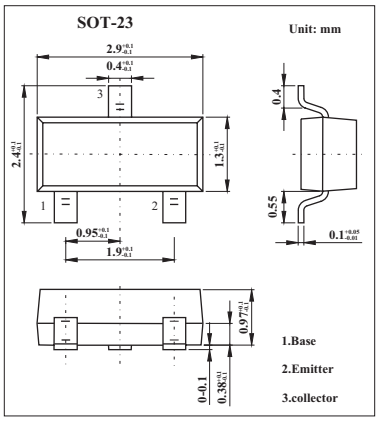
PNP Epitaxial Planar Silicon Transistor

2SA1434

Features

- Adoption of FBET process.
- High DC current gain (h_{FE}=500 to 1200).
- Low collector-to-emitter saturation voltage ($V_{CE}(sat) \leqslant 0.5V$).
- High V_{EBO} ($V_{EBO} \geqslant 15V$).



Absolute Maximum Ratings Ta = 25℃

Parameter	Symbol	Rating	Unit
Collector-base voltage	V_{CBO}	-60	V
Collector-emitter voltage	V_{CEO}	-50	V
Emitter-base voltage	V_{EBO}	-15	V
Collector current	I_C	-100	mA
Collector current (pulse)	I_{cp}	-200	mA
Collector dissipation	P_C	200	mW
Junction temperature	T_j	125	℃
Storage temperature	T_{stg}	-55 to +125	℃

Electrical Characteristics Ta = 25℃

Parameter	Symbol	Testconditons	Min	Typ	Max	Unit
Collector cutoff current	I_{CBO}	V_{CB} = -40V, I_E=0			-0.1	μA
Emitter cutoff current	I_{EBO}	V_{EB} = -10V, I_C=0			-0.1	μA
DC current gain	h_{FE}	V_{CE} = -5V , I_C = -10mA	500	800	1200	
Gain bandwidth product	f_T	V_{CE} = -10V , I_C = -10mA		100		MHz
Output capacitance	C_{ob}	V_{CB} = -10V , f = 1.0MHz		4.8		pF
Collector-emitter saturation voltage	$V_{CE(sat)}$	I_C = -50mA , I_B = -1mA		-0.2	-0.5	V
Base-emitter saturation voltage	$V_{BE(sat)}$	I_C = -10μA , I_B = -1mA		-0.8	-1.1	V
Collector-base breakdown voltage	$V_{(BR)CBO}$	I_C = -10μA , I_E = 0	-60			V
Collector-emitter breakdown voltage	$V_{(BR)CEO}$	I_C = -1mA , R_{BE} = ∞	-50			V
Emitter-base breakdown voltage	$V_{(BR)EBO}$	I_E = -10μA , I_C = 0	-15			V

Marking

Marking	FL