September 2008

FAN2108 — TinyBuck™
3-24V Input, 8A, High-Efficiency, Integrated Synchronous Buck Regulator

Features

- Wide Input Voltage Range: 3V-24V
- Wide Output Voltage Range: 0.8V to 80% V_{IN}
- 8A Output Current
- Programmable Frequency Operation: 200KHz to 600KHz
- Over 95% Peak Efficiency
- Integrated Schottky Diode on Low-side MOSFET Boosts Efficiency
- Internal Bootstrap diode
- Power-Good Signal
- Pre-Bias Startup
- Accepts Ceramic Capacitors on Output
- External Compensation for Flexible Design
- Input Under-Voltage Lockout
- Programmable Current Limit
- Under-Voltage, Over-Voltage, and Thermal Shutdown Protections
- Internal Soft-Start
- 5x6mm, 25-Pin, 3-Pad MLP Package

Applications

- Servers
- Point-of-Load Regulation
- High-End Computing Systems
- Graphics Cards
- Battery-Powered Equipment
- Set-Top Boxes

Description

The FAN2108 TinyBuck™ is a highly efficient, small footprint, 8A, synchronous buck regulator.

The FAN2108 contains both synchronous MOSFETs and a controller/driver with optimized interconnects in one package, which enables designers to solve high-current requirements in a small area with minimal external components.

External compensation, programmable switching frequency, and current limit features allow design optimization and flexibility.

The summing current mode modulator uses lossless current sensing for current feedback and over-current protection. Voltage feedforward helps operation over a wide input voltage range.

Fairchild's advanced BiCMOS power process, combined with low-$R_{DS(ON)}$ internal MOSFETs and a thermally efficient MLP package, provide the ability to dissipate high power in a small package.

Output over-voltage, under-voltage, and thermal shutdown protections help protect the device from damage during fault conditions. FAN2108 prevents pre-biased output discharge during startup in point-of-load applications.

Ordering Information

Part Number	Operating Temperature Range	Package	Eco Status	Packing Method
FAN2108MPX	-10°C to 85°C	Molded Leadless Package (MLP) 5x6mm	Green	Tape and Reel
FAN2108EMPX	-40°C to 85°C	Molded Leadless Package (MLP) 5x6mm	Green	Tape and Reel

For Fairchild's definition of "green" Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Typical Application

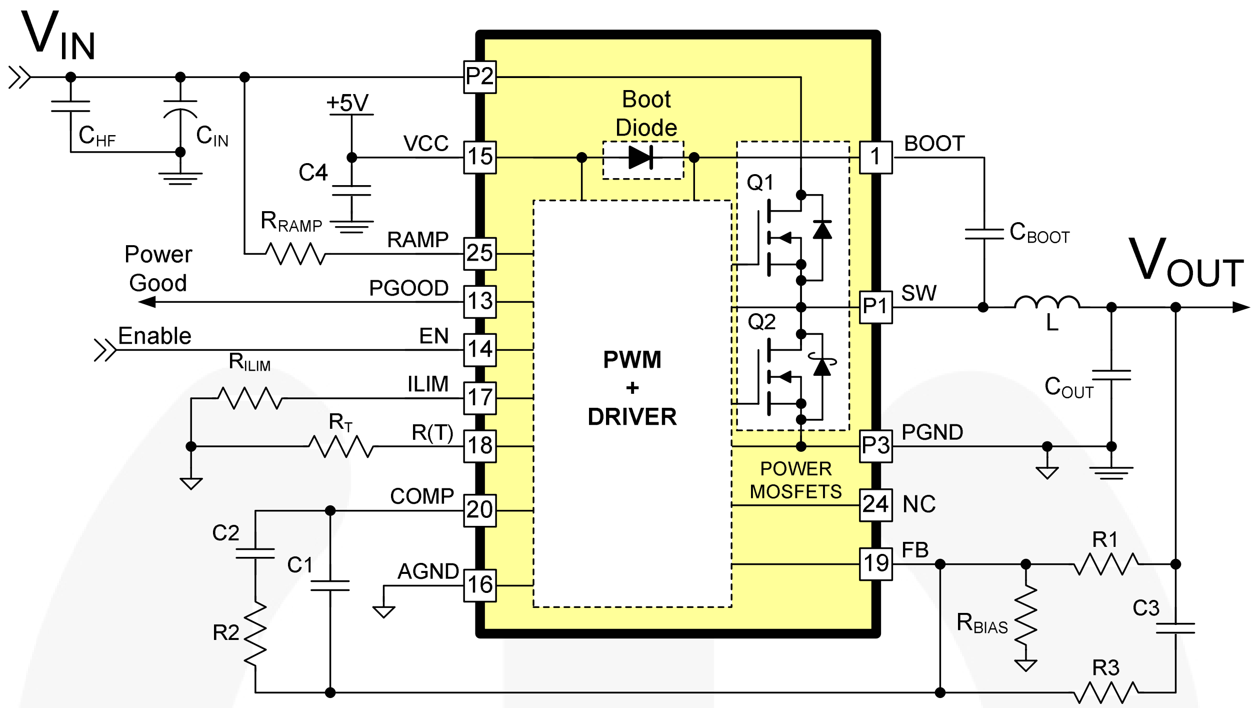

Figure 1. Typical Application Diagram

Block Diagram

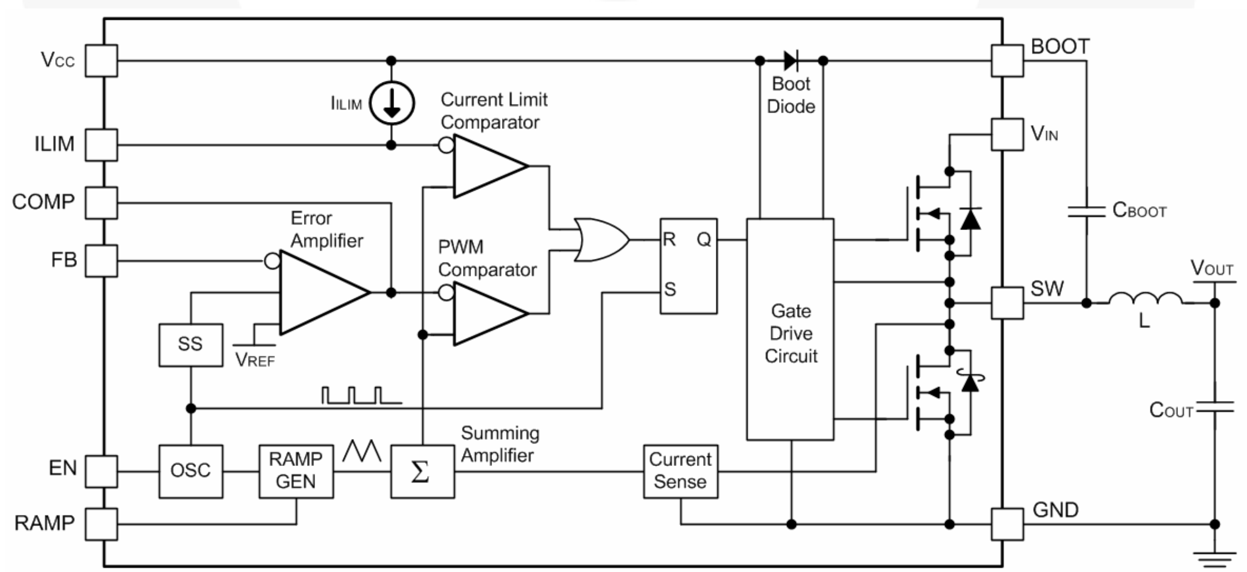

Figure 2. Block Diagram

Pin Configuration

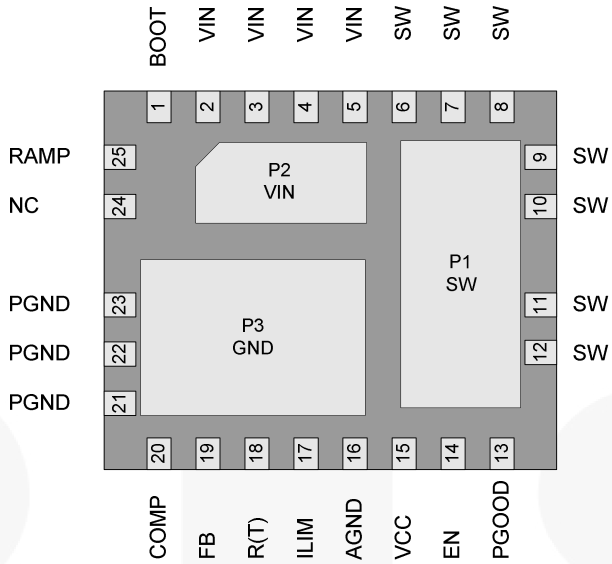

Figure 3. MLP 5x6mm Pin Configuration (Bottom View)

Pin Definitions

Pin #	Name	Description
P1, 6-12	SW	**Switching Node**.
P2, 2-5	VIN	**Power Input Voltage**. Connect to the main input power source.
P3, 21-23	PGND	**Power Ground**. Power return and Q2 source.
1	BOOT	**High-Side Drive BOOT Voltage**. Connect through capacitor (C_{BOOT}) to SW. The IC includes an internal synchronous bootstrap diode to recharge the capacitor on this pin to V_{CC} when SW is LOW.
13	PGOOD	**Power-Good Flag**. An open-drain output that pulls LOW when FB is outside a ±10% range of the reference. PGOOD does not assert HIGH until the fault latch is enabled.
14	EN	**ENABLE**. Enables operation when pulled to logic HIGH or left open. Toggling EN resets the regulator after a latched fault condition. This input has an internal pull-up when the IC is functioning normally. When a latched fault occurs, EN is discharged by a current sink.
15	VCC	**Input Bias Supply for IC**. The IC's logic and analog circuitry are powered from this pin.
16	AGND	**Analog Ground**. The signal ground for the IC. All internal control voltages are referred to this pin. Tie this pin to the ground island/plane through the lowest impedance connection.
17	ILIM	**Current Limit**. A resistor (R_{ILIM}) from this pin to AGND can be used to program the current-limit trip threshold lower than the default setting.
18	R(T)	**Oscillator Frequency**. A resistor (R_T) from this pin to AGND sets the PWM switching frequency.
19	FB	**Output Voltage Feedback**. Connect through a resistor divider to the output voltage.
20	COMP	**Compensation**. Error amplifier output. Connect the external compensation network between this pin and FB.
24	NC	**No Connect**. This pin is not used.
25	RAMP	**Ramp Amplitude**. A resistor (R_{RAMP}) connected from this pin to V_{IN} sets the ramp amplitude and provides voltage feedforward functionality.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Parameter	Conditions	Min.	Max.	Unit
VIN to PGND			28	V
VCC to AGND	AGND=PGND		6	V
BOOT to PGND			35	V
BOOT to SW		-0.3	6.0	V
SW to PGND	Continuous	-0.5	24.0	V
	Transient (t < 20ns, f ≤ 600KHz)	-5	30	V
All other pins		-0.3	V_{CC}+0.3	V
ESD	Human Body Model, JEDEC JESD22-A114	2		kV
	Charged Device Model, JEDEC JESD22-C101	2.5		

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Bias Voltage	VCC to AGND	4.5	5.0	5.5	V
V_{IN}	Supply Voltage	VIN to PGND	3		24	V
T_A	Ambient Temperature	FAN2108MPX	-10		+85	°C
		FAN2108EMPX	-40		+85	°C
T_J	Junction Temperature				+125	°C
f	Switching Frequency				600	kHz

Thermal Information

Symbol	Parameter		Min.	Typ.	Max.	Unit
T_{STG}	Storage Temperature		-65		+150	°C
T_L	Lead Soldering Temperature, 10 Seconds				+300	°C
T_{VP}	Vapor Phase, 60 Seconds				+215	°C
T_I	Infrared, 15 Seconds				+220	°C
θ_{JC}	Thermal Resistance: Junction-to-Case	P1 (Q2)		4		°C/W
		P2 (Q1)		7		°C/W
		P3		4		°C/W
$\theta_{J\text{-}PCB}$	Thermal Resistance: Junction-to-Mounting Surface[(1)]			35		°C/W
P_D	Power Dissipation, T_A=25°C[(1)]				2.8	W

Note:
1. Typical thermal resistance when mounted on a four-layer, two-ounce PCB, as shown in Figure 24. Actual results are dependent on mounting method and surface related to the design.

Electrical Specifications

Electrical specifications are the result of using the circuit shown in Figure 1 unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power Supplies						
I_{CC}	V_{CC} Current	SW=Open, FB=0.7V, V_{CC}=5V, f_{SW}=600KHz		8	12	mA
		Shutdown: EN=0, V_{CC}=5V		7	10	µA
V_{UVLO}	V_{CC} UVLO Threshold	Rising V_{CC}	4.1	4.3	4.5	V
		Hysteresis		300		mV
Oscillator						
f	Frequency	R_T=50KΩ	255	300	345	KHz
		R_T=24KΩ	540	600	660	KHz
t_{ON}	Minimum On-Time(2)			50	65	ns
V_{RAMP}	Ramp Amplitude, peak-to–peak	$16V_{IN}$, $1.8V_{OUT}$, R_T=30KΩ, R_{RAMP}=200KΩ		0.53		V
t_{OFF}	Minimum Off-Time(2)			100	150	ns
Reference						
V_{FB}	Reference Voltage *(see Figure 4 for Temperature Coefficient)*	FAN2108MPX, 25°C	794	800	806	mV
		FAN2108EMPX, 25°C	795	800	805	mV
Error Amplifier						
G	DC Gain(2)	V_{CC}=5V	80	85		dB
BW	Gain Bandwidth Product(2)	V_{CC}=5V	12	15		MHz
V_{COMP}	Output Voltage	V_{CC}=5V	0.4		3.2	V
I_{SINK}	Output Current, Sourcing	V_{CC}=5V, V_{COMP}=2.2V	1.5	2.2		mA
I_{SOURCE}	Output Current, Sinking	V_{CC}=5V, V_{COMP}=1.2V	0.8	1.2		mA
I_{BIAS}	FB Bias Current	V_{FB}=0.8V, 25°C	-850	-650	-450	nA
Protection and Shutdown						
I_{LIM}	Current Limit	R_{ILIM} Open at 25°C *(see Circuit Description)*	12	15	18	A
I_{ILIM}	I_{LIM} Current		-11	-10	-9	µA
T_{TSD}	Over-Temperature Shutdown	Internal IC Temperature		+155		°C
T_{HYS}	Over-Temperature Hysteresis	Internal IC Temperature		+30		°C
V_{OVP}	Over-Voltage Threshold	Two Consecutive Clock Cycles	110	115	121	$\%V_{OUT}$
V_{UVLO}	Under-Voltage Shutdown	16 Consecutive Clock Cycles	68	73	78	$\%V_{OUT}$
V_{FLT}	Fault Discharge Threshold	Measured at FB Pin		250		mV
V_{FLT_HYS}	Fault Discharge Hysteresis	Measured at FB Pin (V_{FB} ~500mV)		250		mV
Soft-Start						
t_{SS}	V_{OUT} to Regulation (T0.8)	Frequency=600KHz		5.3		ms
t_{EN}	Fault Enable/SSOK (T1.0)	Frequency=600KHz		6.7		ms

Note:
2. Specifications guaranteed by design and characterization; not production tested.

Electrical Specifications (Continued)

Recommended operating conditions are the result of using the circuit shown in Figure 1 unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Control Functions						
V_{EN_R}	EN Threshold, Rising			1.35	2.00	V
V_{EN_HYS}	EN Hysteresis			250		mV
R_{EN}	EN Pull-Up Resistance			800		KΩ
I_{EN}	EN Discharge Current	Auto-Restart Mode		1		µA
R_{FB}	FB OK Drive Resistance				800	Ω
V_{PG}	PGOOD Threshold	FB < V_{REF}	-14	-11	-8	%V_{REF}
		FB > V_{REF}	+7	+10	+13.5	
V_{PG_L}	PGOOD Output Low	$I_{OUT} \leq 2mA$			0.4	V

Typical Characteristics

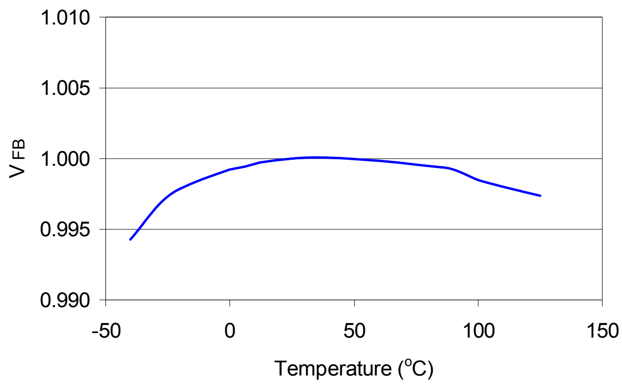

Figure 4. Reference Voltage (V_{FB}) vs. Temperature, Normalized

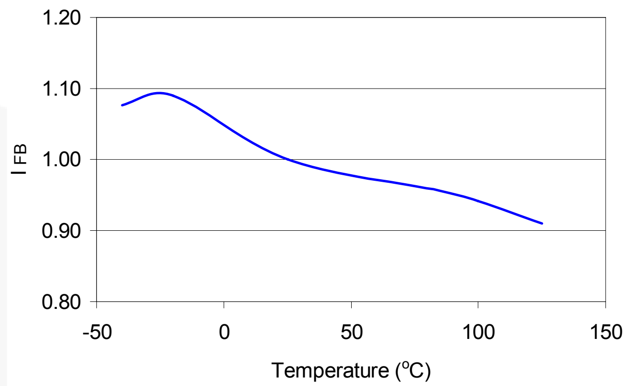

Figure 5. Reference Bias Current (I_{FB}) vs. Temperature, Normalized

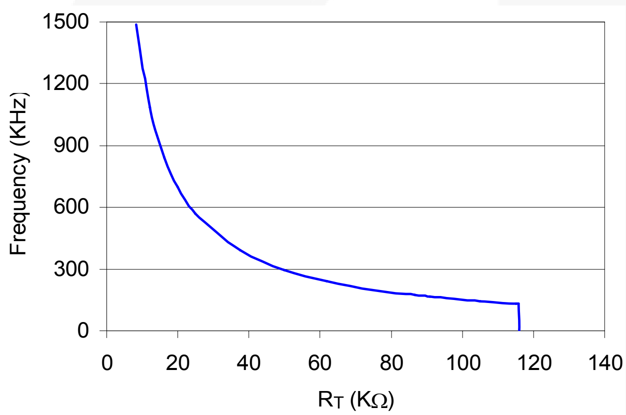

Figure 6. Frequency vs. R_T

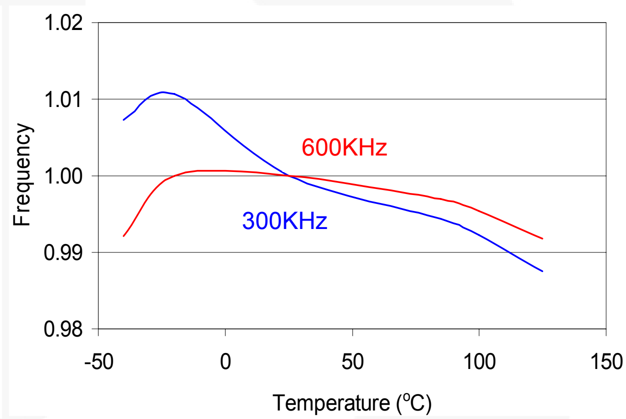

Figure 7. Frequency vs. Temperature, Normalized

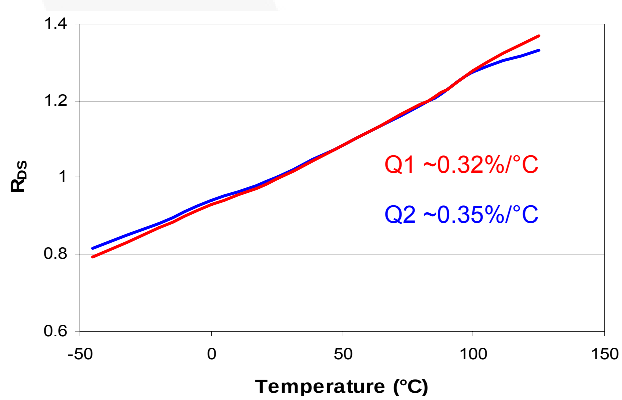

Figure 8. R_{DS} vs. Temperature, Normalized (V_{CC}=V_{GS}=5V)

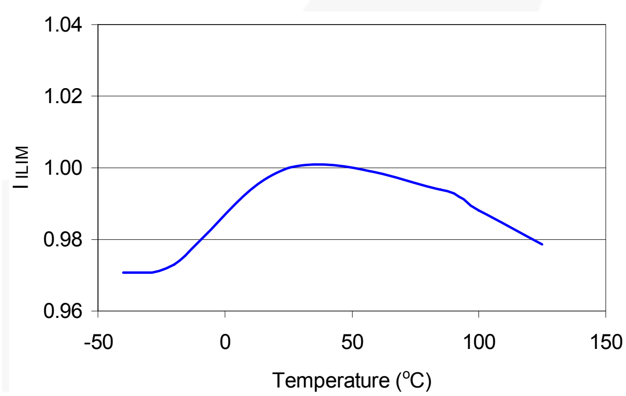

Figure 9. ILIM Current (I_{ILIM}) vs. Temperature, Normalized

Application Circuit

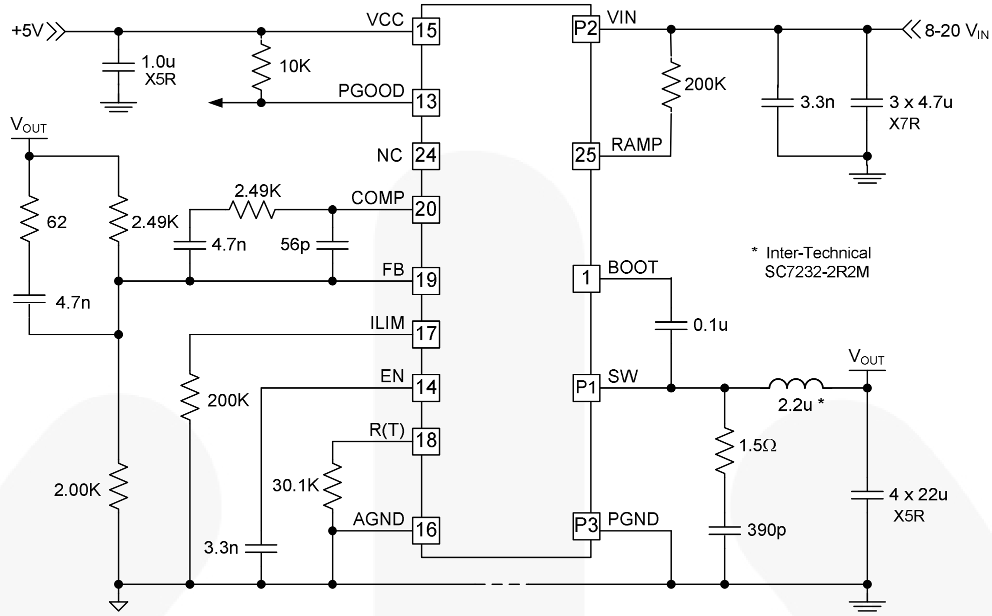

Figure 10. Application Circuit: 1.8V_{OUT}, 500KHz

Typical Performance Characteristics

Typical operating characteristics using the circuit shown in Figure 10. V_{IN}=12V, V_{CC}=5V, unless otherwise specified.

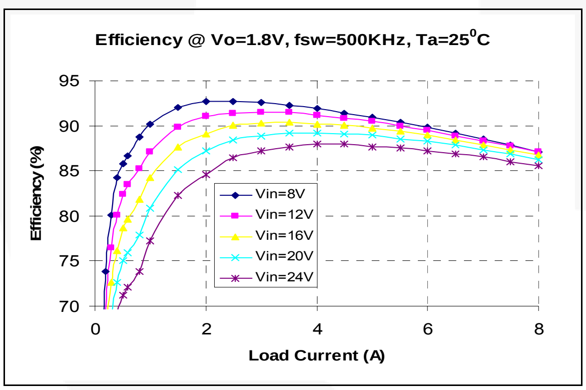

Figure 11. 1.8V_{OUT} Efficiency Over V_{IN} vs. Load

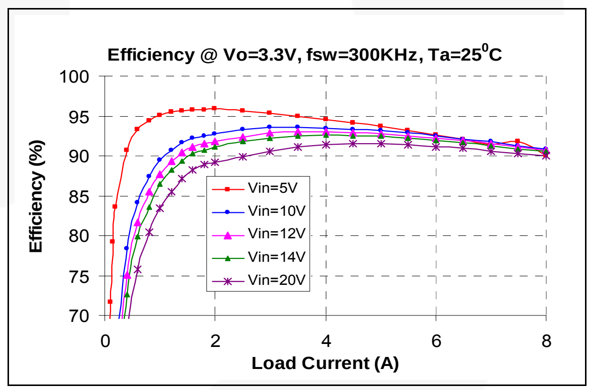

Figure 12. 3.3V_{OUT} Efficiency Over V_{IN} vs. Load

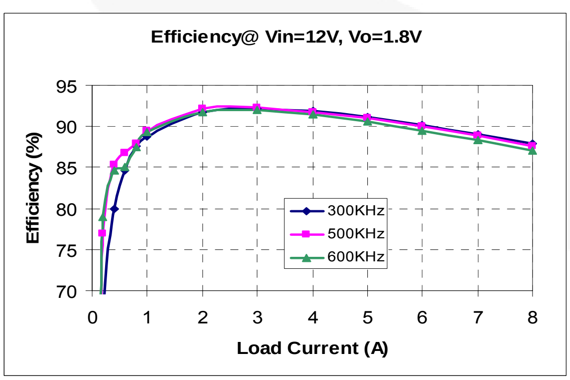

Figure 13. 1.8V_{OUT} Efficiency Over Frequency vs. Load

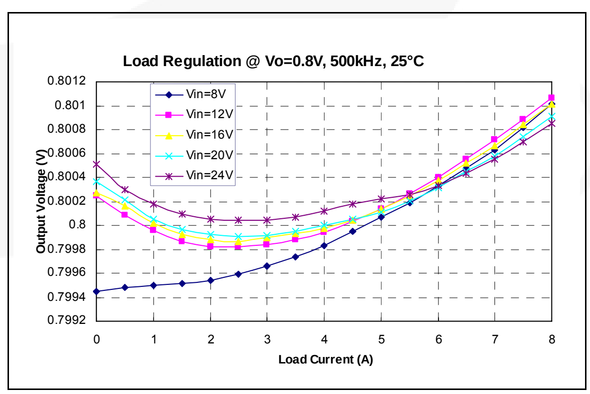

Figure 14. 0.8V_{OUT} Load Regulation Over V_{IN} vs. Load

Typical Performance Characteristics (Continued)

Typical operating characteristics using the circuit shown in Figure 10. V_{IN}=12V, V_{CC}=5V, unless otherwise specified.

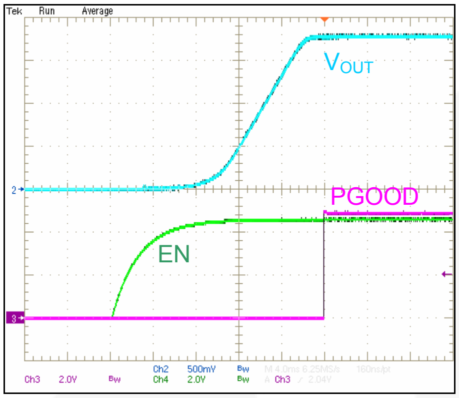

Figure 15. Startup, 3A Load

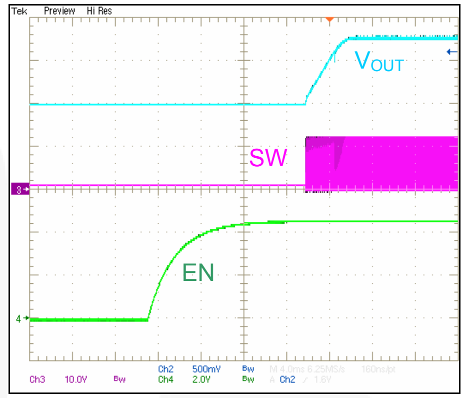

Figure 16. Startup with 1V Pre-Bias on V_{out}

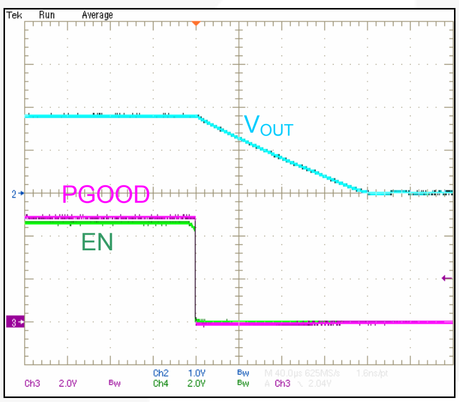

Figure 17. Shutdown, 1A Load

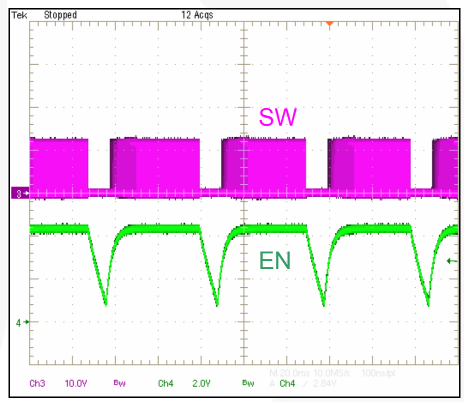

Figure 18. Restart on Fault

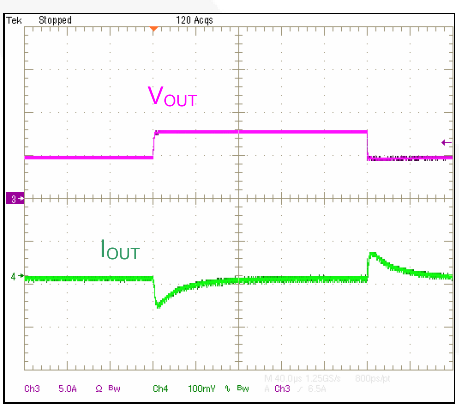

Figure 19. Transient Response, 2-8A Load

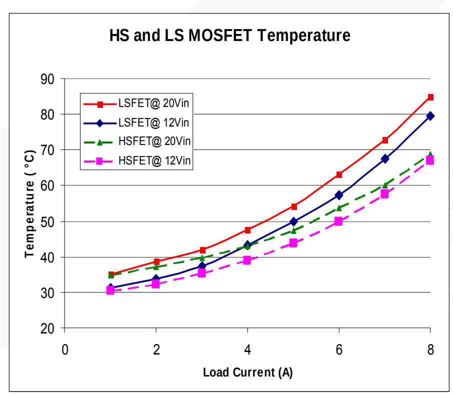

Figure 20. MOSFET Temperature – Still Air at Room Temperature

Circuit Description

Initialization

Once V_{CC} exceeds the UVLO threshold and EN is HIGH, the IC checks for an open or shorted FB pin before releasing the internal soft-start ramp (SS).

If R1 is open *(Figure 1)*, the error amplifier output (COMP) is forced LOW and no pulses are generated. After the SS ramp times out (T1.0), an under-voltage latched fault occurs.

If the parallel combination of R1 and R_{BIAS} is ≤ 1KΩ, the internal SS ramp is not released and the regulator does not start.

Bias Supply

The FAN2108 requires a 5V supply rail to bias the IC and provide gate-drive energy. Connect a ≥ 1.0µf X5R or X7R decoupling capacitor between VCC and PGND.

Since V_{CC} is used to drive the internal MOSFET gates, supply current is frequency and voltage dependent. Approximate V_{CC} current (I_{CC}) is calculated by:

$$I_{CC(mA)} = 4.58 + [(\frac{V_{CC} - 5}{227} + 0.013) \bullet (f - 128)] \qquad (1)$$

where frequency (f) is expressed in KHz.

Enable

FAN2108 has an internal pull-up to enable pin so that the IC is enabled once V_{CC} is applied. Connecting a small capacitor across EN and AGND delays the rate of voltage rise on the EN pin. EN pin also serves for the restart whenever a fault occurs *(refer to the Auto-Restart section)*. For applications where sequencing is required, FAN2108 can be enabled (after the V_{CC} comes up) with external control, as shown in Figure 20.

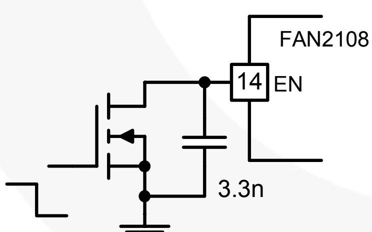

Figure 20. Enabling with External Control

Setting the Frequency

Oscillator frequency is determined by an external resistor, R_T, connected between the R(T) pin and AGND. Resistance is calculated by:

$$R_{T(K\Omega)} = \frac{(10^6 / f) - 135}{65} \qquad (2)$$

where R_T is in KΩ and frequency (f) is in KHz.

The regulator cannot start if R_T is left open.

Soft-Start

Once internal SS ramp has charged to 0.8V (T0.8), the output voltage is in regulation. Until SS ramp reaches 1.0V (T1.0), the fault latch is inhibited.

To avoid skipping the soft-start cycle, it is necessary to apply V_{IN} before V_{CC} reaches its UVLO threshold.

Soft-start time is a function of oscillator frequency.

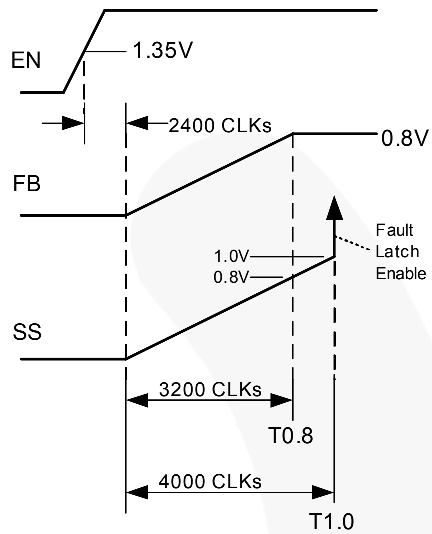

Figure 21. Soft-Start Timing Diagram

The regulator does not allow the low-side MOSFET to operate in full synchronous rectification mode until internal SS ramp reaches 95% of V_{REF} (~0.76V). This helps the regulator to start on a pre-biased output and ensures that inductor current does not "ratchet" up during the soft-start cycle.

V_{CC} UVLO or toggling the EN pin discharges the SS and resets the IC.

Setting the Output Voltage

The output voltage of the regulator can be set from 0.8V to 80% of V_{IN} by an external resistor divider (R1 and R_{BIAS} in Figure 1).

The internal reference is 0.8V with 650nA, sourced from the FB pin to ensure that, if the pin is open, the regulator does not start.

The external resistor divider is calculated using:

$$\frac{0.8V}{R_{BIAS}} = \frac{V_{OUT} - 0.8V}{R1} + 650nA \qquad (3)$$

Connect R_{BIAS} between FB and AGND.

Calculating the Inductor Value

Typically the inductor is set for a ripple current (ΔI_L) of 10% to 35% of the maximum DC load. Regulators requiring fast transient response use a value on the high side of this range; while regulators that require very low output ripple and/or use high-ESR capacitors restrict allowable ripple current.

$$L = \frac{V_{OUT} \bullet (1 - \frac{V_{OUT}}{V_{IN}})}{\Delta I_L \bullet f} \qquad (4)$$

where f is the oscillator frequency.

Setting the Ramp Resistor Value

The internal ramp voltage excursion (ΔV_{RAMP}) during t_{ON} should be set to 0.6V at nominal operating point. R_{RAMP} is approximately:

$$R_{RAMP(K\Omega)} = \frac{(V_{IN} - 1.8) \bullet V_{OUT}}{18x10^{-6} \bullet V_{IN} \bullet f} - 2 \qquad (5)$$

where frequency (f) is expressed in KHz.

Setting the Current Limit

There are two levels of current-limit thresholds in FAN2108. The first level of protection is through an internal default limit set at the factory to limit output current beyond normal usage levels. The second level of protection is externally settable at the ILIM pin. Current-limit protection is enabled whenever the lower of the two thresholds is reached. FAN2108 uses its internal low-side MOSFET for current-sensing. The current-limit threshold voltage (V_{ILIM}) is compared to a scaled version of voltage drop across the low-side MOSFET, sampled at the end of each PWM off-time/cycle. The internal default threshold (with I_{LIM} open) is temperature compensated.

The ILIM pin can source a 10µA current that can be used to establish a lower, temperature–dependent, current-limit threshold by connecting a resistor (R_{ILIM}) between ILIM and AGND. R_{ILIM} can be approximated with the equation:

$$R_{ILIM(K\Omega)} = 95 + 3 \bullet I_{out} \bullet K_T \bullet K1 + \frac{V_{out} \bullet 3.33 \bullet 10^6}{R_{ramp} \bullet f_{sw}} \qquad (6)$$

where:

I = Desired current limit setpoint in Amps;
K_T = Normalized temperature coefficient of the low-side MOSFET (Q2 from Figure 8);
K1 = Overload co-efficient (use 1.2 to 1.4);
V_{OUT} = Set output voltage;
R_{ramp} = Ramp resistor used in KΩ; and
f_{sw} = Selected switching frequency in KHz.

After 16 consecutive, pulse-by-pulse, current-limit cycles, the fault latch is set and the regulator shuts down. Cycling V_{CC} or EN restores operation after a normal soft-start cycle *(refer to Auto-Restart section)*.

The over-current protection fault latch is active during the soft-start cycle. Use a 1% resistor for R_{ILIM}.

In case R_{ILIM} is not connected, the IC uses an internal default current-limit threshold.

Loop Compensation

The loop is compensated using a feedback network around the error amplifier. Figure 22 shows a complete type-3 compensation network. For type-2 compensation, eliminate R3 and C3.

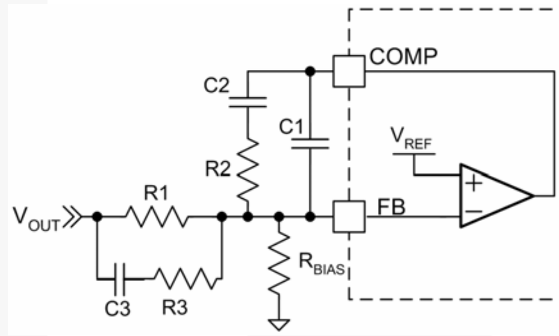

Figure 22. Compensation Network

Since the FAN2108 employs summing current-mode architecture, type-2 compensation can be used for many applications. For applications that require wide loop bandwidth and/or use very low-ESR output capacitors, type-3 compensation may be required.

Protection

The converter output is monitored and protected against extreme overload, short-circuit, over-voltage, under-voltage, and over-temperature conditions.

An internal fault latch is set for any fault intended to shut down the IC. When the fault latch is set, the IC discharges V_{OUT} by enhancing the low-side MOSFET until FB<0.25V. The MOSFET is not turned on again unless FB>0.5V. This behavior discharges the output without causing undershoot (negative output voltage).

Under-Voltage Shutdown

If voltage on the FB pin remains below the under-voltage threshold for 16 consecutive clock cycles, the fault latch is set and the converter shuts down. This protection is not active until the internal SS ramp reaches 1.0V during soft-start.

Over-Voltage Protection / Shutdown

If voltage on the FB pin exceeds the over-voltage threshold for two consecutive clock cycles, the fault latch is set and shutdown occurs.

A shorted high-side MOSFET condition is detected when SW voltage exceeds ~0.7V while the low-side MOSFET is fully enhanced. The fault latch is set immediately upon detection.

The two fault protection circuits above are active all the time, including during soft-start.

Auto-Restart

After a fault, EN pin is discharged by a 1µA current sink to a 1.1V threshold before the internal 800KΩ pull-up is restored. A new soft-start cycle begins when EN charges above 1.35V.

Depending on the external circuit, the FAN2108 can be configured to remain latched-off or to automatically restart after a fault.

Table 1. Fault / Restart Configurations

EN Pin	Controller / Restart State
Pull to GND	OFF (Disabled)
Pull-up to V_{CC} with 100K	No Restart – Latched OFF(After V_{CC} Comes Up)
Open	Immediate Restart After Fault
Cap. to GND	New Soft-Start Cycle After: t_{DELAY} (ms)=3.9 • C(nf)

With EN is left open, restart is immediate.

If auto-restart is not desired, tie the EN pin to the VCC pin or pull it HIGH after V_{CC} comes up with a logic gate to keep the 1µA current sink from discharging EN to 1.1V. Figure 23 shows one method to pull up EN to V_{CC} for a latch configuration.

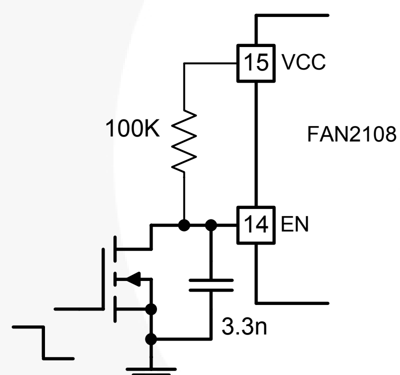

Figure 23. Enable Control with Latch Option

Over-Temperature Protection (OTP)

The chip incorporates an over-temperature protection circuit that sets the fault latch when a die temperature of about 150°C is reached. The IC restarts when the die temperature falls below 125°C.

Power-Good (PGOOD) Signal

PGOOD is an open-drain output that asserts LOW when V_{OUT} is out of regulation, as measured at the FB pin. Thresholds are specified in the Electrical Specifications section. PGOOD does not assert HIGH until the fault latch is enabled (T1.0).

PCB Layout

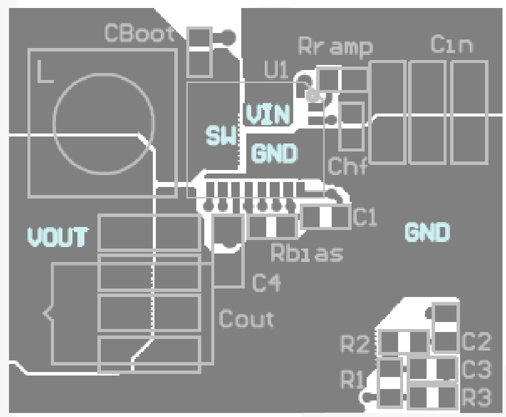

Figure 24. Recommended PCB Layout

Physical Dimensions

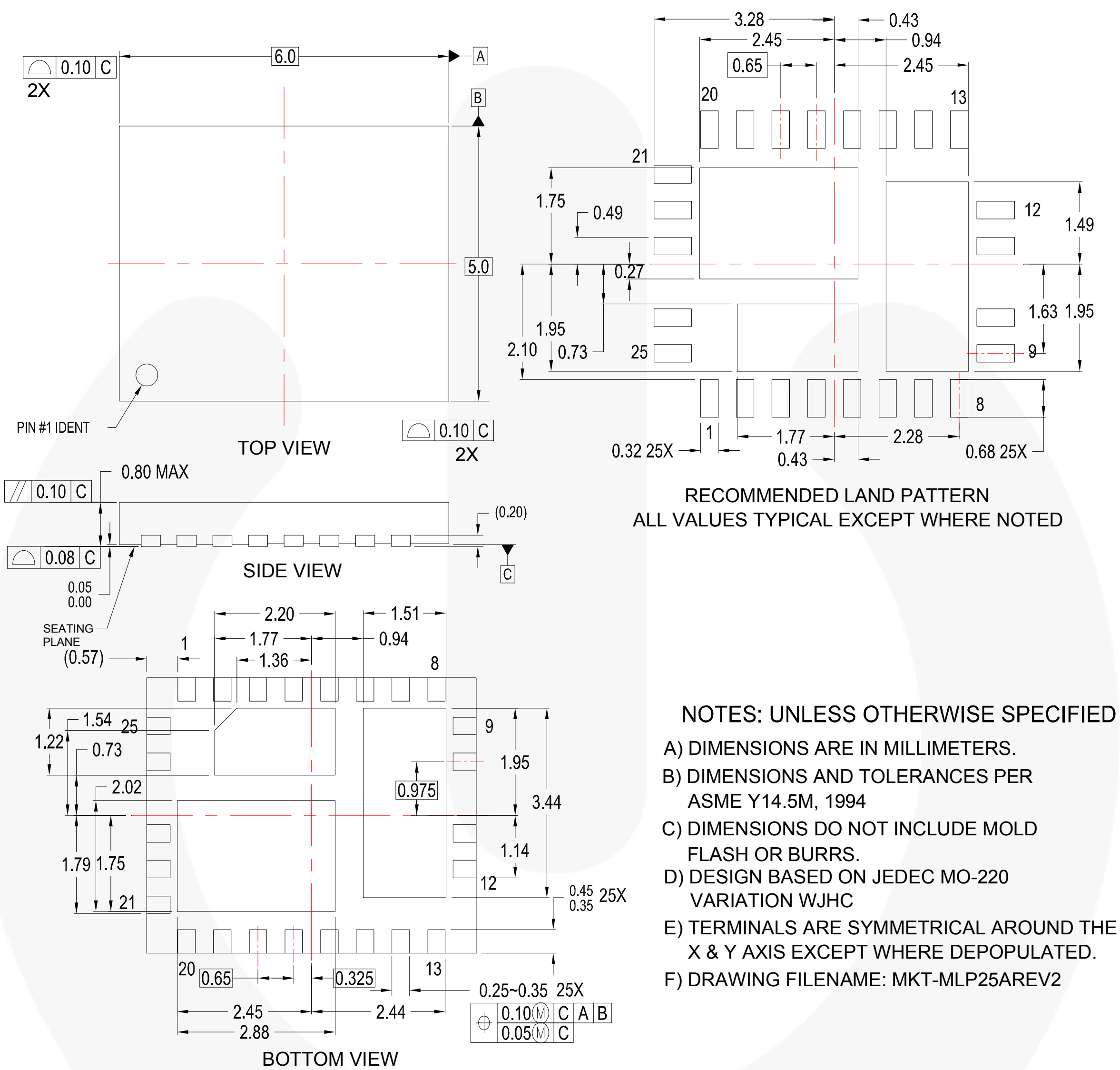

Figure 25. 5x6mm Molded Leadless Package (MLP)

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