STC3500
INTEGRATED - STRATUM 3 TIMING SOURCE

CONNOR WINFIELD

Description

The STC3500 is an integrated single chip solution for the Synchronous Timing Source in SONET/SDH network elements. The device generates four synchronous clocks, including BITS, and is fully compliant with Telcordia GR-1244-CORE, GR-253-CORE and ITU-T G.812/G.813.

The STC3500 can operate in Free Run, locked or Hold Over mode. In the Free Run mode, it locks on an OCXO or TCXO. In the locked mode, it locks on one of 8 input reference clocks. The frequency of each input reference clock can be user selected or automatically detected by the device. The active reference can be automatically selected by the device based on a priority table or manually controlled by the user. All reference switches are hit-less. In Hold Over mode, the device generates outputs based on the frequency history of the last locked reference.

The STC3500 supports the Master or Slave mode of operation for redundant designs. In master mode, the device operates in Free Run, locked or Hold Over. In slave mode, the output clocks are locked to the master's primary Sync_Clk or 8 kHz synchronous clock output and are phase offset adjustable.

Parallel or serial bus interfaces are provided to access STC3500 internal control and status registers.

Major operations can be performed from either the bus interface or external hardwire pins.

Features

- Complies with Telcordia GR-1244-CORE, GR-253-CORE, and ITU-T G.812/G.813
- Supports Master/Slave operation
- Supports Free Run, Locked, and Hold Over modes
- Accepts 8 reference inputs from 8 kHz to 77.76 MHz and one 8 kHz cross reference
- Continuous input reference quality monitoring
- Input reference frequencies are automatically detected
- Automatic or manual selection for active reference
- Supports hardwire pins to select active reference
- Four output signals: one selectable up to 155.52 MHz, one fixed at 8 kHz, one multi-frame sync fixed at 2 kHz, and 1.544 MHz or 2.048 MHz BITS output
- Output phase is adjustable in slave mode
- Frequency ramp control during reference switching
- Hit-less reference switching
- Configurable bandwidth filter
- Supports SPI and 8-bit parallel bus interface
- IEEE 1149.1 JTAG boundary scan
- Available in FBGA144 package

Functional Block Diagram

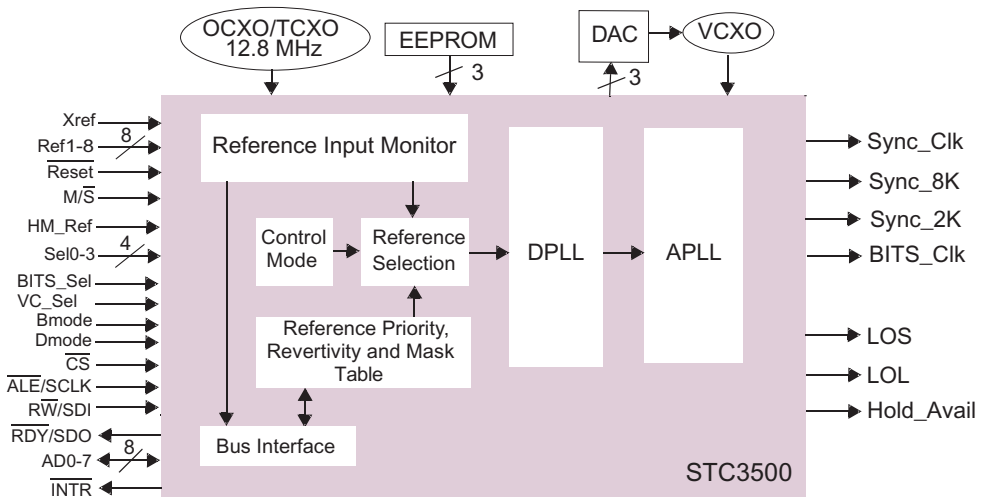

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Table of Contents

How to read this document

In the following sections, the intent is as follows:

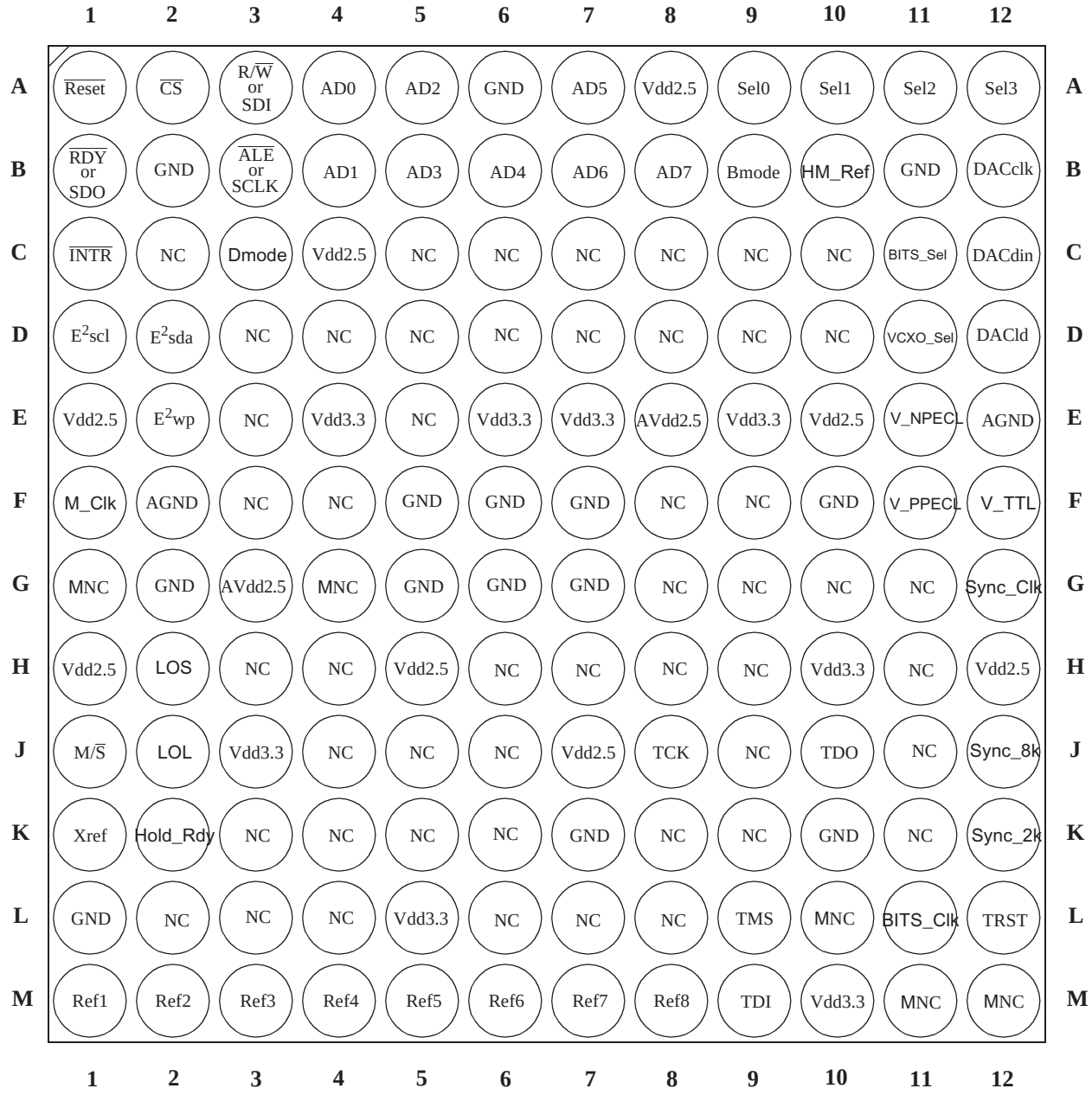
Detailed Description and Register Descriptions – "How the device works"

Performance – This section provides terminology definitions and detailed data on how the chip performs

Application Notes – "How to use the device" from an application perspective

STC3500 Ball Grid Diagram (Top View)

Figure 1



Note: Pins indicated as “MNC” are mandatory no-connects. Pins indicated as “NC” may be left unconnected or may be grounded.

Pin Description

Table 1

Pin Name	Pin #	I/O	Description
Vdd2.5	A8, C4, E1, E10, H1, H5, H12 J7		2.5V Digital Power Supply
Vdd3.3	E4, E6, E7, E9, H10, J3, L5, M10		3.3V Digital Power Supply
GND	A6, B2, B11, F5, F6, F7, F10, G2, G5, G6, G7, K7, K10, L1		Digital Ground
AVdd2.5	E8, G3		2.5V Analog Power Supply
AGND	E12, F2		Analog Ground
TMS	L9	I	Controls the use of Boundary Scan
TCK	J8	I	Clock input for Boundary Scan
TDI	M9	I	Serial input for Boundary Scan
TDO	J10	O	Serial output for Boundary Scan
TRST	L12	I	Active low input pin for resetting boundary-scan circuitry
HM_Ref	B10	I	Hardware Mode for reference selection: 1: Enable, 0: Disable
Bmode	B9	I	Bus interface selection, 1: Parallel, 0: SPI
Dmode	C3	I	Selects the configuration data source, 0: Bus interface, 1: EEPROM
$\overline{\text{Reset}}$	A1	I	Active low to reset the logic, minimum low time: 100 nS
$\overline{\text{CS}}$	A2	I	Chip Select: Asserted low to enable bus interface
$\overline{\text{ALE}}$ or SCLK	B3	I	Address Latch Enable in parallel bus interface mode, SCLK in SPI mode
R/$\overline{\text{W}}$ or SDI	A3	I	Read/$\overline{\text{Write}}$ in Parallel Bus Interface Mode, SDI in SPI Mode
$\overline{\text{RDY}}$ or SDO	B1	O	$\overline{\text{Ready}}$ in Parallel Bus Mode, SDO in SPI Mode
$\overline{\text{INTR}}$	C1	O	Active low to notify Micro-controller of events, cleared by reading register Int_Event
AD0	A4	I/O	AD0: Address/Data bit 0 (multiplexed) in Parallel Bus Mode
AD1	B4	I/O	AD1: Address/Data bit 1 (multiplexed) in Parallel Bus Mode
AD2	A5	I/O	AD2: Address/Data bit 2 (multiplexed) in Parallel Bus Mode
AD3	B5	I/O	AD3: Address/Data bit 3 (multiplexed) in Parallel Bus Mode
AD4	B6	I/O	AD4: Address/Data bit 4 (multiplexed) in Parallel Bus Mode
AD5	A7	I/O	AD5: Address/Data bit 5 (multiplexed) in Parallel Bus Mode
AD6	B7	I/O	AD6: Address/Data bit 6 (multiplexed) in Parallel Bus Mode
AD7	B8	I/O	AD7: Address/Data bit 7 (multiplexed) in Parallel Bus Mode
M/$\overline{\text{S}}$	J1	I	Master or $\overline{\text{Slave}}$ Selection, 1: Master, 0: Slave

Pin Description

Table 1 continued

Pin Name	Pin #	I/O	Description
Sel0	A9	I	In Hardware Mode (HM_Ref = 1), Sel0 ~ Sel3 will determine the Free Run, Locked, Hold Over, and the Active Reference in Locked Mode. See Table 5 in Hardware Control Modes section
Sel1	A10	I	See Table 5 in Hardware Control Modes section
Sel2	A11	I	See Table 5 in Hardware Control Modes section
Sel3	A12	I	See Table 5 in Hardware Control Modes section
BITS_Sel	C11	I	1.544 MHz or 2.048 MHz BITS clock selection, 1 = 1.544 MHz, 0 = 2.048 MHz
LOS	H2	O	Loss of signal indicator for the selected reference, 1 = Loss of Signal
LOL	J2	O	Loss of phase lock, 1 = Loss of Lock
Hold_Rdy	K2	O	Hold Over history built and usable = 1
Xref	K1	I	Cross Reference Input
Ref1	M1	I	Reference Input 1
Ref2	M2	I	Reference Input 2
Ref3	M3	I	Reference Input 3
Ref4	M4	I	Reference Input 4
Ref5	M5	I	Reference Input 5
Ref6	M6	I	Reference Input 6
Ref7	M7	I	Reference Input 7
Ref8	M8	I	Reference Input 8
Sync_Clk	G12	O	Synchronous Clock: Output frequency is dependent on VCXO frequency
Sync_8K	J12	O	Synchronous Clock: 8 kHz
BITS_Clk	L11	O	BITS clock output
Sync_2K	K12	O	Multi-frame sync: 2 kHz
M_Clk	F1	I	OCXO or TCXO local crystal oscillator input
VC_TTL	F12	I	VCXO TTL input
VC_PPECL	F11	I	VCXO PPECL input
VC_NPECL	E11	I	VCXO NPECL input
VC_Sel	D11	I	Selects the VCXO output signal electrical format, 0: PECL, 1: TTL
DACclk	B12	O	DAC Serial Bus Interface: CLK
DACdin	C12	O	DAC Serial Bus Interface: Din
DACld	D12	O	DAC Serial Bus Interface: $\overline{CS}$/LD
E^2scl	D1	O	EEPROM interface: SCL
E^2sda	D2	I/O	EEPROM interface: SDA
E^2wp	E2	O	EEPROM interface: WP
MNC	G1, G4, L10, M11, M12		Mandatory no-connect - must be left floating

Absolute Maximum Ratings

Table 2

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
Vdd2.5	Logic power supply voltage, 2.5V	-0.3	-	3.0	Volts	1
Vdd3.3	Logic power supply voltage 3.3V	-0.3	-	4.0	Volts	1
AVdd2.5	Analog power supply voltage, 2.5V	-0.3	-	4.0	Volts	1
V_{IN}	Logic input voltage, rel. to GND	-0.3	-	Vdd3.3 + 0.5	Volts	1
T_{STG}	Storage Temperature	-55	-	110	°C	1

Note 1: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the Recommended Operating Conditions.

Recommended Operating Conditions & Electrical Characteristics

Table 3

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
Vdd2.5	2.5V digital power supply voltage	2.3	2.5	2.7	Volts	
Vdd3.3	3.3V digital power supply voltage	3.0	3.3	3.6	Volts	
AVdd2.5	2.5V analog power supply voltage	2.3	2.5	2.7	Volts	
V_{IH} (3.3V)	High level input voltage	2.0	-	Vdd3.3 + 0.3	Volts	2
V_{IL} (3.3V)	Low level input voltage	0.3	-	0.8	Volts	2
V_{OH} (3.3V)	High level output voltage (I_{OH} = -7mA)	0.9*Vdd3.3	-	-	Volts	2
V_{OL} (3.3V)	Low level output voltage (I_{OL} =10mA)	-	-	0.4	Volts	2
V_{IL} (PECL)	Low level input voltage (PECL inputs)	0.86	-	2.125	Volts	
V_{OH} (PECL)	High level input voltage (PECL inputs)	1.49	-	2.72	Volts	
V_{ID} (PECL)	PECL differential input voltage	0.3	-	Vdd3.3	Volts	
C_{IN}	Input capacitance	-	-	10	pF	
T_{HL}	Clock fall time (TCXO, OCXO, VCXO)	-	-	5	nS	
T_{LH}	Clock rise time (TCXO, OCXO, VCXO)	-	-	5	nS	
T_{RIP}	Input reference signal positive pulse width	10	-	-	nS	
T_{RIN}	Input reference signal negative pulse width	10	-		nS	
T_A	Operating Ambient Temperature Range	0	-	70	°C	
Icc (Vdd2.5)	2.5V digital supply current	-	-	500	mA	
Icc (Vdd3.3)	3.3V digital supply current	-	-	200	mA	
Icc (Avdd2.5)	2.5V analog supply current	-	-	50	mA	
Pd	Device power dissipation	-	-	2.0	W	

Note 2: LVTTL compatible

Register Map

Table 4

Address	Reg Name	Description	Type
0x00	Chip_ID_Low	Low byte of chip ID	R
0x01	Chip_ID_High	High byte of chip ID	R
0x02	Chip_Revision	Chip revision number	R
0x03	Bandwidth_PBO	Bandwidth & Phase Build-Out option	R/W
0x04	Ctl_Mode	Manual or automatic selection of Op_Mode, BITS clock output frequency indication, and frame/multi-frame sync pulse width mode control	R/W
0x05	Op_Mode	Master Free Run, Locked, or Hold Over mode, or Slave mode	R/W

Register Map continued

Table 4

Address	Reg Name	Description	Type
0x06	Max_Pullin_Range	Maximum pull-in range in 0.1 ppm units	R/W
0x07	Xref_Activity	Cross Reference activity and frequency	R
0x08	Ref_Activity	Activities of 8 reference inputs	R
0x09	Ref_Pullin_Sts	In or out of pull-in range of 8 reference inputs	R
0x0a	Ref_Qualified	Qualification of 8 reference inputs	R
0x0b	Ref_Mask	Availability mask for 8 reference inputs	R/W
0x0c	Ref_Available	Availability of 8 reference inputs	R
0x0d	Ref_Rev_Delay	Reference reversion delay time, 0 - 255 minutes	R/W
0x0e	MS_Phase_Offset	Phase offset between Xref & Sync_8K (for the slave in M/S operation), in 250 pS resolution	R/W
0x0f	Calibration	Local oscillator digital calibration in 0.05 ppm resolution	R/W
0x10	Fr_Pulse_Width	Frame and multi-frame sync pulse width	R/W
0x11	DPLL_Status	Digital Phase Locked Loop status	R
0x12	Intr_Event	Interrupt events	R
0x13	Intr_Enable	Enable individual interrupt events	R/W
0x14	Ref1_Frq_Offset1	Ref1 frequency offset in 0.2 ppm resolution	R
0x15	Ref2_Frq_Offset2	Ref2 frequency offset in 0.2 ppm resolution	R
0x16	Ref3_Frq_Offset3	Ref3 frequency offset in 0.2 ppm resolution	R
0x17	Ref4_Frq_Offset4	Ref4 frequency offset in 0.2 ppm resolution	R
0x18	Ref5_Frq_Offset5	Ref5 frequency offset in 0.2 ppm resolution	R
0x19	Ref6_Frq_Offset6	Ref6 frequency offset in 0.2 ppm resolution	R
0x1a	Ref7_Frq_Offset7	Ref7 frequency offset in 0.2 ppm resolution	R
0x1b	Ref8_Frq_Offset8	Ref8 frequency offset in 0.2 ppm resolution	R
0x1c	Ref1_Frq_Priority1	Ref1 frequency and priority	R/W
0x1d	Ref2_Frq_Priority2	Ref2 frequency and priority	R/W
0x1e	Ref3_Frq_Priority3	Ref3 frequency and priority	R/W
0x1f	Ref4_Frq_Priority4	Ref4 frequency and priority	R/W
0x20	Ref5_Frq_Priority5	Ref5 frequency and priority	R/W
0x21	Ref6_Frq_Priority6	Ref6 frequency and priority	R/W
0x22	Ref7_Frq_Priority7	Ref7 frequency and priority	R/W
0x23	Ref8_Frq_Priority8	Ref8 frequency and priority	R/W
0x24	Free Run_Priority	Control and priority for designation of Free Run as a reference	R/W
0x25	History_Policy	Sets policy for Hold Over history accumulation	R/W
0x26	History_Cmd	Save, restore, and flush commands for Hold Over History	R/W
0x27	Hold Over_Time	Indicates the time since entering the Hold Over state	R
0x30	Cfgdata	Configuration data write register	R/W
0x31	Cfgctr_Lo	Configuration data write counter, low byte	R
0x32	Cfgctr_Hi	Configuration data write counter, high byte	R
0x33	Chksum	Configuration data checksum pass/fail indicator	R
0x36	EE_Wrt_Mode	Disables/Enables writing to the external EEPROM	R/W
0x37	EE_Cmd	Read/Write command and ready indication register for external EEPROM Access	R/W
0x38	EE_Page_Num	Page number for external EEPROM access	R/W
0x39	EE_FIFO_Port	Read/Write data for external EEPROM access	R/W

Detailed Description

The STC3500 is a single chip synchronization and timing solution for the Stratum 3 in network elements. Its highly integrated design includes hardware and software to implement all of the necessary reference selection, monitoring, digital filtering, synthesis, and control functions. An external OCXO/TCXO, DAC, and VCXO (and optional EEPROM) complete a system level solution (see Functional Block Diagram).

Up to 8 external references, each from 8 kHz to 77.76 MHz, may be equipped and monitored for signal presence and frequency offset. Additionally, a cross-couple reference input, accepting from 8 kHz to 77.76 MHz, is provided for master/slave operation. Reference selection may be manual or automatic, according to pre-programmed priorities. All reference switches are performed in a hitless manner, and frequency ramp controls ensure smooth output signal transitions. When references are switched, the device provides a controllable phase build-out to minimize phase transitions in the output clocks.

Three phase aligned output signals are provided, the first up to 155.52 MHz (determined by VCXO selection), the second fixed at 8 kHz for use as a frame signal. Both of these may also be used as a cross-couple reference for master/slave operation. In slave mode, the output phase may be adjusted from -32 to +31.75nS relative to the master, to accommodate downstream system needs, such as different clock distribution path lengths. The third phase aligned output is a 2 kHz multi-frame sync output. The fourth output is a BITS clock, selectable as either 1.544 MHz or 2.048 MHz

Device operation may be in Free Run, synchronized, or Hold Over modes. In Free Run, the clock outputs are simply determined by the accuracy of the digitally calibrated OCXO/TCXO. In synchronized mode, the chip phase locks to the selected input reference. While synchronized, a frequency history is accumulated. In Hold Over mode, the chip outputs are generated according to this history.

The Digital Phase Locked Loop which provides the critical filtering and frequency/phase control functions is implemented with a set of well-proven algorithms and control that meet or exceed all requirements and lead the industry in critical jitter and accuracy performance parameters. Filter bandwidth may be configured.

Control functions are provided either via direct hardware signals or standard SPI or 8-bit parallel bus register interfaces. Direct hardware control provides a very simple system interface, while bus/register access provides greater visibility into a variety of registered information as well as providing more extensive programmable control capability.

Operating Modes: The STC3500 operates in either Free Run, locked, or Hold Over mode:

Free Run – In Free Run mode, **Sync_Clk, Sync_8K, BITS_Clk**, and **Sync_2K**, the output clocks, are determined directly from and have the accuracy of the calibrated free running OCXO/TCXO. Reference inputs continue to be monitored for signal presence and frequency offset, but are not used to synchronize the outputs.

Locked – The **Sync_Clk, Sync_8K, BITS_Clk**, and **Sync_2K** outputs are phase locked to and track the selected input reference. Upon entering the Locked mode, the device begins an acquisition process that includes reference qualification and frequency slew rate limiting, if needed. Once satisfactory lock is achieved, the “Locked” bit is set in the **DPLL_Status** register, and a frequency history for the selected reference will begin to be compiled. When a usable Hold Over history has been established, the **Hold_Avail** pin is set, and the “Hold Over Available” bit is set in the **DPLL_Status** register.

Phase comparison and phase lock loop filtering operations in the STC3500 are completely digital. As a result, device and loop behavior are entirely predictable, repeatable, and extremely accurate. Carefully designed and proven algorithms and techniques ensure completely hit-less reference switches, operational mode changes, and master/slave switches.

Basic loop bandwidth is programmable from .66 milliHertz to 1.4 Hertz, giving the user a wide range of control over the system response.

When a new reference is acquired, maximum frequency slew limits ensure smooth frequency changes. Once lock is achieved, (<100 seconds for stratum) the “Locked” bit is set. If the STC3500 is unable to maintain lock, Loss of Lock (**LOL**) is asserted. All transitions between locked, Hold Over and Free Run modes are performed with no phase hit and smooth frequency and phase transitions.

Reference phase hits or phase differences encountered when switching references (or when entering locked mode) are nulled out with an automatic phase build-out function, with a residual phase error of less than 1 nS. The optional Phase build-out feature can be disabled for phase hits on the selected reference, as required for Stratum 3.

Hold Over – Upon entering Hold Over mode, the **Sync_Clk, Sync_8K, BITS_Clk**, and **Sync_2K** outputs are determined from the Hold Over history established for the last selected reference. Output frequency is determined by a weighted average of the Hold Over history, and accuracy is determined by the OCXO/TCXO. Hold Over mode may be entered manually or automatically. Automatic entry into Hold Over mode occurs when operating in the automatic mode, the reference is lost, and no other valid reference exists. The transfer into and out of Hold Over mode is designed to be smooth and free of hits. The frequency slew is also limited to a maximum of ±2 ppm/sec.

The history accumulation algorithm uses a first order frequency difference filtering algorithm. Typical Hold Over accumulation takes about 15 minutes. When a usable Hold Over history has been established, the **Hold_Avail** pin is set, and the “Hold Over Available” bit is set in the **DPLL_Status** register. The Hold Over history continues to be updated after “Hold Over Available” is declared.

The Hold Over history accumulates only when it has locked on either an external reference in Master operation or the **Xref** clock in Slave operation, starting 15 minutes after power up. Tracking will be suspended automatically when switching to a new reference, while in the Hold Over mode, and in the Free Run mode. A set of registers allows the application to control a Hold Over history maintenance policy, enabling either a rebuild or continuance of the history when a reference switch occurs.

Furthermore, under register access control, a backup Hold Over history register is provided. It may be loaded from the active Hold Over history or restored to the active Hold Over history. The active Hold Over history may also be flushed. See **Hold Over History Accumulation and Maintenance** section.

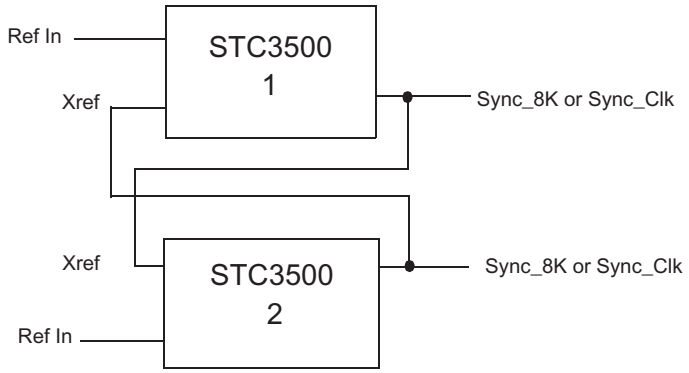
Hold Over mode may be entered at any time. If there is no Hold Over history available, the prior output frequency will be maintained. When in Hold Over, the application may read (via register access) the time since Hold Over was entered.

Master/Slave Operation

Pairs of STC3500 devices may be operated in a master/slave configuration for added reliability. A typical configuration is shown below:

Master / Slave Configuration

Figure 2



The **Sync_8K** or **Sync_Clk** output of each device is cross-connected to the other device's **Xref** input. The device auto-detects the frequency on the **Xref** input. Master or slave state of a device is determined by the **M/S** pin. Thus, master/slave state is always manually controlled by the application. The master synchronizes to the selected input reference, while the slave synchronizes to the **Xref** input. (Note that 8 kHz frame phase alignment is maintained across a master/slave pair of devices only if **Sync_8K** is used as the cross couple signal.)

The unit operating in slave mode locks on and phase-aligns to the cross-reference clock (**Sync_8K** or **Sync_Clk**) from the unit in master mode. The phase skew between the input cross-reference and the output clock for the slave unit is typically less than ±1ns (under ±3ns in dynamic situations, including reference jitter and wander).

Perfect phase alignment of the two **Sync_Clk** output clocks would require no delay on the cross-reference clock connection. To accommodate path length delays, the STC3500 provides a programmable phase skew feature. The slave's **Sync_Clk/8k** output may be phase shifted -32nS to +31.75nS relative to **Xref** according to the contents of the **Phase_Offset** register to compensate for the path length of the **Sync_8K** or **Sync_Clk** to **Xref** connection. This offset may therefore be programmed to exactly compensate for the actual path length delay associated with the particular application's cross-reference traces. The offset may further be adjusted to accommodate any output clock distribution path delay differences. Thus, master/slave switches with the STC3500 devices may be accomplished with near-zero phase hits.

The first time a unit becomes a slave, such as immediately after power-up, its output clock phase starts out arbitrary, and will quickly phase-align to the cross-reference from the master unit. The phase skew will be eliminated (or converged to the programmed phase offset) step by step. The whole pull-in-and-lock process will complete in about 60 seconds. There is no frequency slew protection in slave mode. In slave mode, the unit's mission is to lock to and follow the master.

Once a pair of units has been operating in aligned master/slave mode, and a master/slave switch occurs, the unit that becomes master will maintain its output clock phase and frequency while a phase build-out (to the current output clock phase) is performed on its selected reference input. Therefore, as master mode operation commences, there will be no phase or frequency hits on the clock output.

Likewise, the unit that becomes the slave will maintain its output clock frequency and phase for 1 msec before starting to follow the cross-reference, protecting the downstream clock users during the switch. Assuming the phase offset is programmed for the actual propagation delay of this cross-reference path, there will again be no phase hits on the output clock of the unit that has transitioned from master to slave.

Control Modes

Parallel or serial bus interfaces are provided to access STC3500 internal control and status registers. The selected reference, operational modes, master/slave mode, enabling of phase build-out and loop bandwidth controls can be accessed from either the bus interface or external device pins.

Hardware Control – The device may be configured for direct pin control over key functions for simple hardwired configurations.

The **HM_Ref** pin enables hardware control of reference selection and operational mode. When it is a "1", mode control and reference input selection may be provided by direct hardware pin inputs **Sel0-3** (see Table 5) and the corresponding register access becomes read-only. When **HM_Ref** is disabled (=0), reference selection and operational mode control is via register access.

The **M/S** pin determines master or slave mode. 1=Master, 0=Slave. In master mode and with **HM_Ref** = 1, the hardware control of operational mode and reference selection are as shown in the table below:

Hardware Reference Selection and Mode Control

Table 5

Pin				Function	
Sel3	Sel2	Sel1	Sel0	Mode	Reference
0	0	0	0	Free Run	N/A
0	0	0	1	Locked	1
0	0	1	0	Locked	2
0	0	1	1	Locked	3
0	1	0	0	Locked	4
0	1	0	1	Locked	5
0	1	1	0	Locked	6
0	1	1	1	Locked	7
1	0	0	0	Locked	8
1	0	0	1	Hold Over	N/A
1	0	1	0	Hold Over	N/A
1	0	1	1	Hold Over	N/A
1	1	0	0	Hold Over	N/A
1	1	0	1	Hold Over	N/A
1	1	1	0	Hold Over	N/A
1	1	1	1	Hold Over	N/A

In slave mode, the operational mode is "locked" and the reference is the **Xref** input.

See **Register Descriptions and Operation** and **Application** section: **Control Modes** for more details.

The **VC_Sel** pin determines if the VCXO input to the chip is TTL or PECL, 1 = TTL, 0 = PECL. See **Application Notes, Peripherals** section.

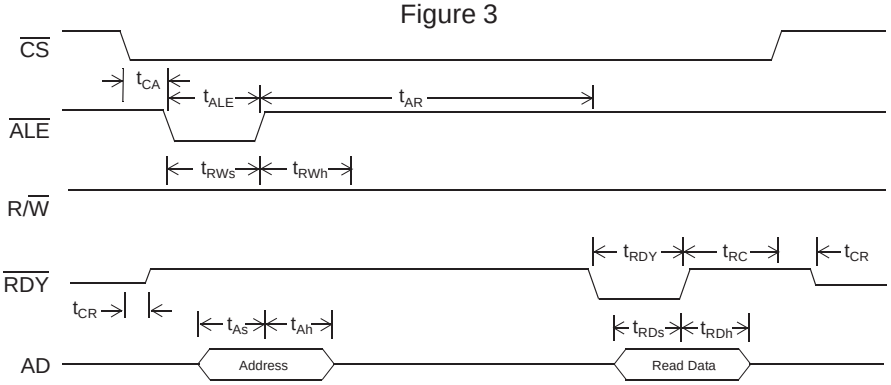
Following any device reset, either via power-up or operation of the **$\overline{\text{Reset}}$** pin, the device needs to be loaded with its DPLL configuration data. This data may come from either an external EEPROM, or the bus interface. The **Dmode** pin selects the source for configuration data, 0 = from the bus interface, 1 = from the EEPROM. If the source is an EEPROM, devices pre-loaded with the configuration data are available from Connor-Winfield (See **Application Notes, External Component Selection** section). Data may also be loaded into or read from the EEPROM via the bus interface (See **Application Notes, Reading and Writing EEPROM Data** section).

If the data is to be application provided on reset through the bus interface (i.e. the optional EEPROM is not equipped), the data is available from Connor-Winfield as a file and is loaded per the procedure described in the **Application Note, Configuration Data** section.

Register Control – Bus/Register access is available in 8-bit parallel or SPI form, as selected by the **Bmode** pin. **Bmode**=1 selects parallel bus access, and **Bmode**=0 selects SPI. Parallel bus and SPI data I/O operations are shown as follows.

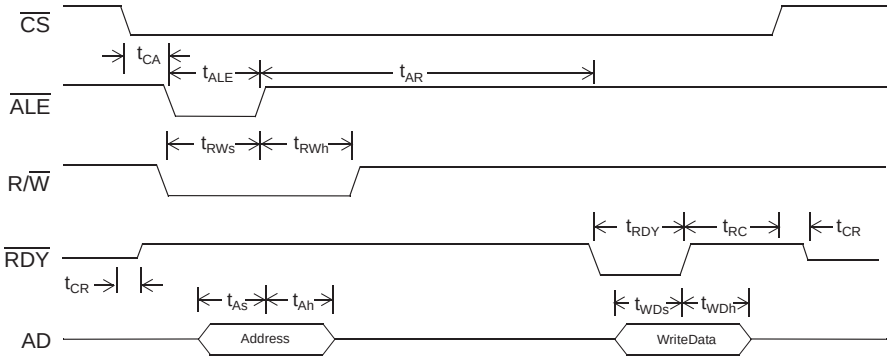
Parallel Bus Timing, Read Access

Figure 3



Parallel Bus Timing, Write Access

Figure 4



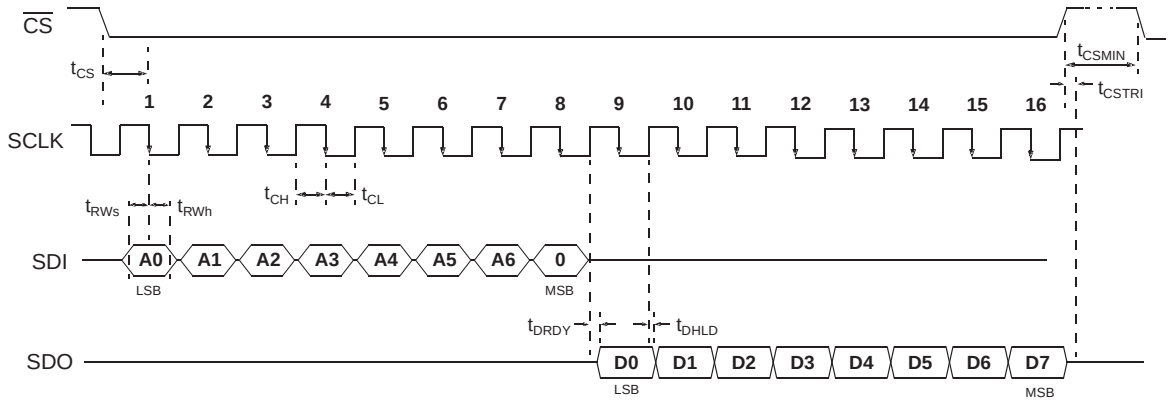
Parallel Bus Timing

Table 6

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
tCA	$\overline{CS}$ low to $\overline{ALE}$ low	0	-	-	ns	
tALE	$\overline{ALE}$ low time	70	-	-	ns	
tAR	$\overline{ALE}$ high to $\overline{RDY}$ low	-	-	250	ns	
tRWs	R/$\overline{W}$ setup time	50	-	-	ns	
tRWh	R/$\overline{W}$ hold time	50	-	-	ns	
tRDY	$\overline{RDY}$ low time	100	-	-	ns	
tRC	$\overline{RDY}$ high to $\overline{CS}$ high	-	-	0	ns	
tCR	$\overline{CS}$ to $\overline{RDY}$ active/tristate time	-	-	10	ns	
tAs	Address setup time	50	-	-	ns	
tAh	Address hold time	50	-	-	ns	
tRDs	Read data setup time	50	-	-	ns	
tRDh	Read data hold time	50	-	-	ns	
tWDs	Write data setup time	50	-	-	ns	
tWDh	Write data hold time	50	-	-	ns	

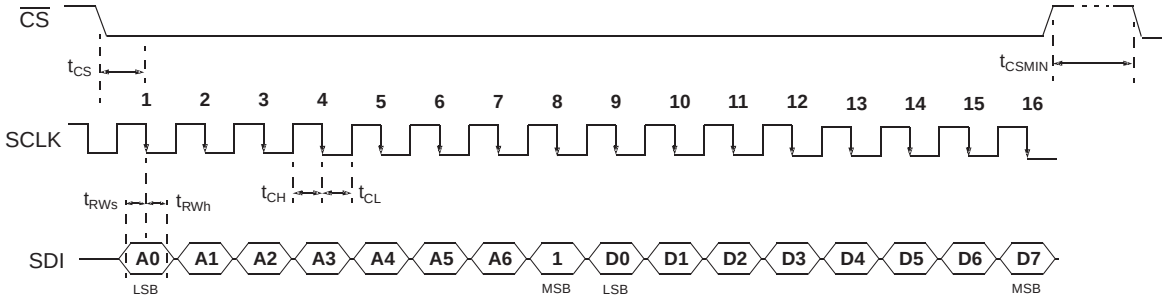
Serial Bus Timing, Read Access

Figure 5



Serial Bus Timing, Write Access

Figure 6



Serial Bus Timing

Table 7

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
tCS	$\overline{CS}$ low to SCLK low	10	-	-	ns	
tCH	SCLK high time	25	-	-	ns	
tCL	SCLK low time	25	-	-	ns	
tRWs	Read/Write setup time	15	-	-	ns	
tRWh	Read/Write hold time	15	-	-	ns	
tDRDY	Data ready	-	-	25	ns	
tDHLD	Data hold	15	-	-	nS	
tCSTRI	Chip select to data tri-state	5	-	-	nS	
tCSMIN	Minimum delay between successive accesses	300	-	-	nS	

Reference Input Quality Monitoring

Each reference input is monitored for signal presence and frequency offset. Signal presence for the **Ref1-8** inputs is indicated in the **Ref_Activity** register and signal presence and frequency for the **Xref** input is indicated in bits 0-3 of the **Xref_Activity** register. The frequency offset between the **Ref1-8** inputs and the calibrated local oscillator is available in the **Ref_Frq_Offset** registers (8). Register **Ref_Pullin_Sts** indicates, for each of the **Ref1-8** inputs, if the reference is within the maximum pull-in range. The maximum pull-in range is indicated in register **Max_Pullin_Range**, and may be set in .1ppm increments. Typically, it would be set according to the values specified by the standards (GR-1244) appropriate for the particular stratum of operation.

The **Ref_Qualified** register contains the “anded” condition of the **Ref_Activity** and **Ref_Pullin_Sts** registers for each of the **Ref1-8** inputs, qualified for 10 seconds. When a reference signal has been present for > 10 seconds and is within the pull-in range, it’s bit is set.

The **Ref_Available** register contains the “anded” condition of the **Ref_Qualified** register and the **Ref_Mask** register, and therefore represents the availability of a reference for selection when automatic reference and operational mode selection is enabled.

When active reference selection is manual (see **Reference Input Selection** below), if the selected reference signal is lost, Loss of Signal (**LOS**) is asserted, active “high” (pin output and bit 0 of the **DPLL_Status** register).

Reference Input Selection, Frequencies, and Mode Selection

One of eight reference input signals (**Ref1-8**) may be selected for synchronization in Master mode (as described below and in the **Op_Mode** register description). **Ref1-8** may each be 8 kHz, 1.544 MHz, 2.048 MHz, 12.96 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, or 77.76 MHz

Reference frequencies are auto-detected (frequency determined by the chip) and the detected frequency may be read from the **Ref_Frq_Priority** registers (See **Register Descriptions and Operation** section).

The **Xref** input for slave operation is frequency auto-detected and may be 8 kHz, 1.544 MHz, 2.048 MHz, 12.96 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, or 77.76 MHz. Signal presence and frequency for the **Xref** input is indicated in bits 0-3 of the **Xref_Activity** register.

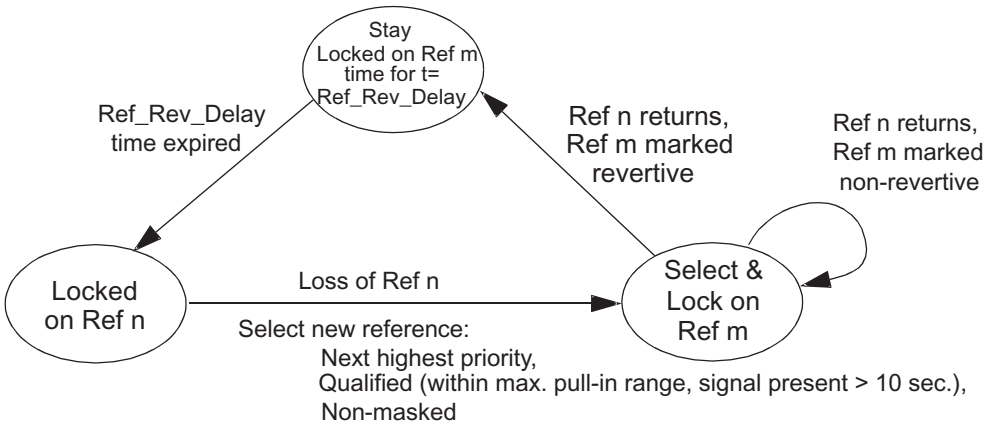
In Register Mode for reference and operational mode selection (**HM_Ref** = 0), active reference and operational mode selection may be manual or automatic, as determined by bit 1 in the **Ctl_Mode** register. In manual mode, register writes to **Op_Mode** select the reference and mode. The reset default is manual mode.

In automatic mode, the reference is selected according to the priorities written to the eight **Ref_Frq_Priority** registers. Individual references may be masked for use/non-use according to the **Ref_Mask** register. A reference may only be selected if it is “available” - that is, it is qualified, as indicated in the **Ref_Qualified** register, and is not masked (See **Reference Input Quality Monitoring** and **Register Descriptions and Operation** sections).

Furthermore, bit 3 of each **Ref_Frq_Priority** register will determine if that reference is revertive or non-revertive. When a reference fails, the next highest priority “available” (signal present, non-masked, and acceptable frequency offset) reference will be selected. When a reference returns, it will be switched to only if it is of higher priority and the current active reference is marked “Revertive”. Additionally, the reversion is delayed according to the value written to the **Ref_Rev_Delay** register (From 0 to 255 minutes).

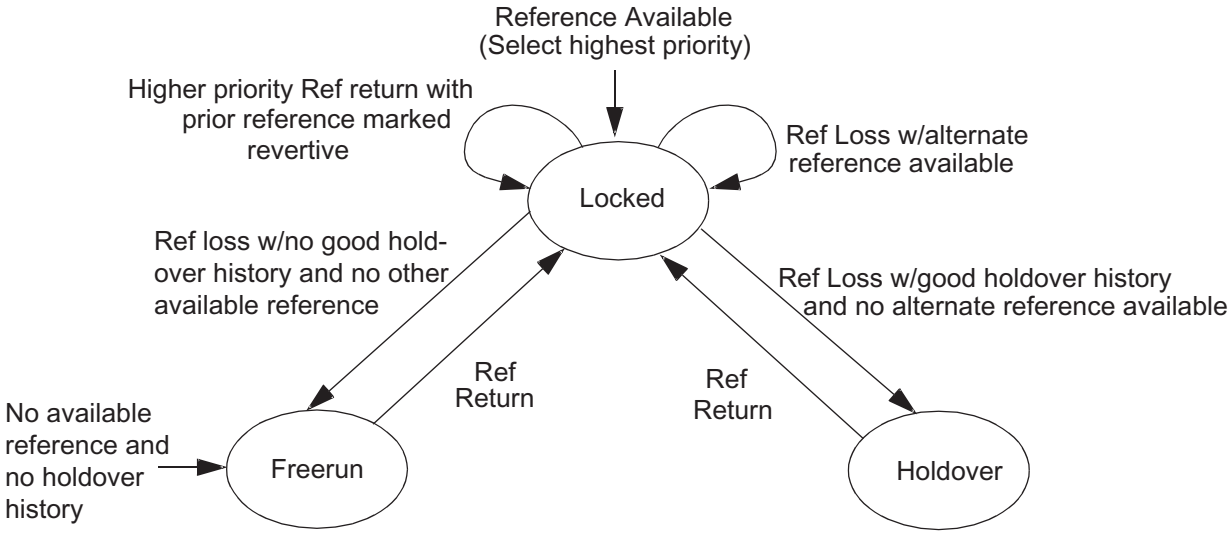
The automatic reference selection is shown in the following state diagram:

Automatic Reference Selection
Figure 7



The operational mode is according to the following state diagram:

Automatic Operational Mode Selection
Figure 8



Output Signals and Frequency

Sync_Clk is the primary chip output, and in locked mode is synchronized to the selected reference. **Sync_Clk** may be any of the following frequencies: 12.96 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, or 77.76 MHz The frequency is determined by the choice of VCXO. See **External Component Selection** section. Operation at 155.52 MHz is also permitted with a 155.52 MHz VCXO, and requires a PECL buffer to provide the main clock output. (See **Application Notes/Peripherals** section). Device PECL VCXO clock input also needs to be selected (via the **VC_Sel** pin). When PECL outputs are selected, the **Sync_Clk** output is disabled.

Sync_8K is an 8 kHz output available as a frame reference or may be used as a synchronization signal for cross-coupled pairs of STC3500 devices operated in master/slave mode. **Sync_8K** may be a 50% duty cycle signal, or variable high-going pulse width, as determined by the **Ctl_Mode** and **Fr_Pulse_Width** registers. In variable pulse width mode, the width may be from 1 to 15 multiples of the **Sync_Clk** cycle time. See **Register Descriptions and Operation** section.

Sync_2K is a 2 kHz multi-frame sync output. It may be a 50% duty cycle signal, or variable high-going pulse width, as determined by the **Ctl_Mode** and **Fr_Pulse_Width** registers. In variable pulse width mode, the width may be from 1 to 15 multiples of the **Sync_Clk** cycle time. See **Register Descriptions and Operation** section.

These three output signals are phase aligned, and in locked mode are synchronized to the selected reference. In slave mode, they are in phase with the **Xref** input, offset by the value written to the **Phase_Offset** register (+31.75 to -32nS, with .25nS resolution).

BITS_Clk is the BITS clock output at either 1.544 MHz or 2.048 MHz It is selected by the **BITS_Sel** input and its state may be read in bit 2 of the **Ctl_Mode** register. When **BITS_Sel** = 1, the BITS frequency is 1.544 MHz and when **BITS_Sel** = 0, the BITS frequency is 2.048 MHz. This output clock is digitally synthesized from **SYNC_CLK** directly and will be synchronized to **SYNC_8k** and **SYNC_2k**.

Hold Over History Accumulation and Maintenance

To be provided.

Interrupts

Eight interrupts are provided and appear in the **INTR_EVENT (0x12)** register. Each interrupt can be individually enabled or disabled via the **INTR_ENABLE (0x13**) register. Each bit enables or disables the corresponding interrupt from asserting the **SPI_INT** pin. Interrupt events still appear in the **INTR_EVENT (0x12)** register independent of their enable state. All interrupts are cleared once **INTR_EVENT (0x12)** register is read. The interrupts provided are:

- Any reference changing from available to not available
- Any reference changing from not available to available
- Xref changing from activity to no activity
- Xref changing from no activity to activity
- DPLL Mode status change
- Reference switch in automatic reference selection mode
- Loss of Signal
- Loss of Lock

Interrupts and Reference change in Autonomous mode – Interrupts can be used to determine the cause of a reference change in autonomous mode. Let us assume that the module is currently locked to REF1. The module switches to REF2 and SPI_INT pin is asserted. The user reads the **INTR_EVENT (0x12)** register.

If the module is operating in autonomous non-revertive mode, the cause can be determined from bits4, 5, 6 and 7. Bit5 is set to indicate Active reference change. If Bit6 is set then the cause of the reference change is Loss of Active Reference. If Bit7 is set then the cause of the reference change is a Loss of Lock alarm on the active reference.

If the module is operating in autonomous revertive mode, the cause can be determined from bits1, 4,5, 6 and 7. Bit5 is set to indicate Active reference change. If Bit6 is set then the cause of the reference change is Loss of Active Reference. If Bit7 is set then the cause of the reference change is a Loss of Lock alarm on the active reference. If Bit1 is set then the cause of the reference change is the availability of a higher priority reference.

Note: The DPLL Mode Status Change bit (Bit4) is also set to indicate a change in **DPLL_STATUS (0x11)** register, during an interrupt caused by a reference change. The data in **DPLL_STATUS (0x11)** register however is not useful in determining the cause of a reference change. This is because bits0-2 of this register always reflects the status of the current active reference and hence cannot be used to determine the status of the last active reference.

Interrupts in Manual Mode – In manual operating mode, when the active reference fails due to a Loss of Signal or Loss of Lock alarm, an interrupt is generated. For example, in case of a Loss of Signal, bits4 and 6 of **INTR_EVENT (0x12)** register would be set to indicate Loss of Signal and DPLL Mode Status Change. The user may choose to read the **DPLL_STATUS (0x11)** register, though in manual mode bit6 of **INTR_EVENT (0x12)** register is a mirror of bit0 of **DPLL_STATUS (0x11)** register. This holds true for a Loss of Lock alarm, where bit7 of **INTR_EVENT (0x12)** register is a mirror of bit1 of **DPLL_STATUS (0x11)** register.

OCXO/TCXO Calibration

The OCXO/TCXO may be calibrated by writing a frequency offset v.s. nominal frequency into the **Calibration** register. This calibration is used by the synchronization software to create a frequency corrected from the actual OCXO/TCXO output by the value written to the **Calibration** register. See **Register Descriptions and Operation** section.

Register Descriptions and Operation

Chip_ID_low, 0x00 (R)

Bit 7 ~ Bit 0
Low byte of chip ID: 0x12

Chip_ID_High, 0x01 (R)

Bit 7 ~ Bit 0
High byte of chip ID: 0x30

Chip_Revision, 0x02 (R)

Bit 7 ~ Bit 0
Chip revision number: Chip revision number is subject to change.

Bandwidth, 0x03 (R/W)

Bit 7 ~ Bit 4	Bit 3 ~ Bit 0
Reserved	Bandwidth Selection in Hz: 0000 - 0101: 0.025 0110: 0.049 0111: 0.098 (Reset Default) 1000: 0.20 1001: 0.39 1010: 0.78 1011 - 1111: 1.6

Bits 3 - 0 select the phase lock loop bandwidth in Hertz. The reset default is .098 Hz.

Ctl_Mode, 0x04 (R/W)

Bit 7 ~ Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Synk 2K 2 kHz Pulse width control: 0: 50% 1: Controlled by FR_Pulse_Width register Default: 0	Sync 8K 8 kHz Pulse width control: 0: 50% 1: Controlled by FR_Pulse_Width register Default: 0	BITS Clock Output Frequency: 1: 1.544 MHz 0: 2.048 MHz (read only)	HM Ref: 1: Sel0-3 pin control of op mode/ref 0: Register control of op model/ref (read only)	Active Reference Selection: 1: Manual 0: Automatic Default: 1	Input Reference Frequency Selection: 1: Manual 0: Automatic Default: 0

When bit 0 is reset (automatic frequency selection), bits 4 - 7 of the **Ref_Frq_Priority** registers become read-only. When bit 1 is reset (automatic reference and mode selection), bits 3 - 0 of the **Op_Mode** register become read-only.

The power-up default control mode is Bits 0, 4 and 5 = 0, manual reference and automatic reference frequency selection, and 50% duty cycle on **Sync_8K** and **Sync_2K**.

When **HM_Ref** = 1, enabling hardware control of reference selection, bit 1 of this register is read-only and = 1.

Bits 2 and 3 are always read-only.

Op_Mode, 0x05 (R/W)

Bit 7 ~ Bit 5	Bit 4	Bit 3 ~ Bit 0
Reserved	Master or Slave Mode 1: Master 0: Slave (read-only)	Free Run, Locked, or Hold Over: 0000: Free Run mode 0001: Locked on Ref1 0010: Locked on Ref2 0011: Locked on Ref3 0100: Locked on Ref4 0101: Locked on Ref5 0110: Locked on Ref6 0111: Locked on Ref7 1000: Locked on Ref8 1001 - 1111: Hold Over

When **HM_Ref** = 1, enabling hardware control of reference selection and operational mode control, bits 3 - 0 of this register are read-only and reflect the state of the device as set by the **SeI3-0** pin inputs.

Bit 4 of this register is read-only and follows the state of the **M/$\overline{S}$** pin.

When the device is in slave mode, it will lock to the **Xref** input, independent of the values written to bits 3 - 0 of the **Op_mode** register. The operational mode and reference selection written to bits 3 - 0 while in slave mode will, however, take effect when the device is made the master.

When bit 1 of the **Ctl_Mode** register is reset (automatic reference and mode selection) and the device is in master mode, bits 3 - 0 of the **Op_Mode** register become read-only.

Max_Pullin_Range, 0x06 (R/W)

Bit 7 ~ Bit 0
Maximum pull-in range in 0.1 ppm unit

This register should be set according to the values specified by the standards (GR-1244) appropriate for the particular stratum of operation. The power-up default value is 10 ppm (= 4.6ppm aging + 4.6ppm pullin + margin).

Xref_Activity, 0x07 (R)

Bit 7 ~ Bit 4	Bit 3 ~ Bit 0
Reserved	Xref signal/frequency 0000: No Signal 0001: 8 kHz 0100: 12.96 MHz 0101: 19.44 MHz 0110: 25.92 MHz 0111: 38.88 MHz 1000: 51.84 MHz 1001: 77.76 MHz 1010-111: Reserved

Indicates signal presence and auto-detected frequency for the **Xref** input.

Ref_Activity, 0x08 (R)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ref8 activity 1: on 0: off	ref7 activity 1: on 0: off	ref6 activity 1: on 0: off	ref5 activity 1: on 0: off	ref4 activity 1: on 0: off	ref3 activity 1: on 0: off	ref2 activity 1: on 0: off	ref1 activity 1: on 0: off

Each bit indicates the presence of a signal for that reference.

Ref_Pullin_Sts, 0x09 (R)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ref8 sts 1: in range 0: out range	ref7 sts 1: in range 0: out range	ref6 sts 1: in range 0: out range	ref5 sts 1: in range 0: out range	ref4 sts 1: in range 0: out range	ref3 sts 1: in range 0: out range	ref2 sts 1: in range 0: out range	ref1 sts 1: in range 0: out range

Each bit indicates if the reference is within the frequency range specified by the value in the **Max_Pullin_Range** register.

Ref_Qualified, 0x0a (R)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ref8 qual: 1: avail. 0: not avail.	ref7 qual: 1: avail. 0: not avail.	ref6 qual: 1: avail. 0: not avail.	ref5 qual: 1: avail. 0: not avail.	ref4 qual: 1: avail. 0: not avail.	ref3 qual: 1: avail. 0: not avail.	ref2 qual: 1: avail. 0: not avail.	ref1 qual: 1: avail. 0: not avail.

This register contains the “anded” condition of the **Ref_Activity** and **Ref_Pullin_Sts** registers for each of the **Ref1-8** inputs, qualified for 10 seconds. When a reference signal has been present for > 10 seconds and is within the pull-in range, it’s bit is set.

Ref_Mask, 0x0b (R/W)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ref8 mask: 1: avail. 0: not avail. Default: 0	ref7 mask: 1: avail. 0: not avail. Default: 0	ref6 mask: 1: avail. 0: not avail. Default: 0	ref5 mask: 1: avail. 0: not avail. Default: 0	ref4 mask: 1: avail. 0: not avail. Default: 0	ref3 mask: 1: avail. 0: not avail. Default: 0	ref2 mask: 1: avail. 0: not avail. Default: 0	ref1 mask: 1: avail. 0: not avail. Default: 0

Individual references may be marked as “use” or “no use” for selection in the automatic reference selection mode (bit 1 = 0 in the **Ctl_Mode** register). The reset default value is 0, “no use”. In manual reference selection, either hardware or register controlled, the reference masks have no effect, but do remain valid and are applied upon a transition to automatic mode.

Ref_Available, 0x0c (R)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ref8 avail: 1: avail. 0: not avail.	ref7 avail: 1: avail. 0: not avail.	ref6 avail: 1: avail. 0: not avail.	ref5 avail: 1: avail. 0: not avail.	ref4 avail: 1: avail. 0: not avail.	ref3 avail: 1: avail. 0: not avail.	ref2 avail: 1: avail. 0: not avail.	ref1 avail: 1: avail. 0: not

This register contains the “anded” condition of the **Ref_Qualified** and **Ref_Mask** registers.

Ref_Rev_Delay, 0x0d (R/W)

Bit 7 ~ Bit 0
Reference reversion delay time, 0 - 255 minutes. default = 0000 0101, 5 minutes

In automatic reference selection mode, when a reference fails and later returns, it must be available for the time specified in the **Ref_Rev_Delay** register before it can be switched back to as the active reference (if the new reference was marked as “revertive”). See Figure 7.

Phase_Offset, 0x0e (R/W)

Bit 7 ~ Bit 0
The 2's complement value of phase offset between Sync_8K and Xref, ranges from -32 nS to +31.75 nS Positive Value: Sync_8K rising edge leads Xref Negative Value: Sync_8K rising edge lags Xref

In slave mode, the slave's outputs may be phase shifted -32nS to +31.75nS in .25nS increments, relative to **Xref** according to the contents of the **Phase_Offset** register, to compensate for the path length of the **Sync_8K** or **Sync_Clk** to **Xref** connection.

If a phase offset is used, then the two STC3500 devices would typically be written to the appropriate phase offset values for the respective path lengths of each **Sync_8K** or **Sync_Clk** to **Xref** connection, to ensure that the same relative output signal phases will persist through master/slave switches.

Calibration, 0x0f (R/W)

Bit 7 ~ Bit 0
2's complement value of local oscillator digital calibration in 0.05 ppm resolution

To digitally calibrate the free running clock synthesized from OCXO/TCXO, this register is written with a value corresponding to the known frequency offset of the oscillator from the nominal center frequency.

Fr_Pulse_Width, 0x10 (R/W)

Bit 7 ~ Bit4	Bit 3 ~ Bit 0
Reserved	Pulse width for Sync_8K and Sync_2K clock outputs, 1-15 multiples of the Sync_Clk clock period.

Bits 4 and 5 of the **Ctl_Mode** register determine if the **Sync_8K** 8 kHz and/or **Sync_2K** 2 kHz outputs are 50% duty cycle or pulsed (high going) outputs. When they are pulsed, the **Fr_Pulse_Width** register determines the width. Width is the register value multiple of the **Sync_Clk** clock period. Valid values are 1 - 15. The same pulse width is applied to both **Sync_8K** and **Sync_2K**. Reset default is 0001. Writing to 0000 maps to 0001.

DPLL_Status, 0x11 (R)

Bit 7 ~ Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Hold Over Build Complete 1: Hold Over history build complete 0: Hold Over history build not complete	Hold Over Available 1: Avail. 0: Not avail.	Locked 1: Locked 0: Not locked	Loss of Lock 1: Loss of Lock 0: No loss of lock	Loss of Signal 1: No activity on active reference 0: Active reference signal present

Bit 0 indicates the presence of a signal on the selected reference.

Bit 1 indicates a loss of lock (LOL). Loss of lock will be asserted if lock is not achieved within the specified time for the stratum of operation, or lock is lost after previously having been established. LOL will not be asserted for automatic reference switches.

Bit 2 indicates successful phase lock. It will typically be set in <100 seconds, with a good reference. It will indicate "not locked" if lock is lost.

Bit 3 indicates if a Hold Over history is available.

Bit 4 indicates when a new Hold Over history has been successfully built and transferred to the active Hold Over history.

Intr_Event, 0x12 (R)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Loss of Lock	Loss of Signal	Active reference change	DPLL Mode status change	Xref Change from no activity to activity	Xref Change from activity to no activity	Any reference change from not available to available	Any reference change from available able to not available

Interrupt state = 1. When an enabled interrupt occurs, the **$\overline{\text{INTR}}$** pin is asserted, active low. All interrupts are cleared and the **$\overline{\text{INTR}}$** pin pulled high when the register is read. Reset default is 0.

Intr_Enable, 0x13 (R/W)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Enable Interrupt event 7 1: Enable 0: Disable Default: 0	Enable Interrupt event 6 1: Enable 0: Disable Default: 0	Enable Interrupt event 5: 1: Enable 0: Disable Default: 0	Enable Interrupt event 4: 1: Enable 0: Disable Default: 0	Enable Interrupt event 3: 1: Enable 0: Disable Default: 0	Enable Interrupt event 2: 1: Enable 0: Disable Default: 0	Enable Interrupt event 1: 1: Enable 0: Disable Default: 0	Enable Interrupt event 0: 1: Enable 0: Disable Default: 0

Enables or disables the corresponding interrupts from asserting the **$\overline{\text{INTR}}$** pin. Interrupt events still appear in the **Intr_Event** register independent of their “enable” state. Reset default is interrupts disabled.

Ref(1-8)_Frq_Offset, 0x14 ~ 0x1b (R)

Bit 7 ~ Bit 0
2’s complement value of frequency offset between reference and calibrated local oscillator, 0.2 ppm resolution

These registers indicate the frequency offset, in 0.2 ppm resolution, between each reference and the local calibrated oscillator. 0x14 - 0x1b correspond to **Ref1 - Ref8**.

Ref(1-8)_Frq_Priority, 0x1c ~ 0x23 (R/W)

Bit 7 ~ Bit 4	Bit 3	Bit 2 ~ Bit 0
Frequency 0000: None 0001: 8 kHz 0010: 1.544 MHz 0011: 2.048 MHz 0100: 12.96 MHz 0101: 19.44 MHz 0110: 25.92 MHz 0111: 38.88 MHz 1000: 51.84 MHz 1001: 77.76 MHz 1010-1111: Reserved	Revertivity 1: revertive 0: non-revertive Default: 0, non revertive	Priority 0: highest 7: lowest Default: 0

Bits 2 - 0 indicate the priority of each reference for use in automatic reference selection mode (bit 1 of the **Ctl_Mode** register =0). In manual reference selection mode (bit 1 of the **Ctl_Mode** register = 1 or **HM_Ref** = 1), these bits are read-only and will contain either the reset default or values written when last in automatic reference selection mode. For equal priority values, lower reference numbers have higher priority.

Bit 3 specifies if the reference is revertive or non-revertive in automatic reference selection mode. When a reference fails, the next highest priority “available” (signal present, non-masked, and acceptable frequency offset) reference will be selected. When a reference returns, it will be switched to only if it is of higher priority and the current active reference is marked “Revertive”.

Bits 7 - 4 indicate the auto-detected frequency for each reference. Invalid frequencies may result in erroneous device operation. If there is no activity on a reference, bits 7-4 will be = 0000. Bits 7 - 4 are read only.

Registers 0x1c - 0x23 correspond to **Ref1** - **Ref8**.

Free Run_Priority, 0x24 (R/W)

Bit 7 ~ Bit 5	Bit 4	Bit 3	Bit 2 ~ Bit 0
	Enable/disable 1: enabled 2: disabled 0: Default, disabled	revertivity 1: revertive 0: non-revertive 0: Default, non-revertive	priority 0: highest 7: lowest 0: Default

Free Run may be treated like a reference. When it is enabled, Free Run will be entered when all references of higher priority are lost or masked. If/when a higher priority reference returns, it is switched if Free Run is set as “revertive”. When disabled, Free Run will be entered only if manually selected, or all references fail and no Hold Over history is available. For equal priority value, Free Run will be treated as lower priority.

History_Policy, 0x25 (R/W)

Bit 7 ~ Bit 1	Bit 0
Reserved	Reference switch Hold Over History Policy 0: rebuild 1: continue

Bit 0 determines if Hold Over history is retained or rebuilt when a reference switch occurs. See **Application Notes, Hold Over History Accumulation and Management** section.

History_Cmd, 0x26 (R/W)

Bit 7 ~ Bit 5	Bit 1 ~ 0
Reserved	Hold Over history commands 01: Save active history to backup history 10: Restore active history from backup 11: Flush the active history and accumulated register 00: No command

Bits 0-1 are written to save a Hold Over history to the backup history, restore the active Hold Over history from the backup, or flush the active history. The default value of the register is 00. The last command is latched and may be ready by the application. A flush does not affect the back up history. See **Application Notes, Hold Over History Accumulation and Management** section.

Hold Over_Time, 0x27 (R)

Bit 7 ~ Bit 0
Indicates the time since entering the Hold Over state. From 0 to 255, one bit per hour. Zero in non-Hold Over state, stops at 255.

Cfgdata, 0x30 (R/W)

Bit 7 ~ Bit 0
Configuration data write register

Configuration data is written to this register. See **Application Notes**, **Configuration Data** section.

Cfgctr_Lo, 0x31 (R)

Bit 7 ~ Bit 0
Configuration data write counter low byte

Low order byte of configuration data write counter. See **Application Notes**, **Configuration Data** section. Initialized to zero on power-up/reset.

Cfgctr_Hi, 0x32 (R)

Bit 7 ~ Bit 0
Configuration data write counter high byte

High order byte of configuration data write counter. See **Application Notes**, **Configuration Data** section. Initialized to zero on power-up/reset.

Chksum, 0x33 (R)

Bit 7 ~ Bit 1	Bit 0
Reserved	Configuration Data checksum pass/fail indicator: 0 = fail, 1 = pass

Checksum verification register for configuration data. See **Application Notes**, **Configuration Data** section. Initialized to zero on power-up/reset, indicates 0 = fail or 1 = pass upon configuration data pump completion.

EE_Mode, 0x36 (R/W)

Bit 7 ~ Bit 1	Bit 0
Reserved	EEPROM write enable: 0 = disabled, 1 = enabled

EEPROM write enable register. See **Application Notes**, **General**, **Reading and Writing EEPROM Data** section.

EE_Cmd, 0x37 (R, W)

Bit 7	Bit 6 ~ Bit 2	Bit 1 ~ 0
EEPROM read/write ready bit: 0 = not ready 1 = ready	Reserved	EEPROM read/write command bits: 00: Reset FIFO 01 = Write command 10 = Read command

EEPROM read/write command register. See **Application Notes**, **General**, **Reading and Writing EEPROM Data** section.

EE_Page_Num, 0x38 (R, W)

Bit 7 ~ Bit 0
EEPROM read/write page number, 0x00 to 0x9f (0 - 159)

EEPROM read/write page number register. EEPROM consists of 160 pages. See **Application Notes**, **General**, **Reading and Writing EEPROM Data** section.

EE_FIFO_Port, 0x39 (R, W)

Bit 7 ~ Bit 0
EEPROM read/write FIFO data

EEPROM read/write FIFO port register. EEPROM data is written to/read from here. See **Application Notes**, **General**, **Reading and Writing EEPROM Data** section.

Performance Definitions

Jitter and Wander – Jitter and wander are defined respectively as “the short-term and long-term variations of the significant instants of a digital signal from their ideal positions in time”. They are therefore the phase or position in time modulations of a digital signal’s transitions’s transitions relative to their ideal positions. These phase modulations can in turn be characterized in terms of their amplitude and frequency. Jitter is defined as those phase variations at rates above 10 Hz, and wander as those variations at rates below 10 Hz.

Fractional frequency offset and drift – The fractional frequency offset of a clock is the ratio of the frequency error (from the nominal or desired frequency) to the desired frequency. It is typically expressed as (n parts in 10^{x}), or (n x 10^{-x}).

Drift is the measure of a clock’s frequency offset over time. It is expressed the same way as offset.

Time Interval Error (TIE) – TIE is a measure of wander and is defined as the variation in the time delay of a given signal relative to an ideal signal over a particular time period. It is typically measured in nS. TIE is set to zero at the start of a measurement, and thus represents the phase change since the beginning of the measurement.

Maximum Time Interval Error (MTIE) – MTIE is a measurement of wander that finds the peak-to-peak variations in the time delay of a signal for a given window of time, called the observation interval (τ). Therefore it is the largest peak-to-peak TIE in any observation interval of length τ within the entire measurement window of TIE data. MTIE is therefore a useful measure of phase transients, maximum wander and frequency offsets. MTIE increases monotonically with increasing observation interval.

Time Deviation (TDEV) – TDEV is a measurement of wander that characterizes the spectral content of phase noise. TDEV(τ) is the RMS of filtered TIE, where the bandpass filter is centered on a frequency of 0.42/τ.

STC3500 performance

Input Jitter Tolerance – Input jitter tolerance is the amount of jitter at its input a clock can tolerate before generating an indication of improper operation. GR-1244 and ITU-813 requirements specify jitter amplitude v.s. jitter frequency for jitter tolerance. The STC3500 device provides jitter tolerance that meets the specified requirements.

Input Wander Tolerance – Input wander tolerance is the amount of wander at its input a clock can tolerate before generating an indication of improper operation. GR-1244 and ITU-813 requirements specify input wander TDEV v.s. integration time as shown below.

Integration Time, τ (seconds)	TDEV (nS)
$0.05 \leq \tau < 10$	100
$10 < \tau < 1000$	$31.6 \times \tau^{0.5}$
$1000 \leq \tau$	N/A

The STC3500 device provides wander tolerance that meets these requirements.

Phase Transient Tolerance – GR-1244 specifies maximum reference input phase transients that a clock system must tolerate without generating an indication of improper operation. The phase transient tolerance is specified in MTIE(nS) v.s. observation time from .001 to 100 seconds, as shown below.

Observation time S (Seconds)	MTIE (nanoseconds)
0.001326 ≤ S < 0.0164	61,000 x S
0.0164 < S < 1.97	925 + 4600 x S (only for Stratum 3)
1.97 ≤ S	10,000 (only for Stratum 3)

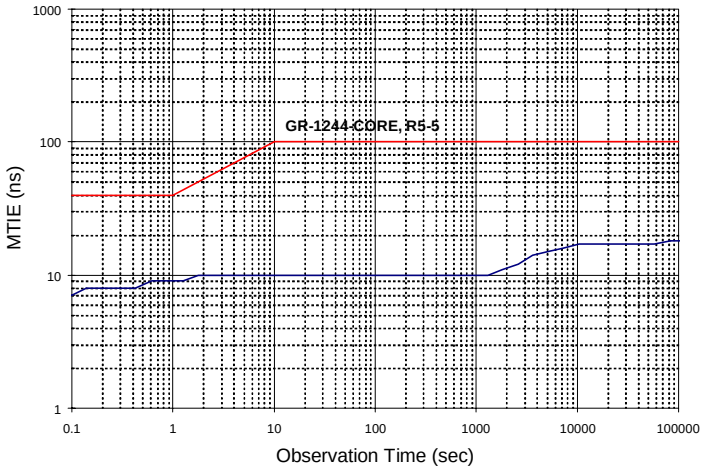
The STC3500 will tolerate all reference input transients within the GR-1244 specification.

Free Run Frequency Accuracy – Free Run frequency accuracy is the maximum fractional frequency offset while in Free Run mode. It is determined by the accuracy of the TCXO/OCXO. All TCXO/OCXO devices recommended for use with the STC3500 in the application section will meet GR-1244 and ITU G.813 requirements.

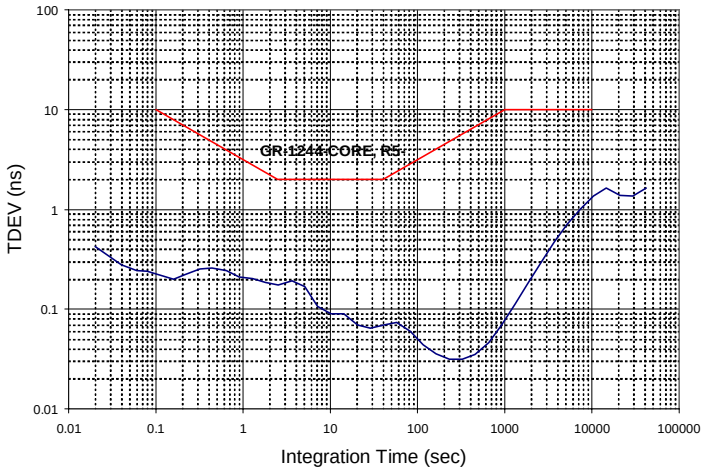
Hold Over Frequency Stability – Hold Over frequency stability is the maximum fractional frequency offset while in Hold Over mode. It is determined by the stability of the TCXO/OCXO. All TCXO/OCXO devices recommended for use with the STC3500 in the application section will meet GR-1244 and ITU G.813 requirements.

Wander Generation – Wander generation is the process whereby wander appears at the output of a clock in the absence of input wander. The STC3500 wander generation characteristics, MTIE and TDEV, are shown below, along with the requirements masks (bandwidth = 0.34 Hz):

Wander Generation Characteristics – MTIE



Wander Generation Characteristics – TDEV



Wander Transfer – Wander transfer is the degree to which input wander is attenuated (or amplified) from input to output of a clock.

Integration time, τ (seconds)	Stratum 3 TDEV (nanoseconds)
$\tau < 0.05$	N/A
$0.05 \leq \tau < 0.1$	$1020 \times \tau$
$0.1 \leq \tau < 1.44$	102
$1.44 \leq \tau < 10$	102
$10 \leq \tau < 300$	$32.2 \times \tau^{0.5}$
$300 \leq \tau \leq 1000$	$32.2 \times \tau^{0.5}$
$1000 < \tau$	N/A

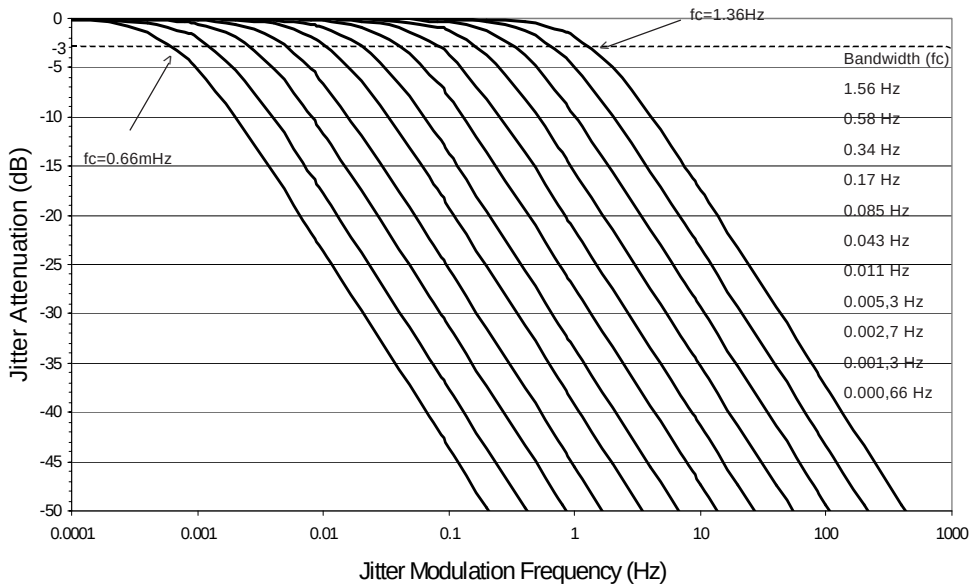
The STC3500, when configured for the appropriate stratum 3 bandwidth frequency, meets the stratum 3 requirements,

Jitter Generation – Jitter generation is the process whereby jitter appears at the output of a clock in the absence of input jitter. The device jitter generation performance is as shown below:

Jitter	STC3500 Performance	Requirement, p-p
Broadband	< 6 pS RMS, < 50 pS p-p	T1/E1:32 nS
500 Hz - 1.3 MHz	< 1.5 pS RMS	T1/E1: 32 nS, STM-1: 3.21nS
65 kHz - 1.3 MHz	< 1 pS RMS	T1/E1: 32 nS, STM-1: 643 pS

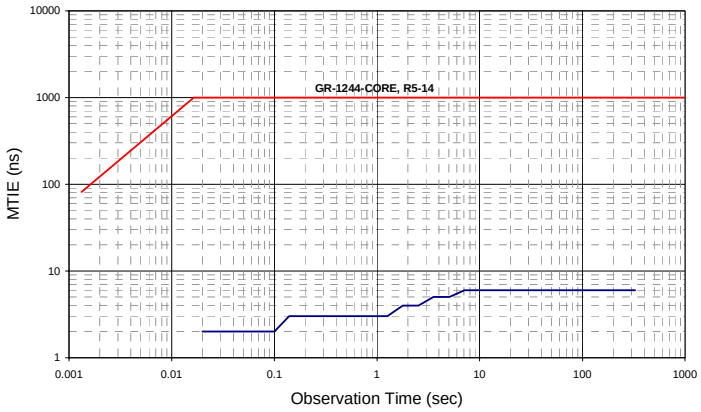
Jitter Transfer – Jitter transfer is the degree to which input jitter is attenuated (or amplified) from input to output of a clock. It is a function of the selected bandwidth. The STC3500 jitter transfer characteristics are shown below:

Jitter Transfer Characteristics

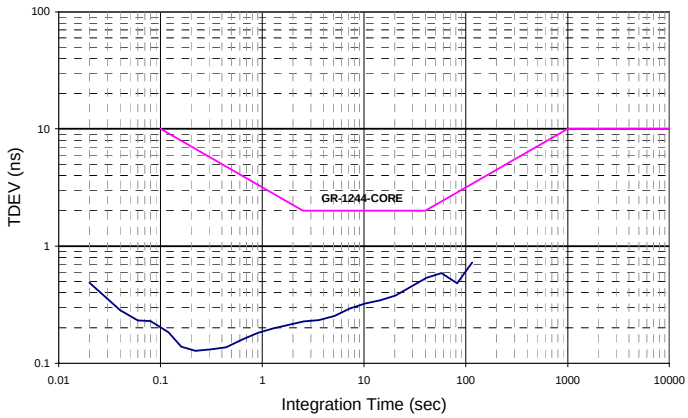


Phase Transients – A phase transient is an unusual step or change in the phase-time of a signal over a relatively short time period. This may be due to switching between equipment, reference switching, diagnostics, entry or exit to/from Hold Over, or input reference transients. The STC3500 performance for reference switches is shown below (loop bandwidth = 0.098 Hz):

Phase Transients – MITE



Phase Transients – TDEV



Capture Range and Lock Range – Capture range and lock range are the maximum frequency errors on the reference input within which the phase locked loop is able to achieve lock and hold lock, respectively. The STC3500 stratum 3 performance is shown below:

Characteristic	STC3500	Requirement
Capture range	± 15 ppm	± 4.6 ppm
Lock in range	± 15 ppm	N/A

This is the minimum chip capability, and guarantees the ability to capture and lock with a reference that is offset the maximum allowed in one direction in the presence of an OCXO/TCXO that is offset the maximum in the opposite direction (4.6 ppm + 4.6 ppm = 9.2 ppm).

Master/Slave Skew, Reference switch settling time, and Phase Build-Out resolution – Master/Slave Skew, Reference switch settling time, and Phase Build-Out resolution performance are shown below:

Characteristic	STC3500	Requirement
Master/Slave phase skew	< 2 nS	N/A
Reference switch settling time	Stratum 3: < 100 sec. up to 20 ppm frequency offset	Stratum 3: < 100 sec. up to +/- 4.6 ppm frequency offset
Phase Build-Out resolution	1 nS	< 50 nS

Application Notes

This section describes typical application use of the STC3500 device. The General section applies to all application variations, while the remaining sections detail use depending on the level of control and automatic operation the application desires.

General

Power and Ground – Well-planned noise-minimizing power and ground are essential to achieving the best performance of the device. The device requires 2.5V and 3.3V digital power and 2.5V analog power input. All digital I/O is at 3.3V, LVTTL compatible. The 2.5V may originate from a common source but should be individually filtered and isolated, as shown in Figure 9. Alternatively, a separate 2.5V regulator may be used for the analog 2.5 volts. R/C filter components should be chosen for minimum inductance and kept as close to the chip as possible.

Note the ferrite bead power filter and bypass capacitors associated with the oscillator power. Mount the bypass capacitors as close to the oscillators as possible. Oscillator and EEPROM ground is the digital ground.

It is desirable to provide individual bypass capacitors, located close to the chip, for each of the digital power input leads, subject to board space and layout constraints. On power-up, it is desirable to have the 3.3V either lead or be coincident with, but not lag the application of 2.5V.

Digital ground should be provided by as continuous a ground plane as possible. While the analog and digital grounds are tied together inside the chip, it is recommended that they be tied together externally at a single point close to the chip as well.

Peripherals – Peripheral connections are also shown in Figure 9:

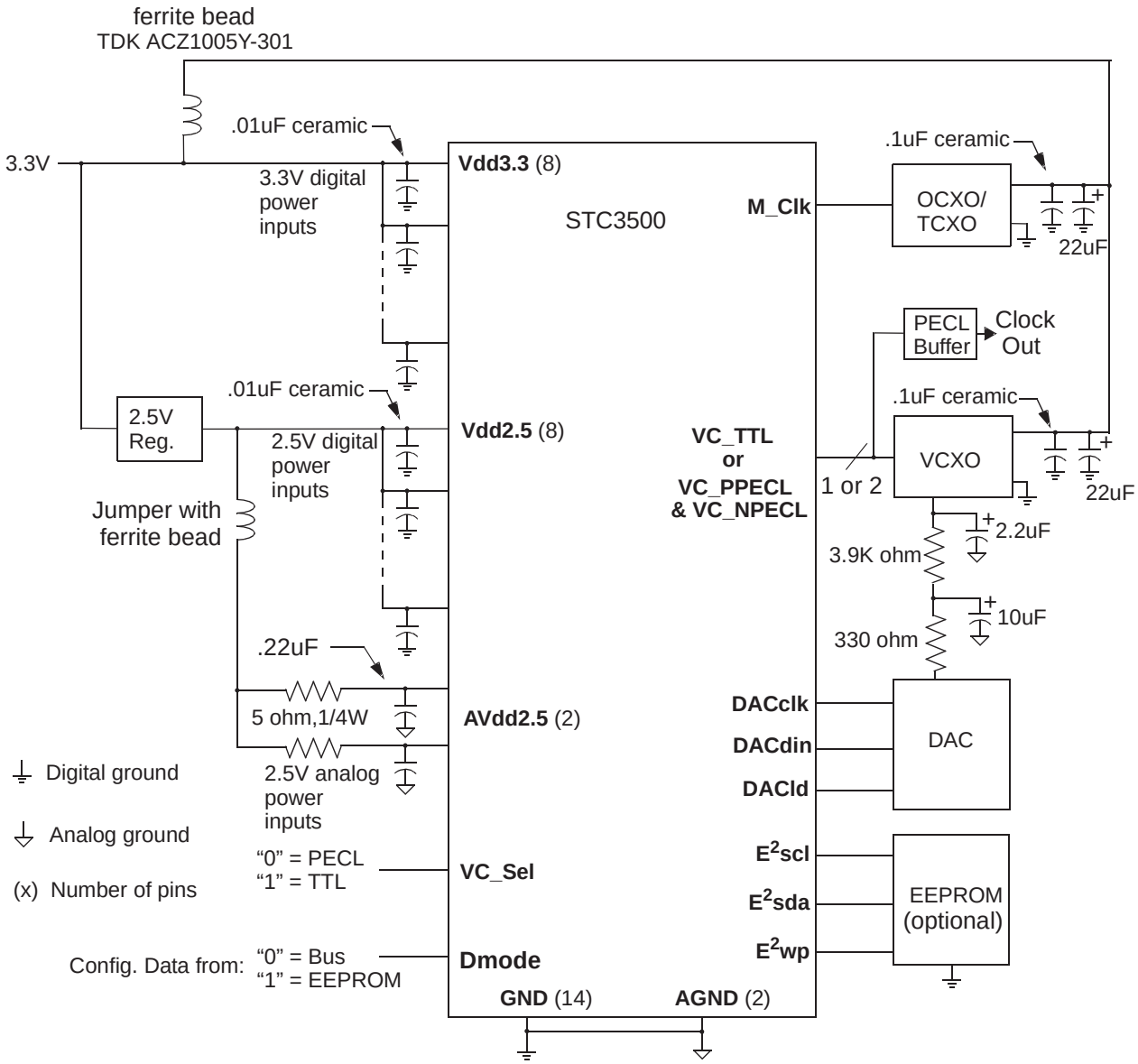
The OCXO/TCXO output is connected to the **M_Clk** pin. VCXOs up to 77.76 MHz connect to the **VC_TTL** pin, and the device is configured for TTL input by tying the **VC_Sel** pin high. If the VCXO is at 155.52 MHz, its output will typically be PECL compatible and should be connected to the **VC_PPECL** and **VC_NPECL** pins. Tie the **VC_Sel** pin low for PECL input. For 155.52 MHz operation, a PECL buffer will also need to be provided for the 155.52 MHz clock output.

Digital to analog converter clock, data, and chip select connect to pins **DACclk**, **DACdin**, and **DACld**, respectively. The DAC output is connected to the VCXO input through a simple R/C filter as shown in Figure 9 below. The capacitors preferably are tantalum.

If the optional EEPROM is included, serial clock, serial data, and WP connect to pins **E²scl**, **E²sda**, and **E²wp**, respectively. The **Dmode** pin selects the source for configuration data, 0 = from the bus interface, 1 = from the EEPROM.

Power Input, Filtering and Peripheral Connections

Figure 9



Environment – The maximum device power dissipation is 2 W. Board layout and device location need to account for adequate cooling.

All device input and output signal levels are 3.3V LVTTL (Except **VC_PPECL** and **VC_NPECL**, which are LVPECL).

External Component Selection – Following are the recommended external components to be used with the STC3500. The device pins to which they connect are also shown. The main oscillator may be an OCXO or TCXO:

Component Selections

Table 8

Component	Vendor	Part Number/Description	Device Pins
OCXO (CT only)	Connor-Winfield	ASOF3S3 12.8 MHz AGOF3S3 12.8 MHz	OCXO
OCXO (IT only)	Connor-Winfield	DSOF3S3 12.8 MHz BGOF3S3 12.8 MHz	OCXO
TCXO (CT range only)	Connor-Winfield	T-501	TCXO
VCXO (CT range)	Connor-Winfield	VKB52B2 (- Sync_Clk frequency)	VCXO
VCXO (IT range)	Connor-Winfield	VKB62B2 (- Sync_Clk frequency)	VCXO
DAC	Linear Technology	LTC1655LCS8	DACclk, DACdin, DACld
EEPROM (Optional)	Atmel	AT24C64N-10SI-2.7	E^2scl, E^2sda, E^2wp

The VCXO determines the **Sync_Clk** output frequency. Acceptable output frequencies are: 12.96 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz 51.84 MHz, 77.76 MHz, or 155.52 MHz. The device will operationally autodetect the output frequency.

The EEPROM is optional, and is required to hold device configuration data if the application intends to operate in hardware control mode only (No bus interface). If the bus interface is used, the application may provide the configuration data pump, and no EEPROM is required. See **Application Notes**, **Configuration Data** section.

Reference Inputs – The application may supply up to 8 reference inputs, applied at input pins **Ref1 - 8**. They may each be 8 kHz, 1.544 MHz, 2.048 MHz, 19.44 MHz, 38.88 MHz, or 77.76 MHz. The device auto-detects frequency in the hardware control modes, and may auto-detect or have the frequency written to registers in register control mode, as described in the control mode sections that follow.

References would typically (but need not be) connected in decreasing order of usage priority. For example if redundant BITS clocks are available, they would typically be assigned to **Ref1** and **Ref2**, with other transmission derived signals following thereafter.

Master/slave operation – For some applications, reliability requirements may demand that the clock system to be duplicated. The STC3500 device will support the master/slave duplicated configuration for such applications. To facilitate it's use, the device includes the necessary signal cross coupling and control functions. Redundancy for reliability implies two major considerations: 1) Maintaining separate failure groups such that a failure in one group does not affect it's mate, and 2) Physical and logical partitioning for repair, such that a failed component can be replaced while the mate remains in service, if so desired. System design needs to account for these appropriately for system level goals to be met.

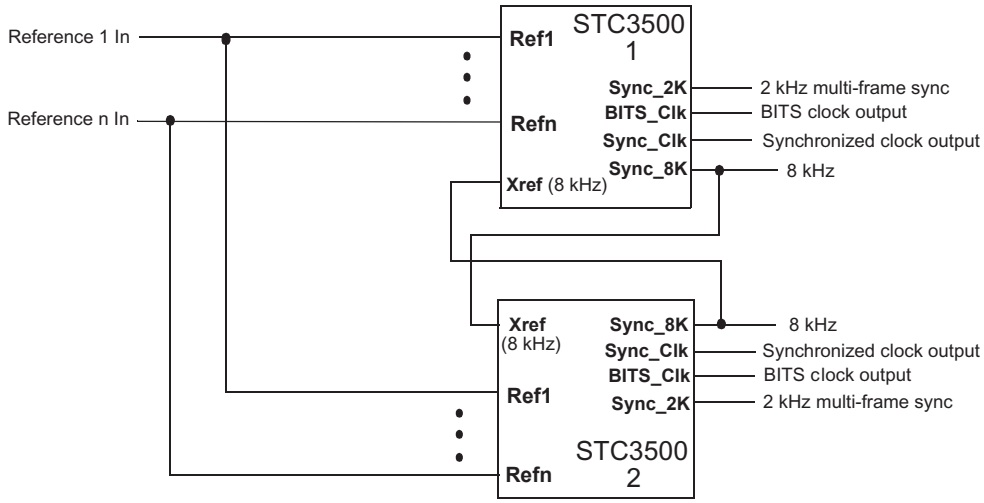
Master/Slave Configuration – A pair of devices are interconnected by cross-coupling their respective **Sync_8K** or **Sync_Clk** outputs to the other device's **Xref** input (See Figure 10). Note that 8 kHz frame phase alignment is maintained across a master/slave pair of devices only if **Sync_8K** is used as the cross couple signal.

Additionally, the reference inputs for each device would typically be correspondingly the same, so that when a Master/Slave switch occurs, synchronization would continue with the same reference. The references may be driven by the same signal directly or via separate drivers, as the redundancy of that part of the system requires. Distribution path lengths are not critical here, as a phase build-out will occur when a device switches from slave to master.

The path lengths of the two **Sync_8K** or **Sync_Clk** to **Xref** signals is of interest, however. They need not be the same. However, to accommodate path length delays, the STC3500 provides a programmable phase skew feature, which allows the application to offset the output clocks from the cross-reference signal by up to ±32 ns, in 0.25nS increments. This offset may therefore be programmed to exactly compensate for the actual path length delay associated with the particular application's cross-reference traces. The offset may further be adjusted to accommodate any output clock distribution path delay differences. Phase offset is programmed by writing to the **Phase_Offset** register, and is typically a one-time device initialization function. (See register description and **Register Access Control** sections). Thus, master/slave switches with the STC3500 devices may be accomplished with near-zero phase hits.

For applications that use Hardware Control only (i.e. phase offset programming is not available), it is desirable to keep the cross couple path lengths at a minimum and relatively equal in length, as the path length will appear as a phase hit in the slave clock output when a master/slave switch occurs in a Hardware Control configuration.

Master / Slave Configuration
Figure 10



Master/Slave Operation and Control – The Master/Slave state is always manually controlled by the application. Master or slave state of a device is determined by the **M/$\overline{S}$** pin. Choosing the master/slave states is a function of the application, based on the configuration of the rest of the system and potential detected fault conditions.

When operating in Hardware Control or Register Access Manual Control mode, it is important to set the slave reference selection the same as the master to ensure use of the same reference when/if the slave becomes master. In Register Access Manual Control mode, the **Ref_Mask** register should also be written to the same value for both devices.

Master/slave switches should be performed with minimal delay between switching the states of each of the two devices. This can be easily accomplished, for example, by controlling the master/slave state with a single signal, coupled to one of the devices through an inverter.

In the case of Register Access Automatic Control mode, where reference selection is automatic, it is necessary to read the operational mode (bits 3-0) from the master's **Op_Mode** register and write it to the slave's **Op_Mode** register. The master's reference selection will then be used by the slave when it becomes master. In addition to having the references populated
the same, and in the same order for both devices, it is desireable to write the reference frequency and priority registers **Ref(1-8)_Frq_Priority** and the **Ref_Mask** registers to the same values for both devices to ensure seamless master/slave switches.

Reset – Device reset is an initialization time function, which resets internal logic and register values. A reset is performed automatically when the device is powered up. Registers return to their default values, as noted in the register descriptions. Device mode and functionality following a reset are determined by the state of the various hardware control pins.

Configuration Data – Following any device reset, either via power-up or operation of the **Reset** pin, the device needs to be loaded with its DPLL configuration data. This data may come from either an external EEPROM, or the bus interface. The **Dmode** pin selects the source for configuration data, 0 = from the bus interface, 1 = from the EEPROM. If the source is the EEPROM, devices pre-loaded with the data are availbale from Connor-Winfield (See **External Component Selection** section). Following a reset, the device automatically pumps the the data from the EEPROM.

If the data is to be application provided through the bus interface, the data is available from Connor-Winfield as a file and is loaded per the following procedure in Table 9:

Configuration Data Registers

Table 9:

0x30	Cfgdata
0x31	Cfgctr_Lo
0x32	Cfgctr_Hi
0x33	Chksum

Table 9 shows the registers associated with the configuration data and pumping process. The configuration file size is 7424 bytes. Following a reset, the pumping process consists of simply writing the 7424 bytes to the **Cfgdata** register. Each write increments the **Cfgctr_Lo/Hi** counter registers, which are initialized to 0x00 after reset. Completion of pump coincides with the counter registers reaching the value of **Cfgctr_Lo/Hi** = 0x1d/ 0x00, corresponding to 7424.

The last two bytes of the configuration data contain the checksum (CRC-16), which is compared to a computed checksum in the device. The **Chksum** register indicates a correct or incorrect checksum in the bit 0 position. Bit 0 = 0 after reset, and is valid after the 7424th write to the **Cfgdata** register, and is set to 1 if the checksum is correct, 0 if it is incorrect. Further writes beyond 7424 will not affect the device.

A typical pump sequence after reset, for example, would consist of checking the **Cfgctr_Lo/Hi** and **Chksum** registers for a value of 0x00, followed by 7424 consecutive writes to the **Cfgdata** register. Then, successful completion of the pump is checked by verifying the values in the **Cfgctr_Lo/Hi** registers = 0x1d/0x00, and **Chksum** = 0x01. Incrementing **Cfgctr_Lo/Hi** values can optionally be checked while writing.

If **Dmode** = 1 and the configuration data is pumped automatically from the EEPROM, the operation of the configuration data registers is still valid. Pump completion and checksum correctness may be verified by reading the **Cfgctr_Lo/Hi** and **Chksum** registers. Writes to the **Cfgdata** register will have no effect on the device when **Dmode** = 1. In any case, writes to the **Cfgdata** register will have no effect on the device after configuration data pump is complete.

Reading and Writing EEPROM Data – If the optional external EEPROM is provided, it may be read or written to via the bus interface. Access is provided via the following registers in Table 10 (Also see **Register Descriptions and Operation** section):

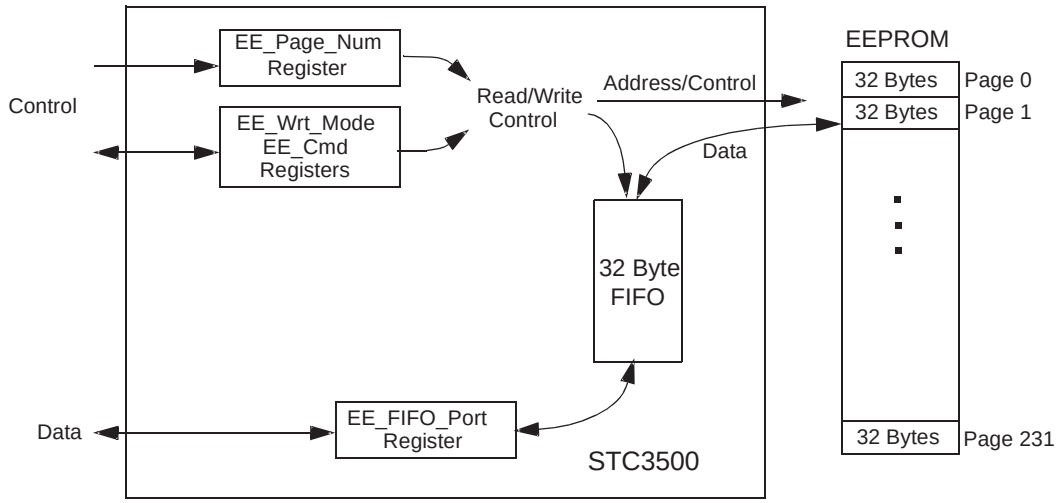
EEPROM Access Registers

Table 10:

0x36	EE_Wrt_Mode
0x37	EE_Cmd
0x38	EE_Page_Num
0x39	EE_FIFO_Port

Figure 11 shows the basic EEPROM access architecture:

EEPROM Access Architecture
Figure 11



Data in the EEPROM is organized as 232 pages of 32 bytes each. A 32 byte FIFO provides the data read/write buffering path for EEPROM accesses, and page numbers are provided by the **EE_Page_Num** register. For writes, the application loads the page number and 32 bytes of data into the FIFO. A write command then initiates the write sequence, which is completed automatically by the device. For a read, the application writes the page number, followed by a read command. The device reads the data into the FIFO, and the application retrieves the data with successive reads of the **EE_FIFO_Port** register.

Specifically, the sequence of operations to perform a write are as follows:

1) Enable writing by setting the write enable bit (write 0x01 to the **EE_Wrt_Mode** register)
2) Poll the Ready bit (bit 7 of the **EE_Cmd** register, ready = 1) until ready
3) Write the page number (0 - 231, 0x00 - 0xe7) to the **EE_Page_Num** register
4) Reset the FIFO by clearing bits 0 and 1 in the **EE_Cmd** register (write 0x00 to the **EE_Cmd** register)
5) Perform 32 successive writes to the **EE_FIFO_Port** register with the desired data for that page number
6) Issue a write command by setting the write bit (write 0x01 to the **EE_Cmd** register)
7) Poll the Ready bit (bit 7 of the **EE_Cmd** register, ready = 1) until ready
8) Disable writing by clearing the write enable bit (write 0x00 to the **EE_Wrt_Mode** register)
9) After a power-up reset, if the EEPROM loaded correctly, the **Chksum** bit in register 33 should read 1.

This sequence is repeated for each page of data desired to be written. Writing of any particular byte of data requires writing the full page. For multiple page writes, the write enable/disable operation may encapsulate the entire write sequence, i.e. it does not need to be repeated per page.

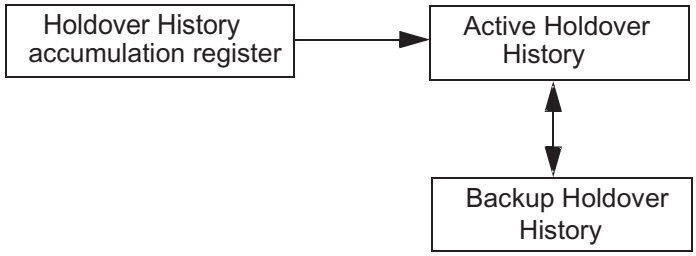
Read operations are performed as follows:

1) Poll the Ready bit (bit 7 of the **EE_Cmd** register, ready = 1) until ready
2) Write the page number (0 - 231, 0x00 - 0xe7) to the **EE_Page_Num** register
3) Set the read bit (write 0x02 to the **EE_Cmd** register)
4) Poll the Ready bit (bit 7 of the **EE_Cmd** register, ready = 1) until ready
5) Do 32 successive reads of the **EE_FIFO_Port** register to retrieve the data

This sequence is repeated for each page of data desired to be read. Reading of any particular byte of data requires reading the full page.

Aborted read or write sequences which do not complete the full 32 read or write cycles for a given page are automatically cleared by the device at the beginning of the next read or write operation.

Hold Over History Accumulation and Maintenance – Hold Over history accumulation and maintenance may be controlled in greater detail if register bus access to the device is provided. Hold Over history accumulation and control encompasses three device internal registers, three bus access registers for control and access, and two status bits in the DPLL_Status register.



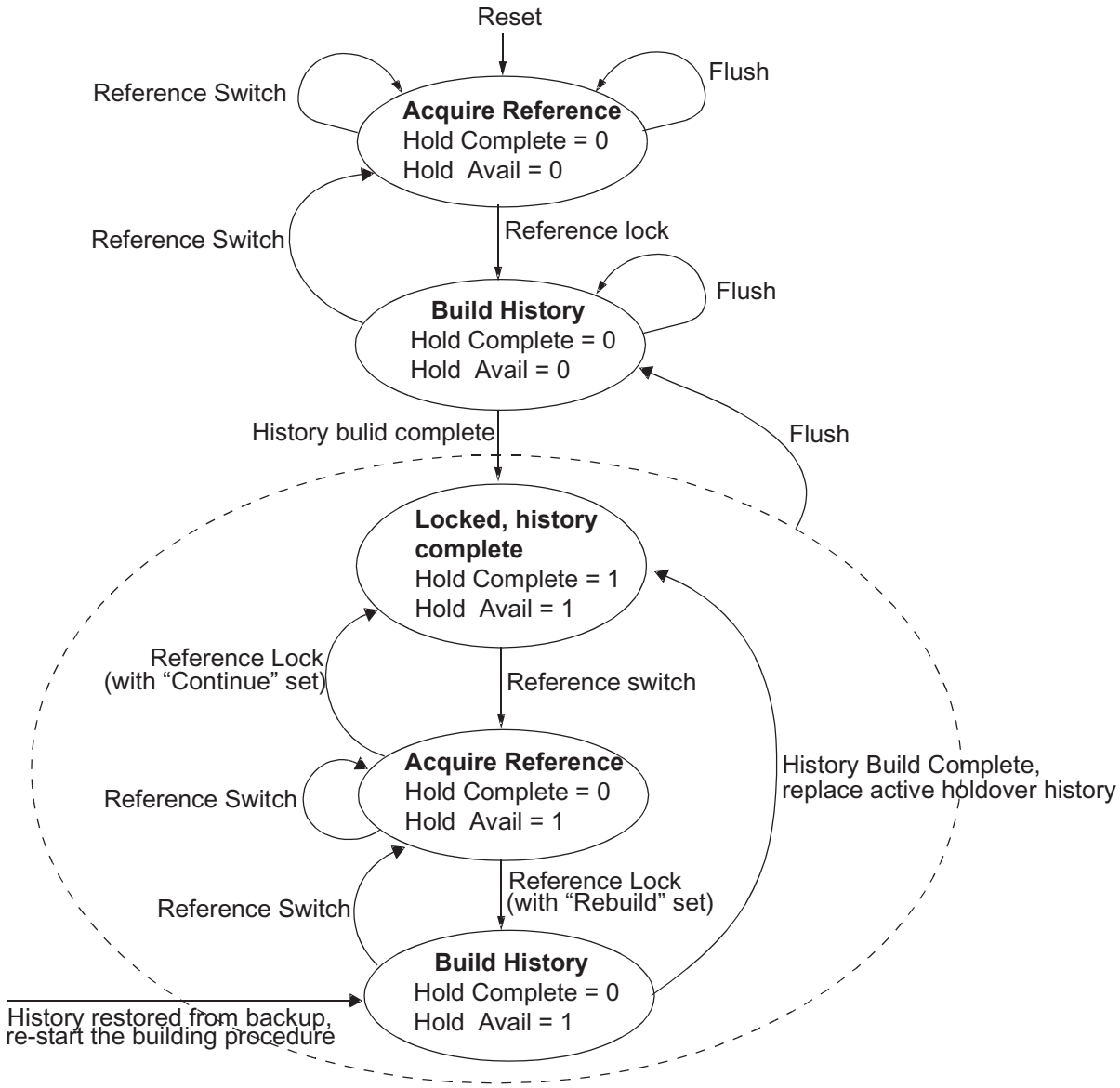
Once lock has been achieved, Hold Over history is compiled in the accumulation register. It is transferred to the Active Hold Over history when it is ready (typically in about 15 minutes). The “Holdover Available” bit and output pin are set to “1”. From then on, the Active Hold Over history is continually updated and kept in sync with the Hold Over history accumulation register. (See Figure 12).

Hold Over History Access and Control Registers

Table 11

0x25	History_Policy	Sets policy for Hold Over history accumulation: “Rebuild” or “Continue”
0x26	History_Cmd	Save, restore, and flush commands for Hold over history
0x27	Hold Over_Time	Indicates the time since entering the Hold Over state
0x11	DPLL_Status	Bits3 and 4: “Hold Over Available” and “Hold Over Build Complete”

Hold Over History and Status States
Figure 12



Hold Over History Accumulation and Maintenance continued

Whenever Hold Over is entered, it is the Active Holdover History that is used to determine the Hold Over frequency. The **History_Cmd** register allows the application to issue three Hold Over history control commands:

1) Save the Active Holdover History to the Backup History.
2) Restore a Backup History to the Active.
3) Flush the active History as well as the accumulation register. The Backup history remains intact.

Both the Active and the Backup Hold Over histories are loaded with the calibrated Free Run synthesizer control data on reset/power-up.

The application might use the “save to backup” in a situation where, for example, the primary reference is known to be of higher quality than any secondary references, in which case it may be desirable to save and then restore the Hold Over history accumulated on the primary reference if the primary reference is lost and Hold Over is entered upon loss of a secondary reference. Users can restore the history from backup any time, even while operating in Holdover mode. The frequency transient will be smooth and continuous. It is the responsibility of application software to keep track of the age and viability of the Hold Over backup history. Given time and temperature effects on oscillator aging, the application may wish to periodically perform a “Save” of the Active history to keep the backup current.

When switching to a new reference, the active Hold Over history will remain intact and marked as “Holdover Available” (if it was available before the reference switch) until a new history is accumulated on the new reference (Typically 15 minutes after lock has been achieved). During the new history accumulation, the “Holdover Build Complete” bit is reset. Once the new history accumulation is complete, it is transferred to the Active History and the “Holdover Build Complete” bit is set. The active history will then continue to be updated to track the reference.

The **History_Policy** register allows the application to control how a new history is built. When set to “Rebuild”:

1) History accumulation begins when lock is achieved on the new reference.
2) The Hold Over history is rebuilt (taking about 15 minutes). The Active History remains untouched until it is replaced when the build is complete.

When the policy is set to “Continue”:

1) If there is no “Available” Active History, a new build occurs, as under the “Rebuild” policy.
2) If there is an “Available” Active History, it will continue, the accumulation register will be loaded from the Active History, and the “Build” process is essentially completed immediately following lock on the new reference.

The “Continue” policy may be used by the application if, for example, it is known that the reference switched to may be traced to the same source and therefore likely has no frequency offset from the prior reference. In that case, the “Continue” policy avoids the delay of rebuilding the Hold Over history. If the switch is likely to be between references with known or unknown frequency offset, then it is preferable to use the “Rebuild” policy.

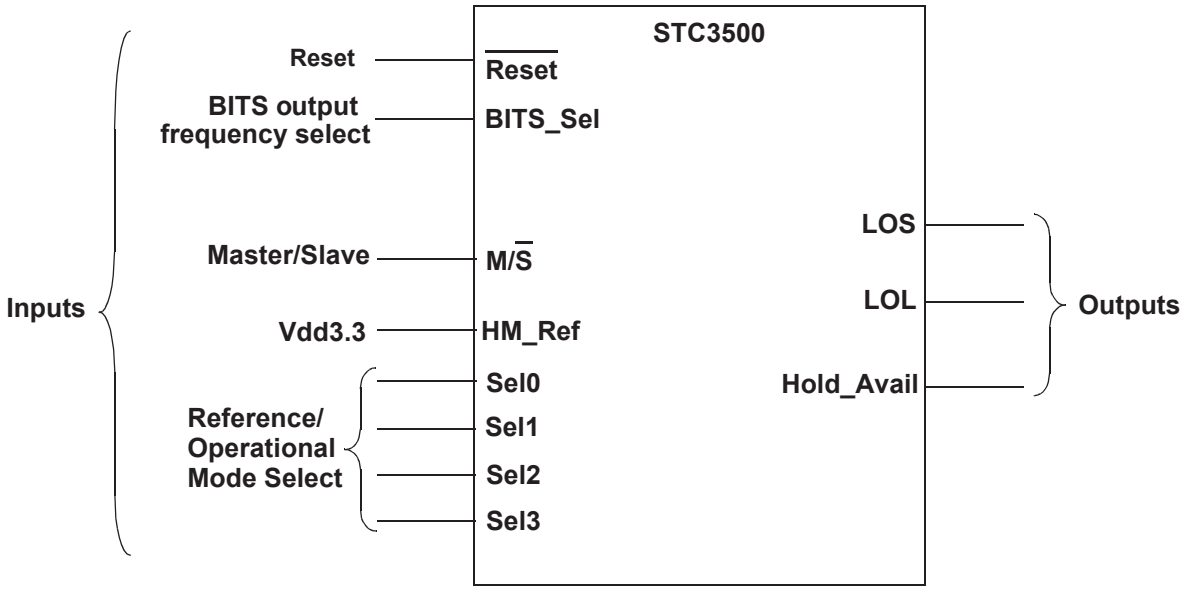
The time since the Hold Over state was entered may be read from the **Hold Over_Time** register. Values are from 0 to 255 hours, limited at 255, and reset to 0 when not in the Hold Over state.

Boundary Scan – The STC3800 provides a standard IEEE 1149.1 JTAG boundary scan interface via the **TMS**, **TCK**, **TDI**, **TDO**, and **TRST** pins. Boundary scan may be used to verify proper device I/O connectivity and functionality.

Control Modes

The STC3500 device may be controlled and interfaced in a pure hardware mode with pin signals, or via SPI or parallel bus/register access. With register access, the device can in turn be operated in a manual control mode, or automatic control and reference selection mode. Hardware mode is most suitable for simple environments where minimal external intelligence is desired. Register access provides more detailed visibility and control for references and general synchronization operation. These three main operating environments are detailed as follows:

Hardware Control Interfaces
Figure 12



Hardware Control – The device interfaces for hardware control are shown in Figure 12.

$\overline{\text{Reset}}$ may be pulled low for a minimum of 100nS during chip start-up (or any other desired time) to initialize the full device state. However, power-up will also perform a reset, so in a minimal configuration, **$\overline{\text{Reset}}$** may be tied input high.

The BITS clock output frequency is selected by the **BITS_Sel** pin. When **BITS_Sel** = 1, the BITS frequency is 1.544 MHz, and when **BITS_Sel = 0**, the BITS frequency is 2.048 MHz.

M/$\overline{\text{S}}$ - Determines the master or slave mode. Set to “1” for a master, and “0” for a slave. Master/slave switches should be performed with minimal delay between switching the states of each of the two devices. This can be easily accomplished, for example, by controlling the master/slave state with a single signal, coupled to one of the devices through an inverter.

For simplex operation, the device should be in Master mode - set **M/$\overline{\text{S}}$** to “1”.

HM_Ref - Set to “1” for hardware control of reference selection and operational mode.

Sel0-3 - Write to the appropriate values for the desired reference selection and operating mode, as shown below:

Hardware Reference Selection and Mode Control

Table 12

Reference / Mode	Pin Sel3	Sel2	Sel1	Sel0
Free Run	0	0	0	0
Lock to Ref1	0	0	0	1
Lock to Ref2	0	0	1	0
Lock to Ref3	0	0	1	1
Lock to Ref4	0	1	0	0
Lock to Ref5	0	1	0	1
Lock to Ref6	0	1	1	0
Lock to Ref7	0	1	1	1
Lock to Ref8	1	0	0	0
Hold Over	1	0	0	1

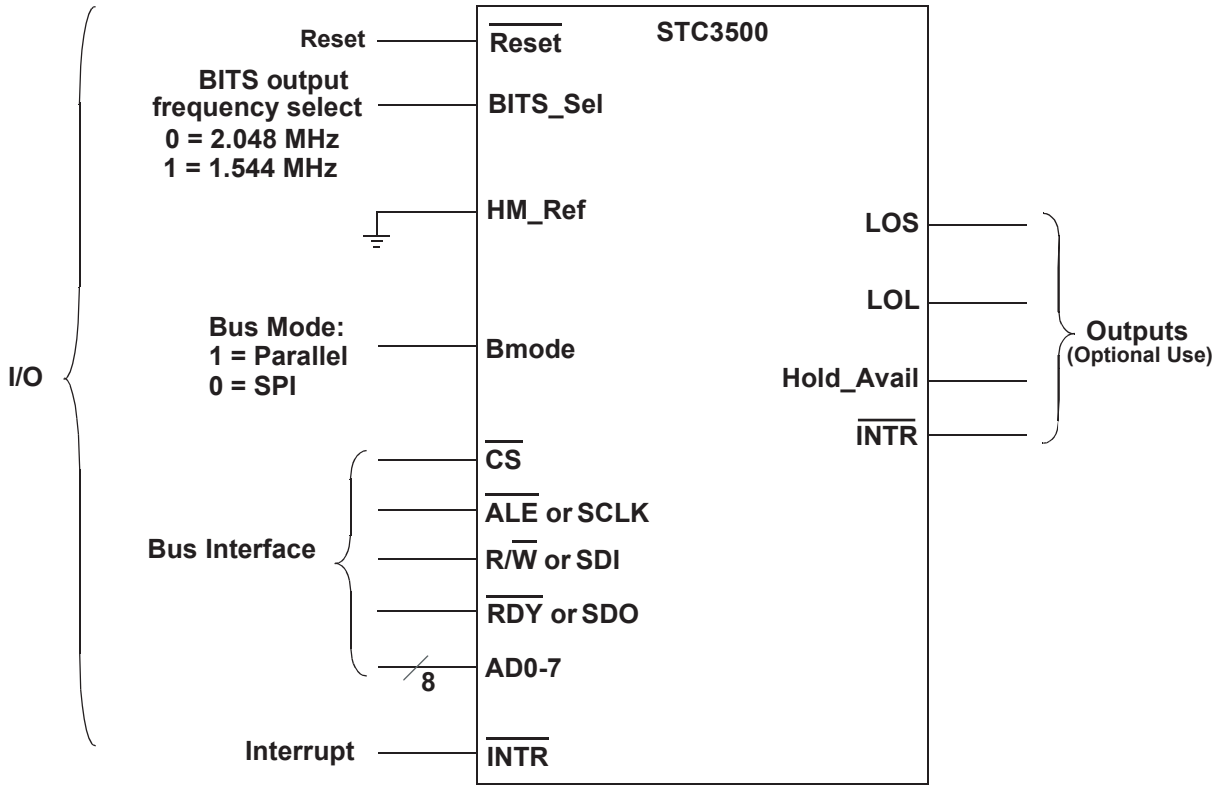
LOS, **LOL**, and **Hold_Avail** are status indication outputs. Their use is at the discretion of the application. See **Operating Modes, Reference Input Quality Mode**, and **Pin Description** sections for details of their operation.

In Hardware Control mode, the **Sync_8K** and **Sync_2K** signals default to 50% duty cycle, and DPLL bandwidth/ phase buildout default to stratum 3.

Register Access Manual Control

In Register Control Mode, far more internal device information is available. However, Operational mode and Reference Selection may still be performed manually. The control configuration for this mode of operation is shown in Figure 13:

Register Access Manual Control Interfaces
Figure 13



In Register Access Manual Control Operation, the hardware control pin, **HM_Ref**, is tied low.

Reset may be pulled low for a minimum of 100nS during chip start-up (or any other desired time) to initialize the full device state.

Following any reset, device configuration data must be pumped, either automatically from the external EEPROM, or by the application through the bus interface (see **Application Notes**, **General**, **Configuration Data** section). Tie **Dmode** "High" for EEPROM pump, and "Low" for register pump.

If the optional EEPROM is equipped, EEPROM data may be read or written via the bus interface. See **Application Notes**, **General**, **Reading and Writing EEPROM** section.

The BITS clock output frequency is selected by the **BITS_Sel** pin. When **BITS_Sel** = 1, the BITS frequency is 1.544 MHz and when **BITS_Sel** = 0, the BITS frequency is 2.048 MHz

Bus access may be either in parallel or SPI mode. **Bmode** is connected "high" for parallel bus and "low" for SPI operation. Parallel bus operation uses **CS**, **ALE**, **R/W**, **RDY**, and **AD0-7**, as described in the Register Control section, Figures 3 and 4, and Table 6. SPI uses **CS**, **SCLK**, **SDI**, and **SDO**, as described in the Register Control section, Figures 5 and 6, and Table 7.

Set the device bandwidth and enable/disable phase build-out by writing the appropriate values to the **Bandwidth_PBO** register, 0x03. (See **Register Descriptions and Operation**). The recommended value is .098 Hz. for Stratum 3.

Select 50% duty cycle or variable pulse width for the **Sync_8K** and **Sync_2K** output by writing the appropriate values to bits 4 and 5 of the **Ctl_Mode** register (0x04), as shown below:

Pulse Width Control	Reg. 0x03 BITS 5-4
Sync_2K and Sync_8K 50% duty cycle	00
Sync_2K 50% duty cycle, Sync_8K variable pulse width	01
Sync_2K variable pulse width, Sync_8K 50% duty cycle	10
Sync_2K and Sync_8K variable pulse width	11

In variable pulse width mode, the desired pulse width is written to register **FR_Pulse_Width** (0x10). The pulse width is the register value (valid range is 1 - 15) multiple of the **Sync_Clk** clock period. The same pulse width is applied to both **Sync_8K** and **Sync_2K**. For example, if **Sync_Clk** is at 19.44 MHz and the desired pulse width is 206nS, write **FR_Pulse_Width** to 0000 0100 (4 x 51.5nS).

The auto-detected input reference frequencies may be read from bits 7-4 of the Ref(1-8)_Frq_Priority registers.

If desired, write the **Freerun_Priority** register (0x24) to enable Free Run to be treated like a reference (See **Register Descriptions and Operation** section). If it is enabled, set the desired priority and revertivity.

Select the desired operational mode and reference by writing the appropriate value to register **Op_Mode** (0x05).

Mode	Reg. 0x03
Free Run	0001 0000
Lock on Ref1	0001 0001
Lock on Ref2	0001 0010
Lock on Ref3	0001 0011
Lock on Ref4	0001 0100
Lock on Ref5	0001 0101
Lock on Ref6	0001 0110
Lock on Ref7	0001 0111
Lock on Ref8	0001 1000
Hold Over	0001 1001

When the device is in slave mode, it will lock to the **Xref** input, independent of the values written to bits 4 - 0 of the **Op_mode** register. The operational mode and reference selection written to bits 4 - 0 while in slave mode will, however, take effect when the device is made the master.

For simplex operation, the device should be in Master mode.

Select the desired Hold Over history policy, “Continue” or “Rebuild”, by writing to the **History_Policy** register, (0x25). The application may further save, restore, or flush the Hold Over history using the **History_Cmd** register (2x26), as described in the **Hold Over History Accumulation and Maintenance** section.

The remainder of the registers provide access to device internals, such as synchronization state, reference activity and quality, and operational customizations. Their use is at the discretion of the application. Some typical uses are described below (see also the **Register Descriptions and Operation** section):

Max_Pullin_Range (0x06) - Set to the maximum allowed frequency offset for a reference.

Ref_Qualified (0x0a) - May be read to determine if a reference is active and within the pull-in range before selecting it as an active reference.

Phase_Offset (0x0e) - May be used to compensate for master/slave **Sync_8K** or **Sync_Clk** to **Xref** pathlength or clock distribution paths, as desired. Requires analytic/experimental technique to determine appropriate values. See also **Master/Slave Operation** sections.

Calibration (0x0f) - This register can be used to compensate for a known OCXO/TCXO frequency offset. Write to a value representing the difference between the oscillator’s measured frequency and the nominal frequency.

DPLL_Status (0x11) - This register provides active reference, lock, and Hold Over history status in support of mode control decisions by the application.

Interrupts - Five interrupts are provided for application monitoring and control of synchronization. They are individually maskeable by the **Intr_Enable** register (0x13), and readable in the **Intr_Event** (0x12) register. Pin **$\overline{\text{INTR}}$** is pulled low when a non-masked interrupt occurs.

Ctl_Mode (0x04) - The state of the **BITS_Sel** and **HM_Ref** pins may be read from bits 2 and 3.

Holdover_Time (2x27) - The time, from 0 to 255 hours, since the Hold Over state was entered, may be read.

While the same information is available via register access, the **LOS**, **LOL**, and **Hold_Avail** status indication outputs are also functional and may be used at the discretion of the application.

Register Access Automatic Control

For Register Access Automatic Control, the interfaces, reset, and bus operations are the same as shown in Figure 12 and described in the **Register Access Manual Control** section. The **Bandwidth_PBO** register write operation is also the same.

The BITS clock output frequency is selected by the **BITS_Sel** pin. When **BITS_Sel** = 1, the BITS frequency is 1.544 MHz and when **BITS_Sel** = 0, the BITS frequency is 2.048 MHz

$\overline{\text{Reset}}$ may be pulled low for a minimum of 100nS during chip start-up (or any other desired time) to initialize the full device state.

Following any reset, device configuration data must be pumped, either automatically from the external EEPROM, or by the application through the bus interface (see **Application Notes**, **General**, **Configuration Data** section). Tie **Dmode** "High" for EEPROM pump, and "Low" for register pump.

If the optional EEPROM is equipped, EEPROM data may be read or written via the bus interface. See **Application Notes**, **General**, **Reading and Writing EEPROM** section.

Select automatic active reference selection by writing bit 1 of the register **Ctl_Mode** (0x04) to 0. The auto-detected input reference frequencies may be read from bits 7-4 of the **Ref(1-8)_Frq_Priority** registers. With automatic reference selection, the device (In master mode) also performs operational mode selection (Locked, Hold Over, and Free Run) automatically, as shown in Figure 8.

Individual references may be enabled or disable for use by writing the appropriate values to the **Ref_Mask** (0x0b) register.

Select 50% duty cycle or variable pulse width for the **Sync_8K** and **Sync_2K** output by writing the appropriate values to bits 4 and 5 of the **Ctl_Mode** register (0x04), as shown below:

Pulse Width Control	Reg. 0x03 BITS 5-4
Sync_2K and Sync_8K 50% duty cycle	00
Sync_2K 50% duty cycle, Sync_8K variable pulse width	01
Sync_2K variable pulse width, Sync_8K 50% duty cycle	10
Sync_2K and Sync_8K variable pulse width	11

In variable pulse width mode, the desired pulse width is written to register **FR_Pulse_Width** (0x10). The pulse width is the register value multiple (valid range is 1 - 15) of the **Sync_Clk** clock period. The same pulse width is applied to both **Sync_8K** and **Sync_2K**. For example, if **Sync_Clk** is at 19.44 MHz and the desired pulse width is 206nS, write **FR_Pulse_Width** to 0000 0100
(4 x 51.5nS).

Max_Pullin_Range register (0x06) - Set to the maximum allowed frequency offset for a reference.

Automatic reference selection is accompanied by per-reference selectable priorities. These are written to bits 2-0 of the **Ref(1-8)_Frq_Priority** registers. The highest priority is 0 and the lowest is 7. For equal priorities, lower reference numbers have higher priority. Active reference selection is then made according to priority and conditioned on reference availability (registered in **Ref_Available**). See figure 7.

Each reference may also be marked as “revertive” or “non-revertive”, by writing bit 3 of the **Ref(1-8)_Frq_Priority** registers to “1” for revertive or “0” for non-revertive.

When a reference becomes unavailable, the device automatically picks the available reference of next lower priority. When a reference returns, it will be switched to only if it is of higher priority and the current active reference is marked “Revertive”. Return to a previously failed reference is delayed by the value in the **Ref_Rev_Delay** register. Write a value from 0 to 255 minutes to the **Ref_Rev_Delay** register for the desired delay. (See figure 7 in the **Reference Input Selection, Frequencies, and Mode Selection** section).

If operating in a master/slave configuration, be sure to write the **Ref_Mask** and the **Ref(1-8)_Frq_Priority** registers to the same values for both devices. Read the operational mode (lower 4 bits) from the master’s **Op_Mode** register, and write them to the lower 4 bits of the slave’s **Op_Mode** (0x05) register. This needs to be repeated whenever there is a reference switch on the master. To facilitate this, an interrupt (bit 4 of the **Intr_Event** register) is provided to indicate a reference change. (Alternatively, the application may choose to poll the master’s **Op_Mode** register to detect reference switches.)

Select the desired Hold Over history policy, “Continue” or “Rebuild”, by writing to the **History_Policy** register, (0x25). The application may further save, restore, or flush the Hold Over history using the **History_Cmd** register (2x26), as described in the **Hold Over History Accumulation and Maintenance** section.

The remainder of the registers provide access to device internals, such as synchronization state, reference activity and quality, and operational customizations. Their use is at the discretion of the application. Some typical uses are described below (see also the **Register Descriptions and Operation** section):

Phase_Offset (0x0e) - May be used to compensate for master/slave **Sync_8K** or **Sync_Clk** to **Xref** path-length or clock distribution paths, as desired. Requires analytic/experimental technique to determine appropriate values. See also **Master/Slave Operation** sections.

Calibration (0x0f) - This register can be used to compensate for a known OCXO/TCXO frequency offset. Write to a value representing the difference between the oscillator’s measured frequency and the nominal frequency.

DPLL_Status (0x11) - This register provides active reference, lock, and Hold Over history status.

Interrupts - Five interrupts are provided for application monitoring and control of synchronization. They are individually maskeable by the **Intr_Enable** register (0x13), and readable in the **Intr_Event** (0x12) register. Pin **INTR** is pulled low when a non-masked interrupt occurs.

Ref_Qualified (0x0a) - May be read to determine if a reference is active and within the pull-in range.

Ref_Available (0x0c) - May be read to determine if a reference is qualified and not masked.

Ref(1-8)_Frq_Offset (0x13 -0x1a) - May be read to determine the frequency offset, in 0.2 ppm resolution, between each reference and the local calibrated oscillator.

Ctl_Mode (0x04) - The state of the **BITS_Sel** and **HM_Ref** pins may be read from bits 2 and 3.

While the same information is available via register access, the **LOS**, **LOL**, and **Hold_Avail** status indication outputs are also functional and may be used at the discretion of the application.

Ref(1-8)_Frq_Offset (0x13 -0x1a) - May be read to determine the frequency offset, in 0.2 ppm resolution, between each reference and the local calibrated oscillator.

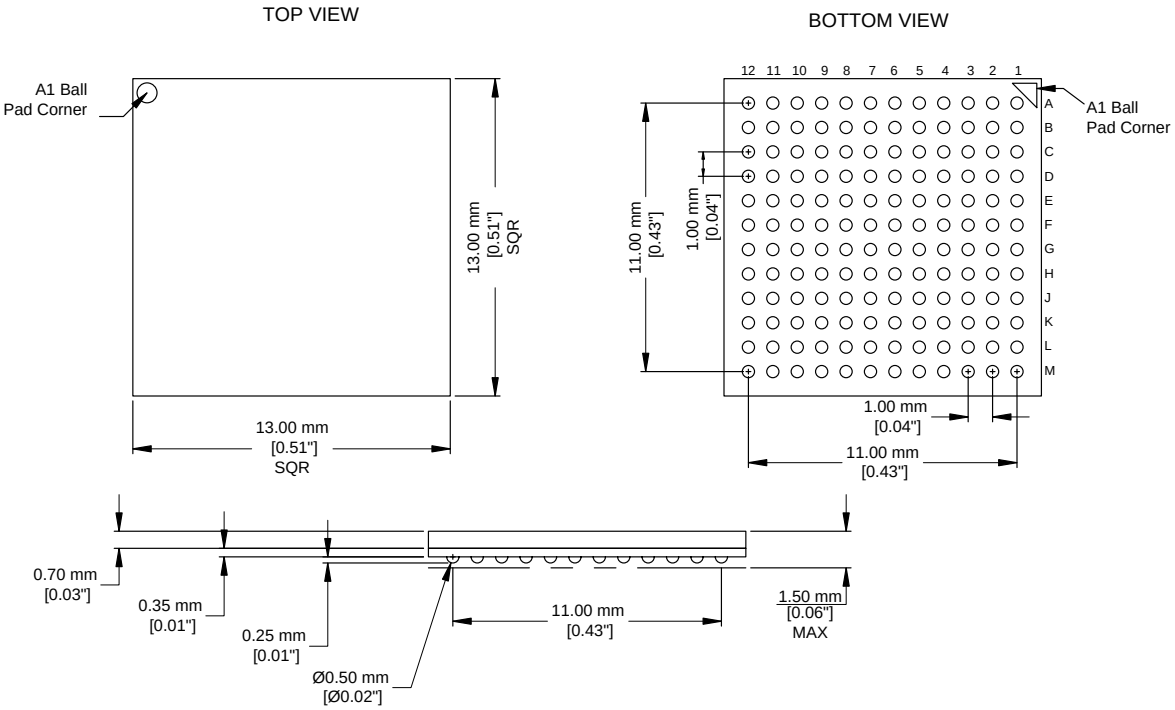
Ctl_Mode (0x04) - The state of the **BITS_Sel** and **HM_Ref** pins may be read from bits 2 and 3.

Holdover_Time (2x27) - The time, from 0 to 255 hours, since the Hold Over state was entered, may be read.

Mechanical Specifications

Package Dimensions

Figure 14



All dimensions are ±10%
unless otherwise indicated

Additional External Components

1. Place series resistors (33 ohms) on all reference inputs.
2. Place series resistors (33 ohms) on SPI_IN and SPI_CLK inputs.
3. Place one .01uF at the input power pins.
4. One 4.7uF (25V) capacitor is required at the VPP pin.
5. One 4.7uF (25V) capacitor is required at the VPN pin.

PCB Layout Recommendations

1. Place .01 nF caps close to Vcc pins.
2. Place de-coupling and/or filter components as close to module pins as possible.
3. Ensure that only clean and well-regulated power is supplied to the module.
4. Isolate power and ground inputs to the module from noisy sources.
5. Must provide a separate power and ground trace to the oscillator that provides sufficient power to the oscillator.
6. Keep module signals away from sensitive or noisy analog and digital circuitry.
7. Avoid split ground planes as high-frequency return currents may be affected.
8. Allow extra spacing between traces of high-frequency inputs and outputs.
9. Keep all traces as short as possible - avoid meandering trace paths.
10. It is recommended that the connections of the JTAG, VPP and VPN pins be routed to pads, preferably in a SIL pattern as shown in Figure 15 below. It is recommended to use 0.1” center to center spacing.

JTAG/ISP Header Connections

Figure 15

CONNOR WINFIELD

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Revision	Revision Date	Note
A02	07/01/03	Advance Release
P02	01/21/04	Miscellaneous Spec Revisions
P03	02/05/04	Features GR-253-CORE, 10^{-6} to 1 ppb, Pkg Dim
P04	02/19/04	External Components, PCB Layout Rec, JTAG/ISP
P05	11/15/04	EEPROM Access Architecture
P06	11/22/04	Chip Revision Update