SM8230A

Tone Dialer with Built-in Piezo Driver

OVERVIEW

The SM8230A is a dual-tone signal generator LSI developed for DTMF (dual tone multi-frequency) dialing. It features a built-in piezo-electric speaker driver for direct connection to a piezo-electric buzzer. The DTMF frequencies can be set to correspond to the DTMF standards of any country. The output level is also adjustable under software control. These features, combined with its small package and low power dissipation, make the SM8230A a very use device to use.

FEATURES

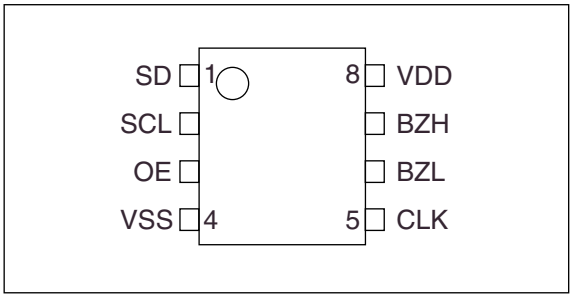
- 3-line serial interface to external CPU
- 2 independent, adjustable frequency outputs
- Piezo driver for direct connection to a piezo-electric buzzer
- 4 system clock frequencies selectable (480kHz, 960kHz, 1.92MHz, 3.84MHz)
- 2.6 to 3.3V supply voltage
- Low current consumption
  - 3.0mA (max) operating current
  - 1µA (max) standby current
- Package: 8-pin plastic SOP

ORDERING INFORMATION

Device	Package
SM8230AS	8-pin SOP

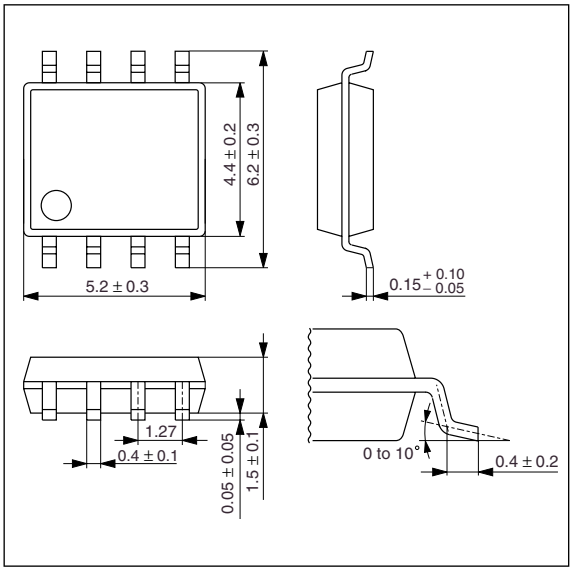
PINOUT

(Top view)

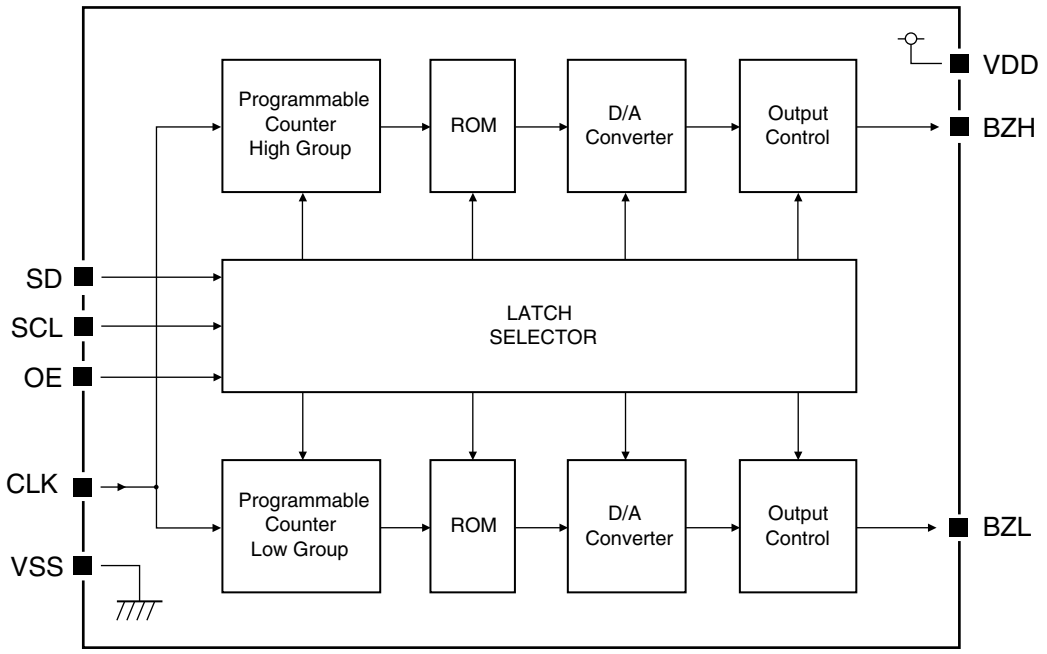


PACKAGE DIMENSIONS

(Unit: mm)



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O	Description
1	SD	I	Serial data input
2	SCL	I	Serial data transfer clock input. (For valid transfer, OE must stay LOW for 16 clock cycles.)
3	OE	I	DTMF output enable/serial data transfer select input. Serial data transfer is selected when LOW.
4	VSS	–	Ground
5	CLK	I	System clock input. The clock can be set to one of four frequencies (480kHz, 960kHz, 1.92MHz, 3.84MHz).
6	BZL	O	DTMF low-frequency group analog output
7	BZH	O	DTMF high-frequency group analog output
8	VDD	–	Supply voltage

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	–0.3 to 7.0	V
Input voltage range	V_{IN}	V_{SS} – 0.3 to V_{DD} + 0.3	V
Output voltage range	V_{OUT}	V_{SS} – 0.3 to V_{DD} + 0.3	V
Storage temperature range	T_{stg}	–55 to 125	°C
Power dissipation	P_D	250	mW

Recommended Operating Conditions

V_{SS} = 0V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltage range	V_{DD}		2.6	3.0	3.3	V
Operating temperature	T_{opr}		–20	25	70	°C

DC Characteristics

V_{DD} = 2.6 to 3.3V, V_{SS} = 0V, Ta = –20 to 70°C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Operating current consumption	I_{DD}	V_{DD} = 3.0V, Ta = 25°C, f_{CLK} = 480kHz	–	1.5	3	mA
Standby current consumption	I_{ST}	V_{DD} = 3.3V, OE = LOW	–	–	1	µA
Input voltage (all inputs)	V_{IH}	HIGH-level input	1.1	–	V_{DD}	V
	V_{IL}	LOW-level input	V_{SS}	–	0.6	
Input leakage current	I_{IL}	HIGH/LOW-level input	–1	–	1	µA
BZH/BZL tone output voltage	V_{BZO}	0dB output level	0.86V_{DD}	0.93V_{DD}	1.0V_{DD}	Vp-p
BZH/BZL tone output adjustment step	D_{RES}		–	1.0	–	dB
BZH/BZL tone output absolute error	D_{LIN}	V_{ZBO} levels	–1	–	1	dB
BZH/BZL tone output impedance	Z_{OUT}		100	150	200	Ω

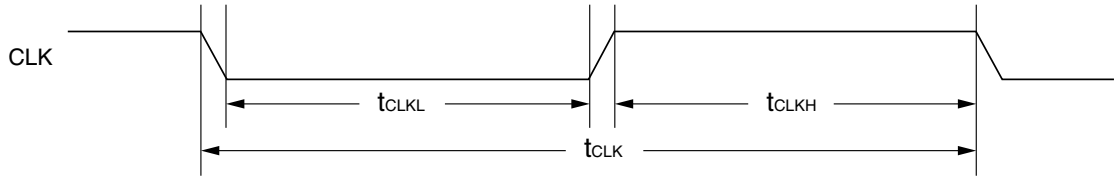
AC Characteristics

V_{DD} = 2.6 to 3.3V, V_{SS} = 0V, Ta = –20 to 70°C

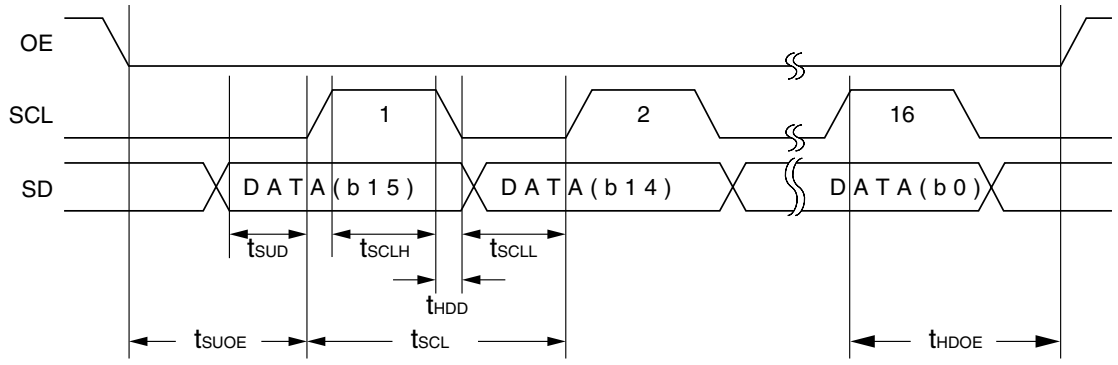
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Tone output frequency error	Δf	f_{CLK} = 3.84MHz, no deviation	–	–	0.37	%
Tone distortion[1]	DIS	BZH/BZL	–	5	10	%
CLK cycle time	t_{CLK}	CLK input waveform	250	–	–	ns
CLK LOW-level pulsewidth	t_{CLKL}		100	–	–	ns
CLK HIGH-level pulsewidth	t_{CLKH}		100	–	–	ns
OE setup time	t_{SUOE}	Between OE and SCL	100	–	–	ns
OE hold time	t_{HDOE}		100	–	–	ns
SCL cycle time	t_{SCL}	SCL input waveform	1	–	–	µs
SCL LOW-level pulsewidth	t_{SCLL}		400	–	–	ns
SCL HIGH-level pulsewidth	t_{SCLH}		400	–	–	ns
Input data setup time	t_{SUD}	Between SD and SCL	100	–	–	ns
Input data hold time	t_{HDD}		100	–	–	ns

1. Ta = –10 to 70°C, THD + N (10Hz to 500kHz), no load

System clock input timing



Serial data transfer timing



FUNCTIONAL DESCRIPTION

Serial Interface

Data is transferred in 16-bit units by writing commands over a 3-line serial interface comprising OE (output enable), SCL (serial clock) and SD (serial data input). Note that data transfer is unidirectional; no data is output from the SM8230A. The operating sequence is described below.

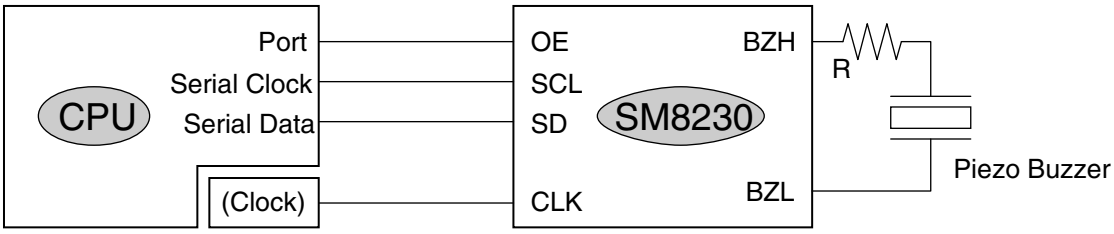


Figure 1. Serial interface connection example

Command transfer

Data can be transferred when OE goes LOW. Data is transferred in 16-bit units in sync with the rising edge of the SCL clock.

Note that when OE is LOW and both SD and SCL are tied LOW, the current consumption is less than 1µA (standby mode).

The internal states are undefined when power is first applied.

DTMF analog signal output

Data transfer stops and DTMF analog signal output starts when OE goes HIGH, as shown in figure 2.

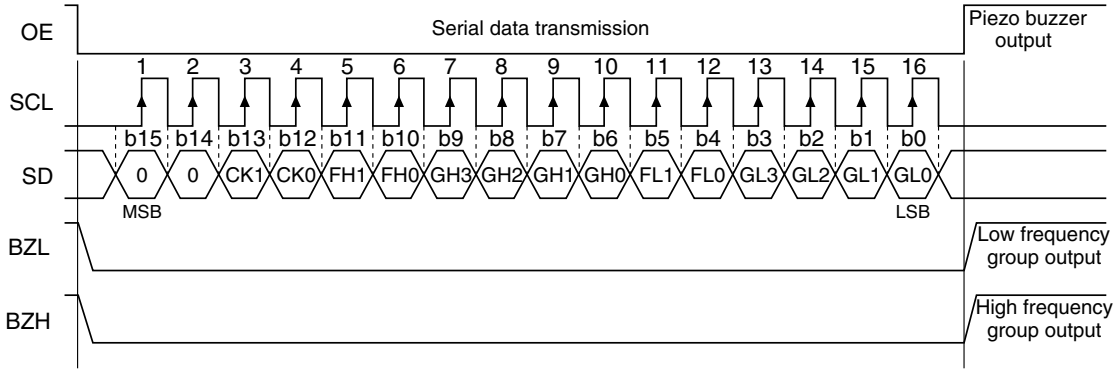


Figure 2. Serial data transfer timing

Transfer Command Specifications

The transfer data code format is shown in figure 3. Data is transferred with the MSB as the leading bit. The data sets the input clock, high-frequency group and low-frequency group frequencies, and the output levels. The commands are shown in tables 1 to 4.

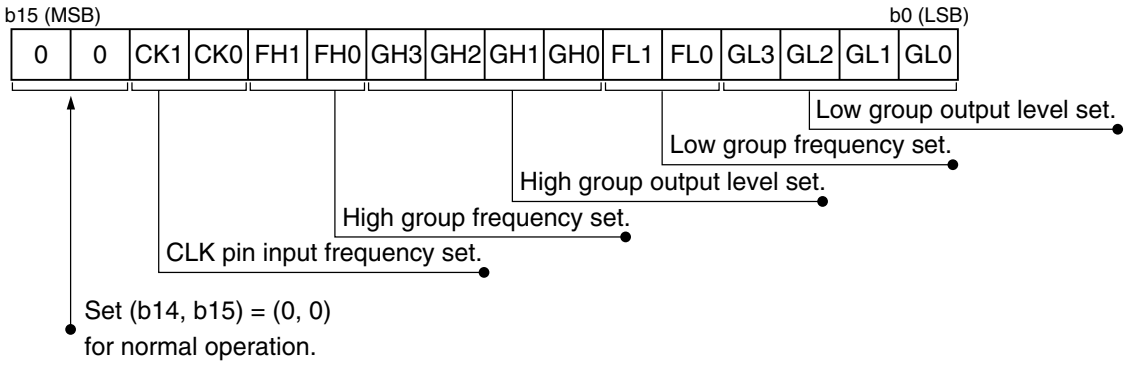


Figure 3. Transfer command format

CK command (CK1, CK0)

These bits set the frequency of the input clock on CLK. The frequency can be set to 1×, 2×, 4×, and 8× multiples of 480kHz. The input code and the corresponding clock frequency are shown in table 1.

Table 1. CK command

CK1	CK0	CLK input clock frequency
0	0	480kHz
0	1	960kHz
1	0	1.92MHz
1	1	3.84MHz

FH/FL command (HF1, FH0/FL1, FL0)

These bits set the DTMF signal high-frequency and low-frequency group frequencies, respectively.The input code, the corresponding group frequency specification, the design value and frequency deviation are shown in tables 2 and 3. Note that the design value and frequency deviation are calculated values assuming a deviation-free system clock input on CLK.

Table 2. FH command

FH1	FH0	DTMF frequency [Hz]	Design value [Hz]	Deviation [%]
0	0	1209	1212.1	+0.26
0	1	1336	1333.3	–0.20
1	0	1477	1481.5	+0.30
1	1	1633	1632.7	–0.02

Table 3. FL command

FH1	FH0	DTMF frequency [Hz]	Design value [Hz]	Deviation [%]
0	0	697	697.7	+0.10
0	1	770	769.2	–0.10
1	0	852	851.1	–0.11
1	1	941	937.5	–0.37

GH/GL command (GH3 to GH0, GL3 to GL0)

These bits set the output levels of the high-frequency group and low-frequency group outputs, respectively. The input code and the corresponding output level are shown in table 4. Note that the 0dB point is typically 93% of the supply voltage. Any value above 0dB results in amplitude clipping of the output waveform.

Table 4. GH/GL command

GH3/GL3	GH2/GL2	GH1/GL1	GH0/GL0	Output level
0	0	0	0	–9dB
0	0	0	1	–8dB
0	0	1	0	–7dB
0	0	1	1	–6dB
0	1	0	0	–5dB
0	1	0	1	–4dB
0	1	1	0	–3dB
0	1	1	1	–2dB
1	0	0	0	–1dB
1	0	0	1	0dB
1	0	1	0	1dB
1	0	1	1	2dB
1	1	0	0	3dB
1	1	0	1	4dB
1	1	1	0	5dB
1	1	1	1	6dB

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