

# M62393P/FP

## 8-bit 8ch I<sup>2</sup>C BUS D/A Converter with Buffer Amplifiers

REJ03D0884-0300

Rev.3.00

Mar 25, 2008

### Description

The M62393P/FP is an integrated circuit semiconductor of CMOS structure with 8 channels of built-in D/A converters with output buffer operational amplifiers. The input is 2-wires serial method is used for the transfer format of digital data to allow connection with a microcomputer with minimum wiring.

The output buffer operational amplifier employs AB class output circuit with sink and source drive capacity of 1.0 mA or more, and it operates in the whole voltage range from VrefU to ground. And because of connects maximum 8 pieces to 64 channels control.

### Features

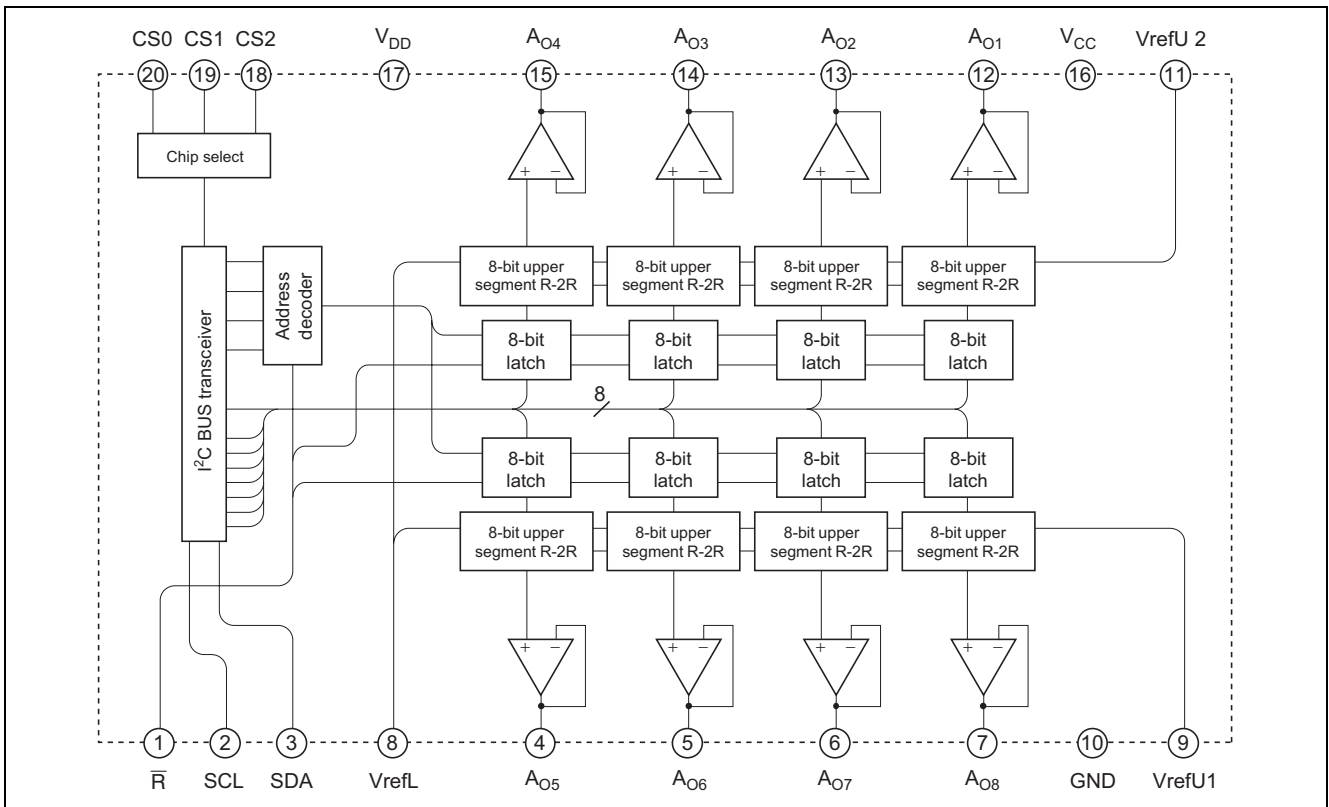
- Digital data transfer format: I<sup>2</sup>C BUS serial data method
- Output buffer operational amplifier  
It operates in the whole voltage range from VrefU (0 to 5 V) to ground.
- High output current drive capacity: ±1.0 mA over
- Preparation two high level reference voltage terminal because there are two high level reference voltage terminal, it can set up two kinds differ voltage range.

### Application

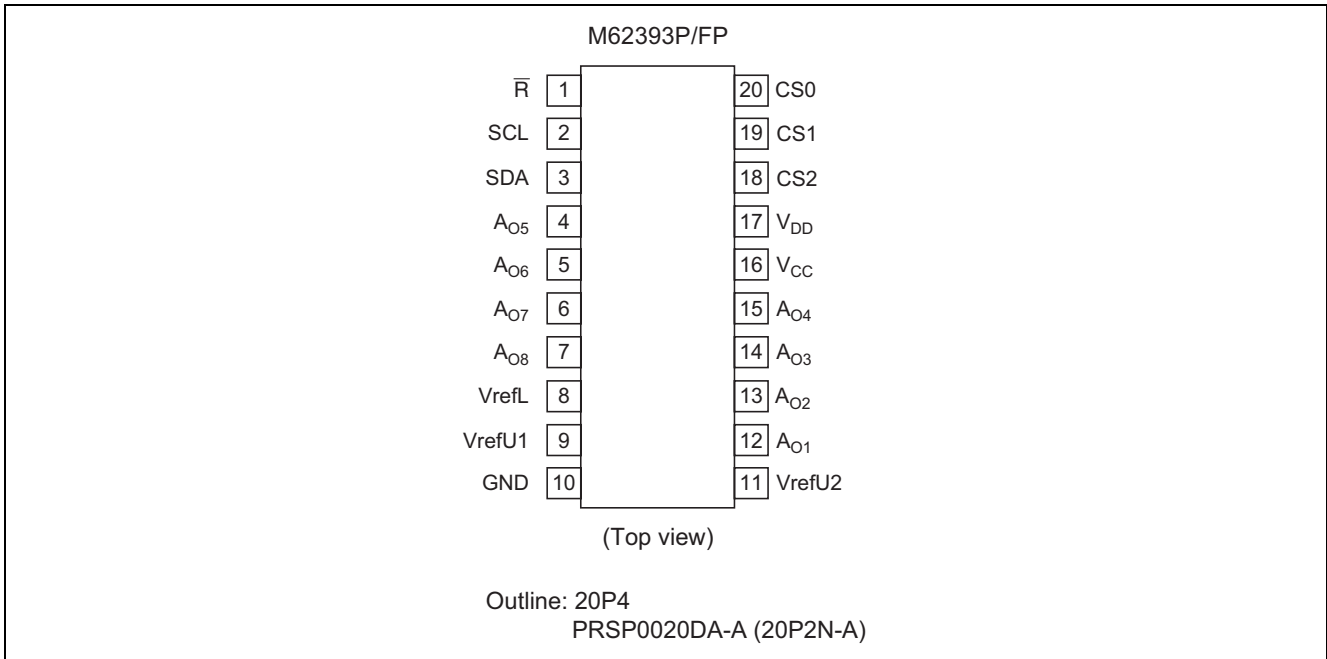
Conversion from digital control data to analog control data for home-use and industrial equipment.

Signal gain control or automatic adjustment of display-monitor or CTV.

### Block Diagram



## Pin Arrangement



## Pin Description

Pin No.	Pin Name	Function
3	SDA	Serial data input terminal
1	R	Reset signal input terminal
2	SCL	Serial clock input terminal
12	Ao1	8-bit D/A converter output terminal
13	Ao2	
14	Ao3	
15	Ao4	
4	Ao5	
5	Ao6	
6	Ao7	
7	Ao8	
16	V <sub>CC</sub>	Analog power supply terminal
17	V <sub>DD</sub>	Digital power supply terminal
10	GND	Analog and digital common GND
8	VrefL	D/A converter low level reference voltage input terminal
9	VrefU1	D/A converter high level reference voltage input terminal 1
11	VrefU2	D/A converter high level reference voltage input terminal 2
18	CS2	Chip select data input terminal 2
19	CS1	Chip select data input terminal 1
20	CS0	Chip select data input terminal 0

## Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	$V_{CC}$	-0.3 to +7.0	V
Supply voltage	$V_{DD}$	-0.3 to +7.0	V
D/A converter high level reference voltage	$V_{refU1, 2}$	-0.3 to +7.0	V
Input voltage	$V_{IN}$	-0.3 to $V_{DD} + 0.3$	V
Output voltage	$V_O$	-0.3 to $V_{DD} + 0.3$	V
Power dissipation	$P_d$	990 (P) / 590 (FP)	mW
Operating temperature	$T_{opr}$	-20 to +85	°C
Storage temperature	$T_{stg}$	-40 to +125	°C

## Electrical Characteristics

### <Digital Part>

( $V_{CC}$ ,  $V_{DD}$ ,  $V_{refU1, 2} = +5\text{ V} \pm 10\%$ ,  $V_{CC} \geq V_{refU1, 2}$ ,  $GND = V_{refL} = 0\text{ V}$ ,  $T_a = -20\text{ to }+85^\circ\text{C}$ , unless otherwise noted.)

Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Supply voltage	$V_{DD}$	4.5	5.0	5.5	V	
Supply current	$I_{DD}$	—	—	1.0	mA	CLK = 1 MHz operation, $I_{AO} = 0\ \mu\text{A}$
Output low voltage (SDA)	$V_{OL}$	—	—	0.4	V	$I_{sink} = 3\text{ mA}$
Input leak current	$I_{ILK}$	-10	—	10	$\mu\text{A}$	$V_{IN} = 0\text{ to }V_{CC}$
Input low voltage	$V_{IL}$	—	—	$0.2 V_{CC}$	V	
Input high voltage	$V_{IH}$	$0.8 V_{CC}$	—	—	V	

### <Analog Part>

( $V_{CC}$ ,  $V_{DD}$ ,  $V_{refU1, 2} = +5\text{ V} \pm 10\%$ ,  $V_{CC} \geq V_{refU1, 2}$ ,  $GND = V_{refL} = 0\text{ V}$ ,  $T_a = -20\text{ to }+85^\circ\text{C}$ , unless otherwise noted.)

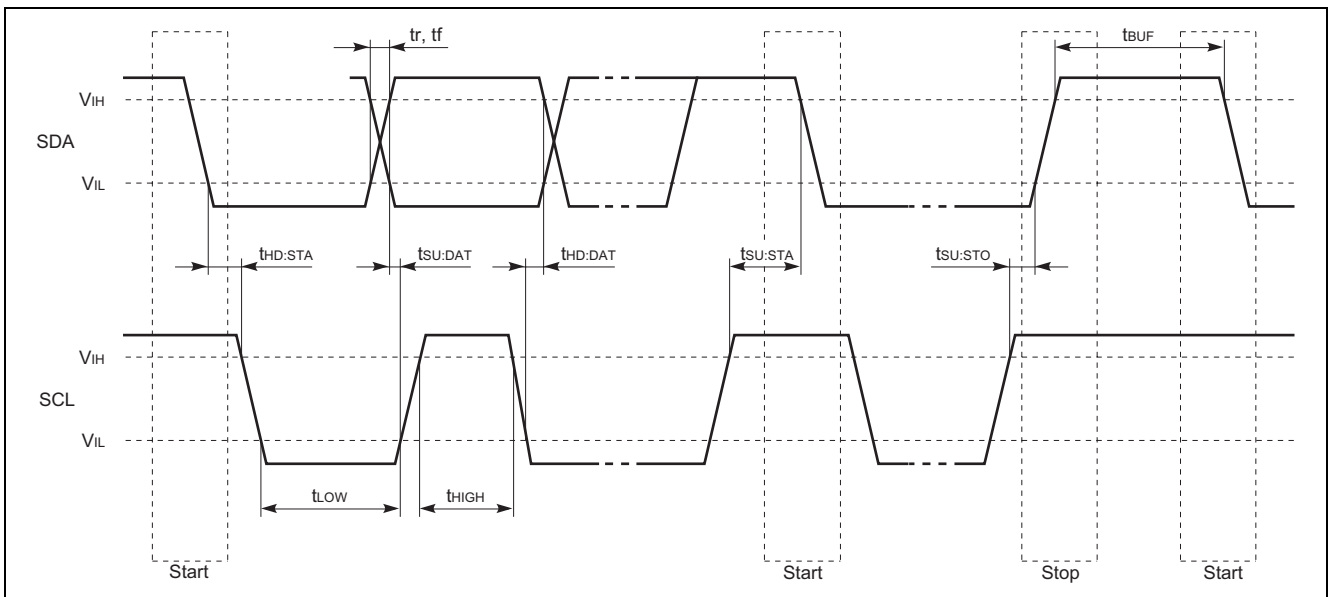
Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V	
Supply current	$I_{CC}$	—	1.6	3.2	mA	CLK = 1 MHz operation, $I_{AO} = 0\ \mu\text{A}$
D/A converter high level reference voltage input current	$I_{refU}$	—	1.0	2.0	mA	$V_{refU} = 5\text{ V}$ , $V_{refL} = 0\text{ V}$ Data condition: at maximum current
D/A converter high level reference voltage range	$V_{refU}$	3.5	—	$V_{CC}$	V	The output dose not necessarily be the values within the reference voltage setting range.
D/A converter low level reference voltage range	$V_{refL}$	GND	—	$V_{CC} - 3.5$	V	
Buffer amplifier output voltage range	$V_{AO}$	0.1	—	$V_{CC} - 0.1$	V	$I_{AO} = \pm 100\ \mu\text{A}$
		0.2	—	$V_{CC} - 0.2$	V	$I_{AO} = \pm 500\ \mu\text{A}$
Buffer amplifier output current range	$I_{AO}$	-1.0	—	1.0	mA	Upper side saturation voltage = 0.3 V Lower side saturation voltage = 0.2 V
Differential nonlinearity	$S_{DL}$	-1.0	—	1.0	LSB	$V_{refU} = 4.79\text{ V}$
Nonlinearity	$S_L$	-1.5	—	1.5	LSB	$V_{refL} = 0.95\text{ V}$
Zero code error	$S_{ZERO}$	-2.0	—	2.0	LSB	$V_{CC} = 5.5\text{ V}$ (15 mV/LSB)
Full scale error	$S_{FULL}$	-2.0	—	2.0	LSB	Without load ( $I_{AO} = 0$ )
Output capacitive load	$C_O$	—	—	0.1	$\mu\text{F}$	
Buffer amplifier output impedance	$R_O$	—	5.0	—	$\Omega$	

I<sup>2</sup>C BUS Line Characteristics

Item	Symbol	Normal Mode		High Speed Mode		Unit
		Min	Max	Min	Max	
SCL clock frequency	$f_{SCL}$	0	100	0	400	kHz
Time the bus must be free before a new transmission can start	$t_{BUF}$	4.7	—	1.3	—	$\mu$ s
Hold time start condition. After this period. The first clock pulse is generated.	$t_{HD:STA}$	4.0	—	0.6	—	$\mu$ s
Low period of the clock	$t_{LOW}$	4.7	—	1.3	—	$\mu$ s
High period of the clock	$t_{HIGH}$	4.0	—	0.6	—	$\mu$ s
Setup time for start condition (only relevant for a repeated start condition)	$t_{SU:STA}$	4.7	—	4.7	—	$\mu$ s
Hold time data	$t_{HD:DAT}$	0	—	0	0.9	$\mu$ s
Setup time data	$t_{SU:DAT}$	250	—	100	—	ns
Rise time of both SDA and SCL lines	$t_R$	—	1000	20	300	ns
Fall time of both SDA and SCL lines	$t_F$	—	300	20	300	ns
Setup time for stop condition	$t_{SU:STO}$	4.0	—	0.6	—	$\mu$ s

Note: Transmitter must internally at reset a hold time to bridge the undefined region (300 ns Max) of the falling edge of SCL.

## Timing Chart

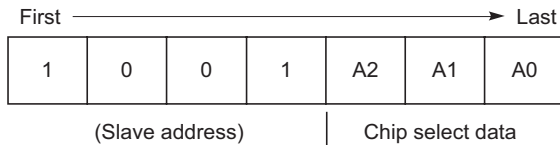


## I<sup>2</sup>C BUS Format

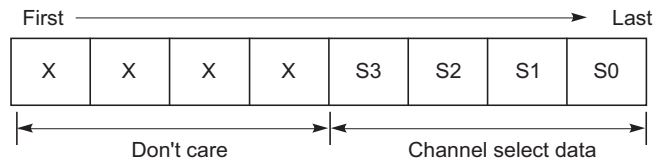
STA	Slave address	W	A	Sub address	A	DAC data	A	STP
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### Digital Data Format

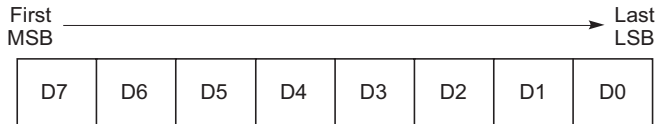
- Slave Address



- Sub Address



- DAC Data



#### (1) Chip Select Data

MSB	LSB				
A2	A1	A0	CS2	CS1	CS0
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
:	:	:	:	:	:
1	1	1	1	1	1

#### (2) Channel Select Data

MSB	LSB				Channel Selection
S3	S2	S1	S0		
0	0	0	0	Don't care	
0	0	0	1	ch1 selection	
0	0	1	0	ch2 selection	
:	:	:	:	:	
0	1	1	1	ch7 selection	
1	0	0	0	ch8 selection	
1	0	0	1	Don't care	
:	:	:	:	:	
1	1	1	1	Don't care	

#### (3) DAC Data

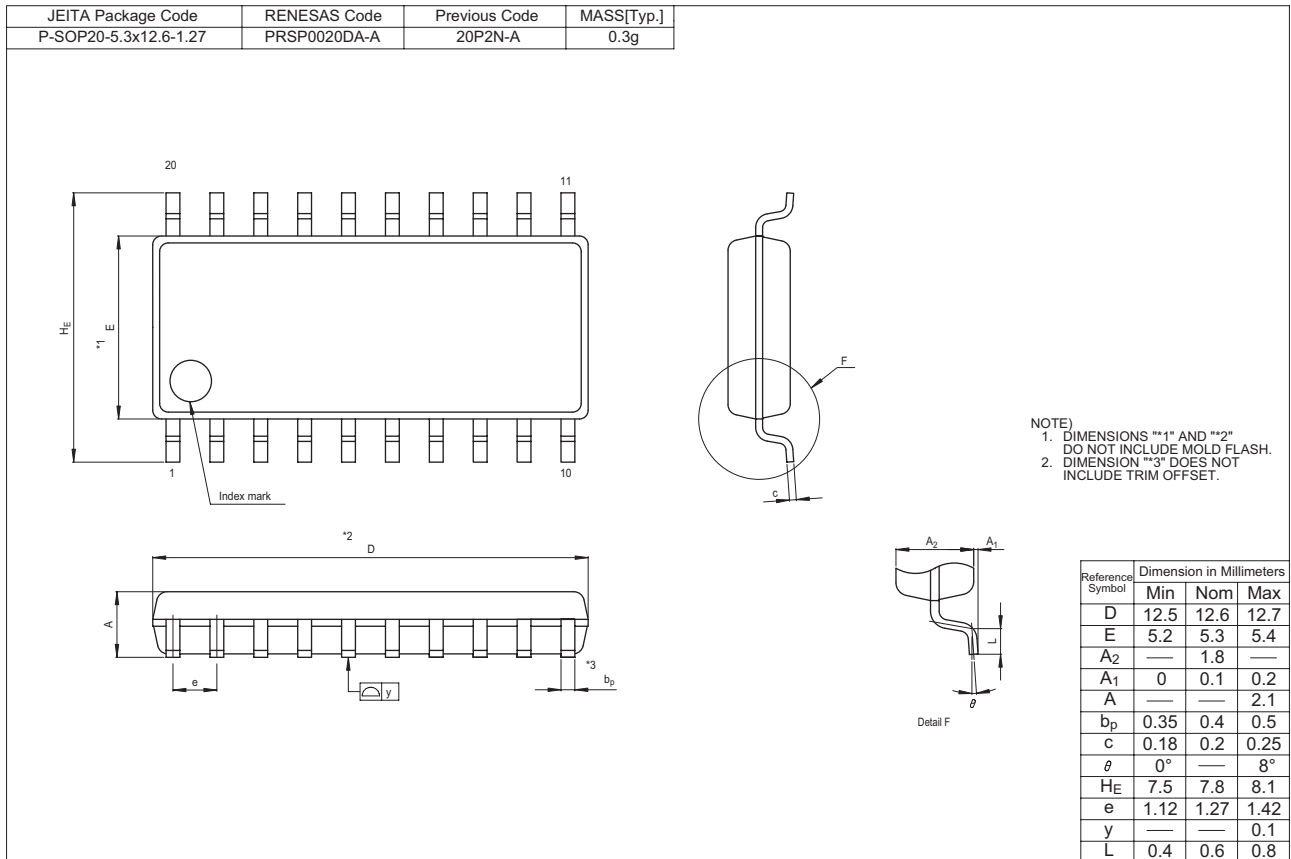
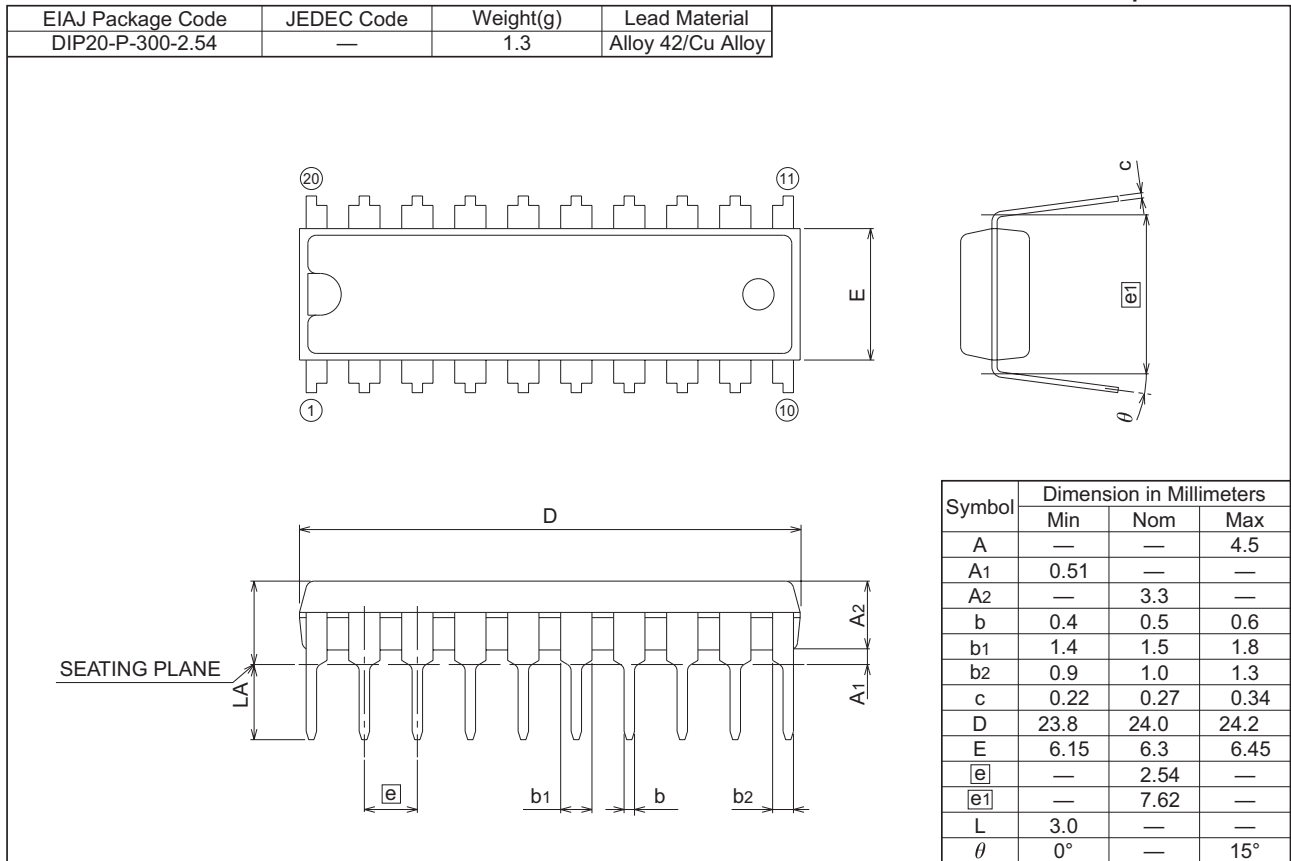
First MSB → Last LSB

D7	D6	D5	D4	D3	D2	D1	D0	DAC Output
0	0	0	0	0	0	0	0	$(V_{refU} - V_{refL}) / 256 \times 1 + V_{refL}$
0	0	0	0	0	0	0	1	$(V_{refU} - V_{refL}) / 256 \times 2 + V_{refL}$
0	0	0	0	0	0	1	0	$(V_{refU} - V_{refL}) / 256 \times 3 + V_{refL}$
0	0	0	0	0	0	1	1	$(V_{refU} - V_{refL}) / 256 \times 4 + V_{refL}$
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	0	$(V_{refU} - V_{refL}) / 256 \times 255 + V_{refL}$
1	1	1	1	1	1	1	1	$V_{refU}$

Package Dimensions

20P4

Plastic 20pin 300mil DIP



Notes:

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