

60V Complementary PowerTrench MOSFET

KDS8333C

■ Features

- N-Channel

4.1 A, 30 V $R_{DS(ON)} = 80\text{m}\Omega$ @ $V_{GS} = 10\text{ V}$
 $R_{DS(ON)} = 130\text{m}\Omega$ @ $V_{GS} = 4.5\text{V}$

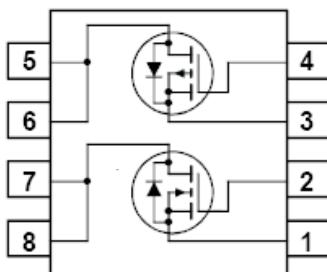
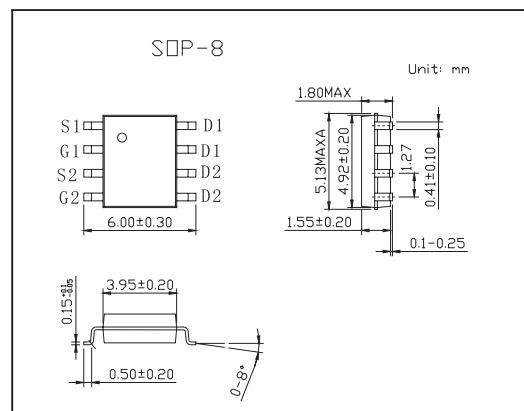
- P-Channel

-3.4 A, 30 V $R_{DS(ON)} = 130\text{ m}\Omega$ @ $V_{GS} = -10\text{ V}$
 $R_{DS(ON)} = 200\text{ m}\Omega$ @ $V_{GS} = -4.5\text{V}$

- Low gate charge

- High performance trench technology for extremely low $R_{DS(ON)}$.

- High power and handling capability in a widely used surface mount package.



■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	N-Channel	P- Channel	Unit
Drain to Source Voltage	V_{DSS}	30	-60	V
Gate to Source Voltage	V_{GS}	± 16	± 20	V
Drain Current Continuous (Note 1a)	I_D	4.1	-3.4	A
Drain Current Pulsed		20	-20	A
Power Dissipation for Single Operation	P_D	2		W
Power Dissipation for Single Operation (Note 1a)	P_D	1.6		W
(Note 1b)		1		
(Note 1c)		0.9		
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150		°C
Thermal Resistance Junction to Ambient (Note 1a)	$R_{\theta JA}$	78		°C/W
Thermal Resistance Junction to Case (Note 1)	$R_{\theta JC}$	40		°C/W

KDS8333C■ Electrical Characteristics $T_a = 25^\circ\text{C}$

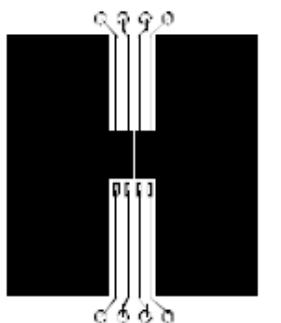
Parameter	Symbol	Testconditons		Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	Bv_{DSS}	$V_{GS} = 0 \text{ V}, ID = 250 \mu\text{A}$	N-Ch P-Ch	30			V
		$V_{GS} = 0 \text{ V}, ID = -250 \mu\text{A}$		-30			
Breakdown Voltage Temperature Coefficient	$\frac{\Delta Bv_{DSS}}{\Delta T_J}$	$ID = 250 \mu\text{A}, \text{Referenced to } 25^\circ\text{C}$	N-Ch P-Ch		25		$\text{mV/}^\circ\text{C}$
		$ID = -250 \mu\text{A}, \text{Referenced to } 25^\circ\text{C}$			-22		
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24\text{V}, V_{GS} = 0 \text{ V}$	N-Ch P-Ch			1	μA
		$V_{DS} = -24 \text{ V}, V_{GS} = 0 \text{ V}$				-1	
Gate-Body Leakage	I_{GSS}	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0 \text{ V}$	N-Ch P-Ch			± 100	nA
		$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$				± 100	
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, ID = 250 \mu\text{A}$	N-Ch P-Ch	1	1.7	3	V
		$V_{DS} = V_{GS}, ID = -250 \mu\text{A}$		-1	-1.8	-3	
Gate Threshold Voltage Temperature Coefficient	$\frac{\Delta V_{GS(\text{th})}}{\Delta T_J}$	$ID = 250 \mu\text{A}, \text{Referenced to } 25^\circ\text{C}$	N-Ch P-Ch		-4.2		$\text{mV/}^\circ\text{C}$
		$ID = -250 \mu\text{A}, \text{Referenced to } 25^\circ\text{C}$			3.7		
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}, ID = 4.1\text{A}$	N-Ch		67	80	$\text{m}\Omega$
		$V_{GS} = 10 \text{ V}, ID = 4.1 \text{ A}, T_J = 125^\circ\text{C}$			81	130	
		$V_{GS} = 4.5 \text{ V}, ID = 3.2 \text{ A}$			103	145	
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -10 \text{ V}, ID = -3.4\text{A}$	P-Ch		105	130	
		$V_{GS} = -10 \text{ V}, ID = -3.4 \text{ A}, T_J = 125^\circ\text{C}$			167	200	
		$V_{GS} = -4.5 \text{ V}, ID = -2.5\text{A}$			147	220	
On-State Drain Current	$I_{D(on)}$	$V_{GS} = 10 \text{ V}, V_{DS} = 5\text{V}$	N-Ch P-Ch	10			A
		$V_{GS} = -10 \text{ V}, V_{DS} = -5\text{V}$		-5			
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{V}, ID = 4.1\text{A}$	N-Ch P-Ch		9		S
		$V_{DS} = -5\text{V}, ID = -3.4\text{A}$			5		
Input Capacitance	C_{iss}	N-Channel $V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1.0 \text{ MHz}$	N-Ch P-Ch		282		pF
					185		
Output Capacitance	C_{oss}	P-Channel $V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1.0 \text{ MHz}$	N-Ch P-Ch		49		pF
					56		
Reverse Transfer Capacitance	C_{rss}	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1.0 \text{ MHz}$	N-Ch P-Ch		20		pF
					26		
Gate Resistance	R_G	$V_{GS} = 15 \text{ mV}, f = 1.0 \text{ MHz}$ $V_{GS} = -15 \text{ mV}, f = 1.0 \text{ MHz}$	N-Ch P-Ch		2.3		Ω
					-9.6		
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 10 \text{ V}, ID = 1 \text{ A},$ $V_{GS} = 4.5 \text{ V}, R_{GEN} = 6 \Omega \text{ (Note 2)}$	N-Ch P-Ch		4.5	9	ns
					4.5	9	
Turn-On Rise Time	tr		N-Ch P-Ch		6	12	ns
					13	23	
Turn-Off Delay Time	$t_{d(off)}$	P-Channel $V_{DD} = -10 \text{ V}, ID = -1 \text{ A},$ $V_{GS} = -4.5 \text{ V}, R_{GEN} = 6 \Omega \text{ (Note 2)}$	N-Ch P-Ch		19	34	ns
					11	20	
Turn-Off Fall Time	tf		N-Ch P-Ch		1.5	3	ns
					2	4	
Total Gate Charge	Q_g	N-Channel $V_{DS} = 10\text{V}, ID=4.1\text{A}, V_{GS}=4.5\text{V}$	N-Ch P-Ch		4.7	6.6	nC
					4.1	5.7	
Gate-Source Charge	Q_{gs}	R _{GEN} = 6 Ω (Note 2) P-Channel	N-Ch P-Ch		0.9		nC
					0.8		
Gate-Drain Charge	Q_{gd}	$V_{DS}=-10\text{V}, ID=-3.4\text{A}, V_{GS}=-4.5\text{V}$ (Note 2)	N-Ch P-Ch		0.6		nC
					0.4		

KDS8333C■ Electrical Characteristics $T_a = 25^\circ\text{C}$

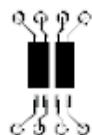
Parameter	Symbol	Testconditons	Min	Typ	Max	Unit
Drain-Source Diode Forward Voltage	V _{SD}	V _{GS} = 0 V, I _S = 1.3A (Not 2)	N-Ch	0.8	1.2	V
		V _{GS} = 0 V, I _S = -1.3A (Not 2)	P-Ch	0.8	-1.2	
Diode Reverse Recovery Time	t _{rr}	I _F = 4.1 A, dI _F /dt = 100 A/ μs	N-Ch	16.3		nS
		I _F = -3.4 A, dI _F /dt = 100 A/ μs	P-Ch	14.5		
Diode Reverse Recovery Charge	Q _{rr}	I _F = 4.1 A, dI _F /dt = 100 A/ μs	N-Ch	26.7		nC
		I _F = -3.4 A, dI _F /dt = 100 A/ μs	P-Ch	21.1		

Notes:

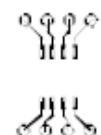
1. R_{SJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{SJC} is guaranteed by design while R_{SCA} is determined by the user's board design.



a) 78°C/W when mounted on a 0.5in² pad of 2 oz copper



b) 125°C/W when mounted on a 0.02 in² pad of 2 oz copper



c) 135°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%