E7765
1.3 GHz Quad Pin Electronics Driver

Description

The E7765 four channel, monolithic ATE pin electronics solutions manufactured in a high-performance complementary bipolar process.

The E7765 power consumption can be minimized to accommodate the required performance and levels. The E7765 has bias and other inputs that provide a means to adjust performance versus power consumption. The E7765 operates at data rates up to 1.3 GHz/2.6 Gbps.

The power supplies to the E7765 are specified over a wide range to accommodate between –2V, +7V and –0.5V, +4.2V output voltage ranges.

The E7765 driver is capable of generating 8V swings over a –2 to +7V range. The driver minimum swing is 100 mV. A differential driver mode configures pairs of adjacent drivers on-chip to drive differential signals from a single data input. The driver pairs are DOUT[0]:DOUT[1] and DOUT[2]:DOUT[3]. The on-chip distribution of the driving signal and the close matching of performance on-chip will result in very low skew for differential output to output.

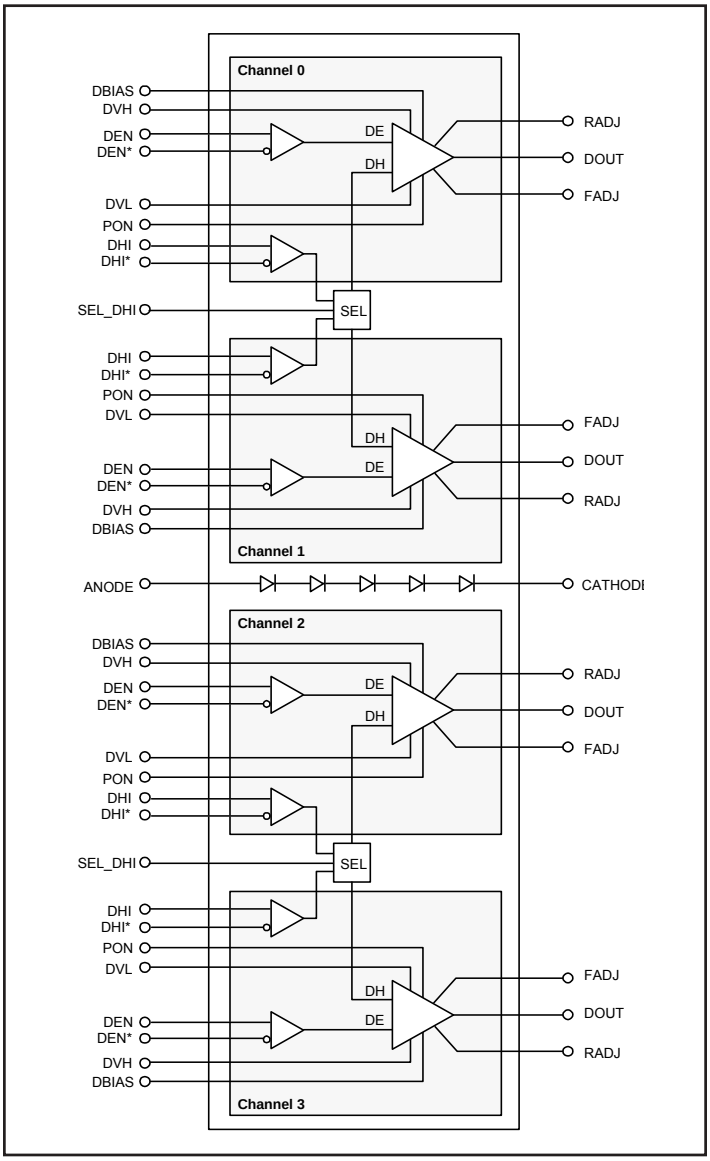
Applications

- Memory Testers
  - Companion Chip to E7725 as Drive-Only Channels
- Programmable Clock Drivers
- Test Instruments

Features

- Four Fully Integrated, Three-Statable Drivers
- Wide Choice of Range, Performance vs. Power
- Differential Driver Mode
- Programmable Driver Rise, Fall Times
- –2V, +7V Driver Voltage Range
- Small, 80-Pin LQFP Package

Functional Block Diagram



PIN Description

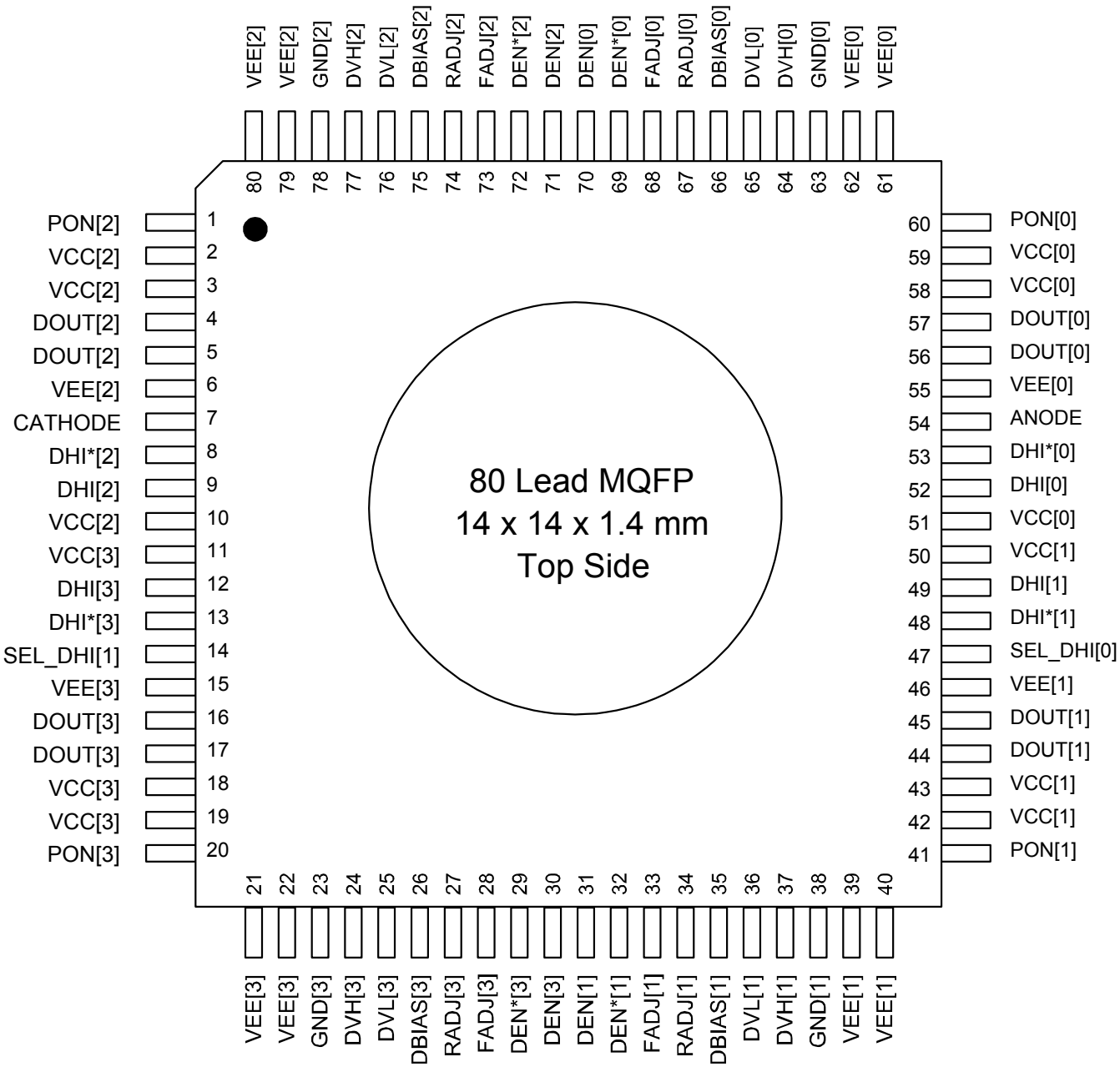
[0:3] Refers to Channels 0, 1, 2 or 3

Pin #	Pin Name	Description
Driver		
56, 57; 44, 45; 4, 5; 16, 17	DOUT[0:3]	Driver output.
52, 49, 9, 12 53, 48, 8, 13	DHI[0:3] DHI*[0:3]	"Flex" differential input digital pins which select the driver high or low level.
70, 31, 71, 30 69, 32, 72, 29	DEN[0:3] DEN*[0:3]	"Flex" differential input pins which control the driver output being active or in a high impedance state.
64, 37, 77, 24 65, 36, 76, 25	DVH[0:3] DVL[0:3]	High impedance analog voltage inputs which determine the driver high and low levels.
67, 34, 74, 27 68, 33, 73, 28	RADJ[0:3] FADJ[0:3]	Input currents which determine the driver output signal rise and fall times.
66, 35, 75, 26	DBIAS[0:3]	Analog current input that sets an internal bias current for the driver and its overall performance by adjusting the overall power.
Control		
47, 14	SEL_DHI[0:1]	TTL inputs that select the Differential Drive mode when a logical high. SEL_DHI[0] will enable DOUT[0] and DOUT[1] to differential mode. SEL_DHI[1] enables DOUT[2] and DOUT[3] to differential mode.
60, 41, 1, 20	PON[0:3]	TTL input that powers the driver ON and OFF. Logical 1 will power ON.
Power Supplies		
59, 58, 51; 50 43, 42; 2, 3, 10; 11, 18, 19	VCC[0:3]	Positive power supply to each of the four driver channels (Note 1).
62, 61, 55; 46, 40, 39; 79, 80, 6; 15, 21, 22	VEE[0:3]	Negative power supply to each of the four driver channels (Note 1).
63, 38, 78, 23	GND[0:3]	Device ground to each of the four driver channels (Note 1).
Miscellaneous		
7, 54	CATHODE, ANODE	Terminals of the on-chip thermal diode string.

Note 1: All VEEs must be connected, externally, to the same supply.
All VCCs must be connected, externally, to the same supply.
All GNDs must be connected, externally.

PIN Description *(continued)*

80 Lead LQFP Package
14 x 14 x 1.4mm



Circuit Description

Introduction

Figure 1 shows a detailed block diagram of the E7765.

Each of the four drivers has independent signal control and voltage inputs. In addition, each driver has independent power-down ability as well as adjustability for output rising and falling edge speeds.

Refer to Table 1 for a truth table depicting the different modes of operation of an individual channel. Table 2 expands on the independent operations with a description of the differential drive mode operation. Differential pair[0] consists of drive channels 0 and 1 and are controlled by SEL_DHI[0]. Differential pair[1] consists of drive channels 2 and 3 and are controlled by SEL_DHI[1].

Channel 0 Control			Output	Comments
DHI[0]	DEN[0]	PON[0]	DOUT[0]	
X	X	0	Off	Low Power, HiZ State
X	0	1	HiZ	Driver Disabled (HiZ)
0	1	1	DVL	Driver Enabled, Follow DHI
1	1	1	DVH	

Channels 1, 2 and 3 similar. SEL_DHI[0] and [1] at logical low.

Table 1. Driver Control Truth Table

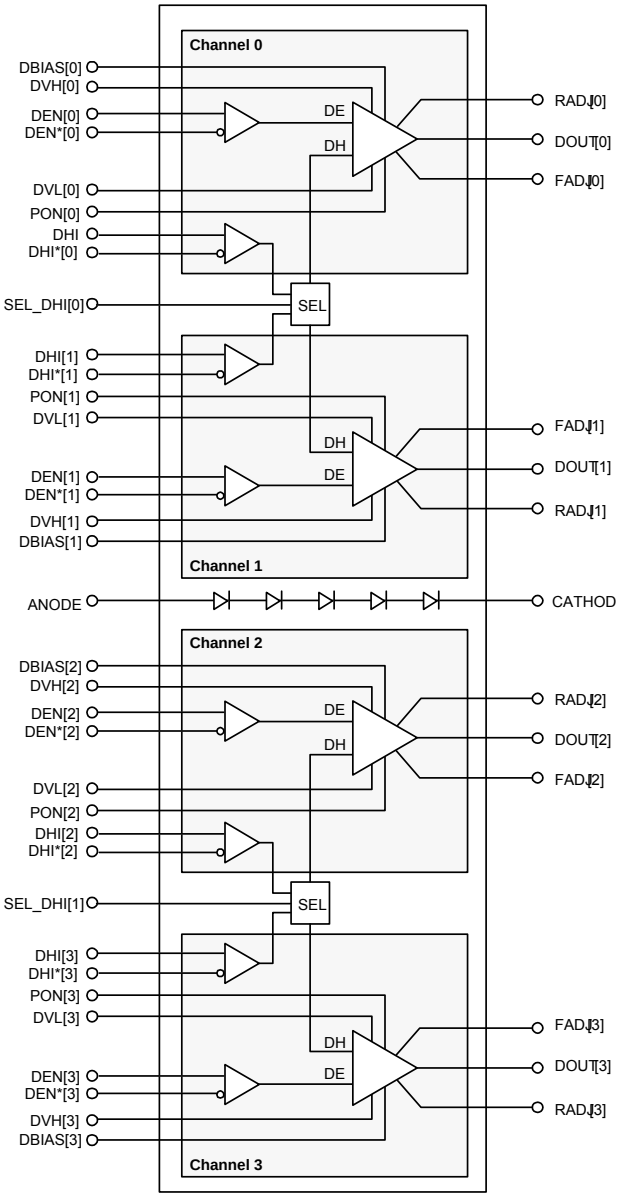


Figure 1. E7765 Detailed Block Diagram

Circuit Description *(continued)*

Diff Mode	*Channel 0 Control*			*Output*	*Channel 1 Control*			*Output*	*Comments*
SEL_DHI[0]	DHI[0]	DEN[0]	PON[0]	DOUT[0]	DHI[1]	DEN[1]	PON[1]	DOUT[1]	
0	SEL_DHI[0]=0, Channel 0 and Channel 1 are independently controlled (see Table 1)								
1	X	X	0	Off	X	0	1	HiZ	Differential mode, PON and DEN are independent per channel.
1	0	X	0	Off	X	1	1	DVH[1]	
1	1	X	0	Off	X	1	1	DVL[1]	
1	0	0	1	HiZ	X	X	0	Off	
1	0	1	1	DVL[0]	X	1	1	DVH[1]	Differential mode, both channels enabled.
1	1	1	1	DVH[0]	X	1	1	DVL[1]	
1	0	1	1	DVL[0]	X	0	1	HiZ	Differential mode, DOUT[0] logically follows DHI[0]
1	1	1	1	DVH[0]	X	0	1	HiZ	
1	0	0	1	HiZ	X	1	1	DVH[1]	Differential mode, DOUT[1] logically follows the complement of DHI[0]
1	1	0	1	HiZ	X	1	1	DVL[1]	

DHI[1] has no effect in differential mode since the Channel 1 output will follow the complemented state of DHI[0].

Diff Mode	*Channel 2 Control*			*Output*	*Channel 3 Control*			*Output*	*Comments*
SEL_DHI[1]	*DHI[2]*	*DEN[2]*	*PON[2]*	*DOUT[2]*	*DHI[3]*	*DEN[3]*	*PON[3]*	*DOUT[3]*	
0	SEL_DHI[1]=0, Channel 2 and Channel 3 are independently controlled (see Table 1)								
1	X	X	0	Off	X	0	1	HiZ	Differential mode, PON and DEN are independent per channel.
1	0	X	0	Off	X	1	1	DVH[3]	
1	1	X	0	Off	X	1	1	DVL[3]	
1	0	0	1	HiZ	X	X	0	Off	
1	0	1	1	DVL[2]	X	1	1	DVH[3]	Differential mode, both channels enabled.
1	1	1	1	DVH[2]	X	1	1	DVL[3]	
1	0	1	1	DVL[2]	X	0	1	HiZ	Differential mode, DOUT[2] logically follows DHI[2]
1	1	1	1	DVH[2]	X	0	1	HiZ	
1	0	0	1	HiZ	X	1	1	DVH[3]	Differential mode, DOUT[3] logically follows the complement of DHI[2]
1	1	0	1	HiZ	X	1	1	DVL[3]	

DHI[3] has no effect in differential mode since the Channel 3 output will follow the complemented state of DHI[2].

Table 2. Differential Mode Control – Driver State Truth Tables

Circuit Description *(continued)*

Driver

The driver digital control inputs DHI/DHI* and DEN/DEN* are "Flex Inputs" – wide voltage differential inputs capable of receiving ECL, TTL, CMOS, or custom level signals. Single-ended operation is supported by connecting the non-driven, differential input to the appropriate DC threshold level. Differential input drive is recommended for highest performance.

Drive Enable

The drive enable inputs (DEN / DEN*) control whether the driver is forcing a voltage, or is placed in a high-impedance state. If DEN is more positive than DEN*, the output will force either DVH or DVL. If DEN is more negative than DEN*, the output goes into a high impedance state. The DEN/DEN* inputs are independent per drive channel and remain effective in the differential mode.

Do NOT leave DEN / DEN* floating.

Driver Data

When the driver is enabled (Table 1) the drive data inputs (DHI / DHI*) determine whether the driver output is forcing a high or a low. If DHI is more positive than DHI*, the driver will force DVH when the driver is active. If DHI is more negative than DHI*, the driver will force DVL when active. The DHI/DHI* inputs are independent per drive channel, but these input signals for drive channels 1 and 3 are not effective when differential mode is enabled.

Do NOT leave DHI / DHI* floating.

Driver Differential Mode Selection

The TTL input SEL_DHI will place a pair of drive channels into a differential drive mode. Channels 0 and 1 are a differential pair that is independent from the channel 2 and 3 differential pair.

SEL_DHI[0]	DH[0] from:	DH[1] from:
0	DHI/DHI*[0]	DHI/DHI*[1]
1	DHI/DHI*[0]	DHI*/DHI[0]

SEL_DHI[0] = 1 is used for outputting a differential signal where DOUT[1] is the inverse of DOUT[0] with the minimum of skew, and both drivers respond to the DHI/DHI*[0] signal. More detail is shown in Table 2. Notice that power-on (PON) and drive enable (DEN) controls are all still in effect for individual drivers. SEL_DHI[1] likewise controls the second pair, channels 2 and 3.

Driver Levels

DVH and DVL are high input impedance voltage inputs which establish the driver's high and low output levels.

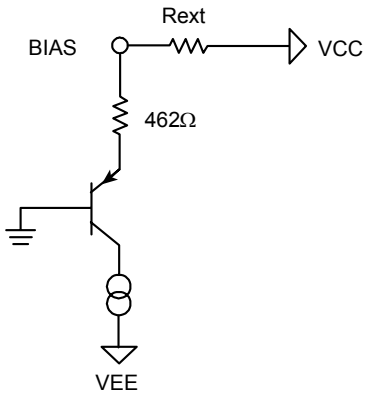
Driver Bias

The DBIAS pin is an analog current input which establishes an on-chip bias current, from which other currents are generated. This current, to some degree, also establishes the overall power consumption and performance of the drivers. Each driver is given its own DBIAS control to allow for varying performance among the four drivers.

Ideally, an adjustable external current source would be used to minimize any part-to-part performance variation within a test system. However, a precision external resistor tied to a large positive voltage is typically acceptable. (See figure below.) The optimal DBIAS current is a function of the RADJ and FADJ settings, and cannot be set independently.

The established bias current follows the equation:

$$DBIAS = (VCC - 0.7) / (Rext + 462\Omega).$$



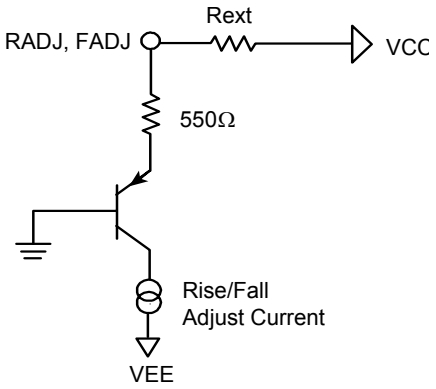
Circuit Description *(continued)*

Driver Slew Rate Adjustment

The driver rising and falling transition times are independently adjustable. The RADJ and FADJ pins are analog current inputs which establish the driver rise and fall times.

Ideally, an adjustable external current source would be used for RADJ and FADJ. However, for applications where the rise and fall times are fixed, precision external resistors to a positive voltage can be used. The currents into RADJ and FADJ follow the equation:

$$RADJ, FADJ = (VCC - 0.7) / (Rext + 550\Omega).$$



The diagrams opposite show how driver rise and fall are adjusted by RADJ, FADJ and DBIAS.

Power Down of the Driver

Referring to Table 1, there are configurations in which a driver can be put into a power down mode, and others in which the driver is powered and ready for operation.

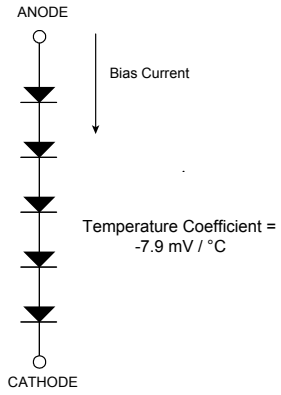
PON[0:3] are the TTL inputs controlling power to the individual driver circuits. A logical 1 will power up the driver. The PON inputs remain effective on a per-driver basis in differential mode.

Thermal Monitor

An on-chip thermal diode string of five diodes in series exists (see figure below). This string allows accurate die temperature measurements.

An external bias current of 100 µA is injected through the string, and the measured voltage corresponds to a specific junction temperature with the following equation:

$$Tj[°C] = \{(ANODE – CATHODE) / 5 – 0.768\} / (–0.00169).$$



Power Supply Sequencing

In order to avoid the possibility of latch-up, the following power-up requirements must be satisfied:

1. VEE <= GND <= VCC at all times
2. VEE <= Analog Inputs <= VCC
3. VEE <= Digital Inputs <= input max voltage or VCC, whichever is less

The following sequencing can be used as a guideline when powering up the E7765:

1. VEE
2. VCC
3. Digital Inputs
4. Analog Inputs

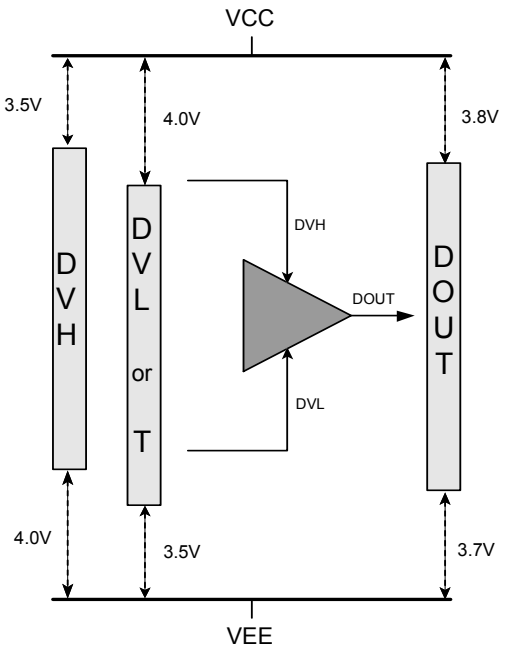
The recommended power-down sequence is the reverse order of the power-up sequence.

Application Information

Computing the Driver Output Voltage Range

The output voltage range of the driver at the DOUT pin is defined by two fundamental calculations. First is the relationship to the power supply voltages at the device (VCC and VEE) and second to the range of programmability of the DVH and DVL input voltages. Remaining in the calculated output voltage range is required to maintain all the DC and AC accuracy specifications for the driver function.

The DOUT range relative to the power supply voltages is straightforward and depicted in the following figure at the output of the driver. The required DOUT range must comply with the noted headrooms to the VCC and VEE power supplies. Headrooms larger than noted is also acceptable but must remain within the power supply recommended operating ranges.



The DOUT range is also dependant on the allowable programming voltages at the DVH and DVL inputs. Each of these inputs have similar requirements for power supply headrooms as DOUT does. These headrooms are also depicted in the figure. Furthermore, the DVH/L inputs will have voltage offsets and gain error specifications. These specifications require that the DVH/L input programming range be greater than the required DOUT voltage range if the worst case offset and gain figures are used. The equation for the resulting minimum and maximum voltage at DOUT is;

$$V_{DOUT(MIN/MAX)} = V_{OFFSET(MIN/MAX)} + [\, V_{IN} * GAIN_{(MIN)} \,]$$

Solving for VIN;

$$V_{IN} = [\, V_{DOUT(MIN/MAX)} + V_{OFFSET(MIN/MAX)} \,] / GAIN_{(MIN)}$$

To solve for the range of V_{IN}, first select the Vout ranges required. For example, if we choose -2.0V for the minimum end and +6.5V for the maximum end of V_{DOUT}, and an offset min/max of -100mV/+100mV and a minimum gain of 0.975 the equations solve as;

For -2.0V;

$$V_{IN(-2V)} = [\, -2.0V - 100mV \,] / 0.975 = -2.154V$$

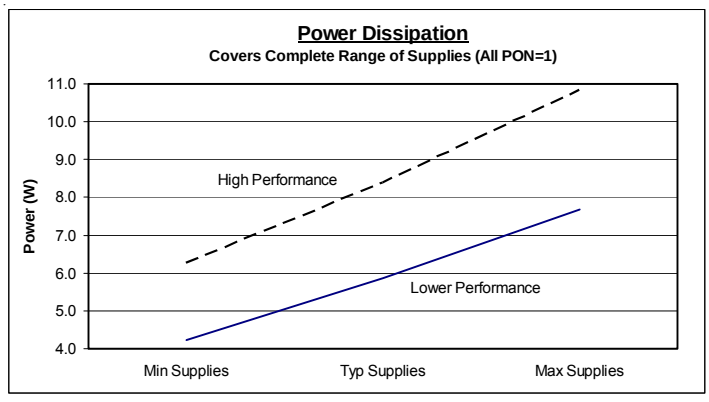
For +6.5V;

$$V_{IN(+6.5V)} = [\, +6.5V + 100mV \,] / 0.975 = +6.769V$$

These resulting V_{IN} values then need to meet the headroom requirements previously mentioned as well as the absolute (relative to ground) voltage limitations specified in the DC specifications data.

Computing Maximum Power Consumption

The diagram below shows the power consumption of the E7765 as a function of power supply and performance bias settings.



Application Information *(continued)*

The power consumption goes up as the power supplies are raised in voltage, and the RADJ, FADJ and DBIAS settings are increased for higher frequency performance. There are specifications and graphs for the relationships of these controls to overall performance in the DC Specifications section. Refer to them for choosing the settings for a particular system performance. This section deals with how to heatsink the various power dissipation levels.

Cooling Considerations

Depending on the applied power supply levels and bias conditions the E7765 will use, various methods of heatsinking will be required to keep the maximum die junction termperature within a safe range and below the specified maximum of 100°C.

The E7765 package has an integral heat slug located at the top side of the package to efficiently conduct heat away from the die to the package top. The thermal resistance of the package to the top is the θ_{JC} (junction-to-case) and is specified at 0.8°C/Watt.

In order to calculate what type of heatsinking should be applied to the E7765, the designer needs to determine the worst case power dissipation of the device in the application. The graph above gives a good visual relationship of the range of power dissipation that can be expected from the E7765. The range of power covers the different modes of operation, power supply settings, and performance bias adjustments available. Use the data and graphs in subsequent sections to determine a particular applications power dissipation.

Another variable that needs to be determined is the maximum ambient air temperature that will be surrounding or blowing on the device and/or the heatsink system in the application (assuming an air cooled system). A heatsinking solution should be chosen to be at or below a certain thermal impedance known as R_θ in units of °C/Watt. The heatsinking system is a combination of factors including the actual heatsink chosen and the selection of the interface material between the E7765 and the heatsink itself. This could be thermal grease or thermal epoxy, and they also have their own thermal impedances. The heatsinking solution will also depend on the volume of air passing over the heatsink and at what angle the air is impacting the heatsink. There are many options available in selecting a heatsinking system. The formula below shows how to calculate the required maximum thermal impedance for the entire heatsink system. Once this is known, the designer can evaluate the options that best fit the system design and meet the required R_θ.

$$R_\theta(\text{heatsink\_system}) = (T_{Jmax} - T_{ambient} - P * \theta_{JC}) / P$$

where, R_θ (heatsink_system) is the thermal resistance of the entire heatsink system

T_{Jmax} is the maximum die temperature (100°C)

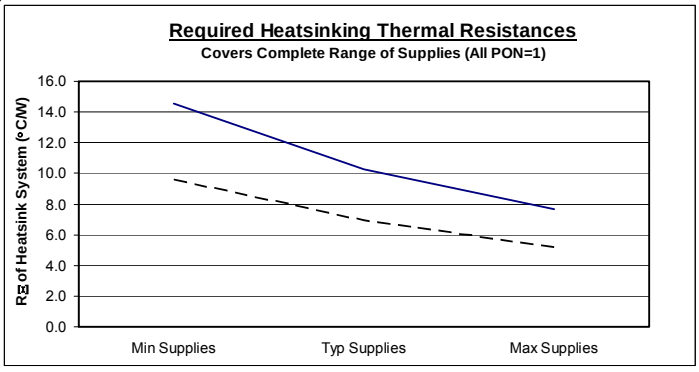
$T_{ambient}$ is the maximum ambient air temp expected at the heatsink (°C)

P is the maximum expected power dissipation of the E7765 (Watts)

θ_{JC} is the thermal impedance of the E7765 junction to case (0.8°C/W)

The graph below uses the power estimates from the previous graph and indicates the required maximum thermal impedances required for the heatsinking system using the above formula with $T_{ambient}$ at 35°C.

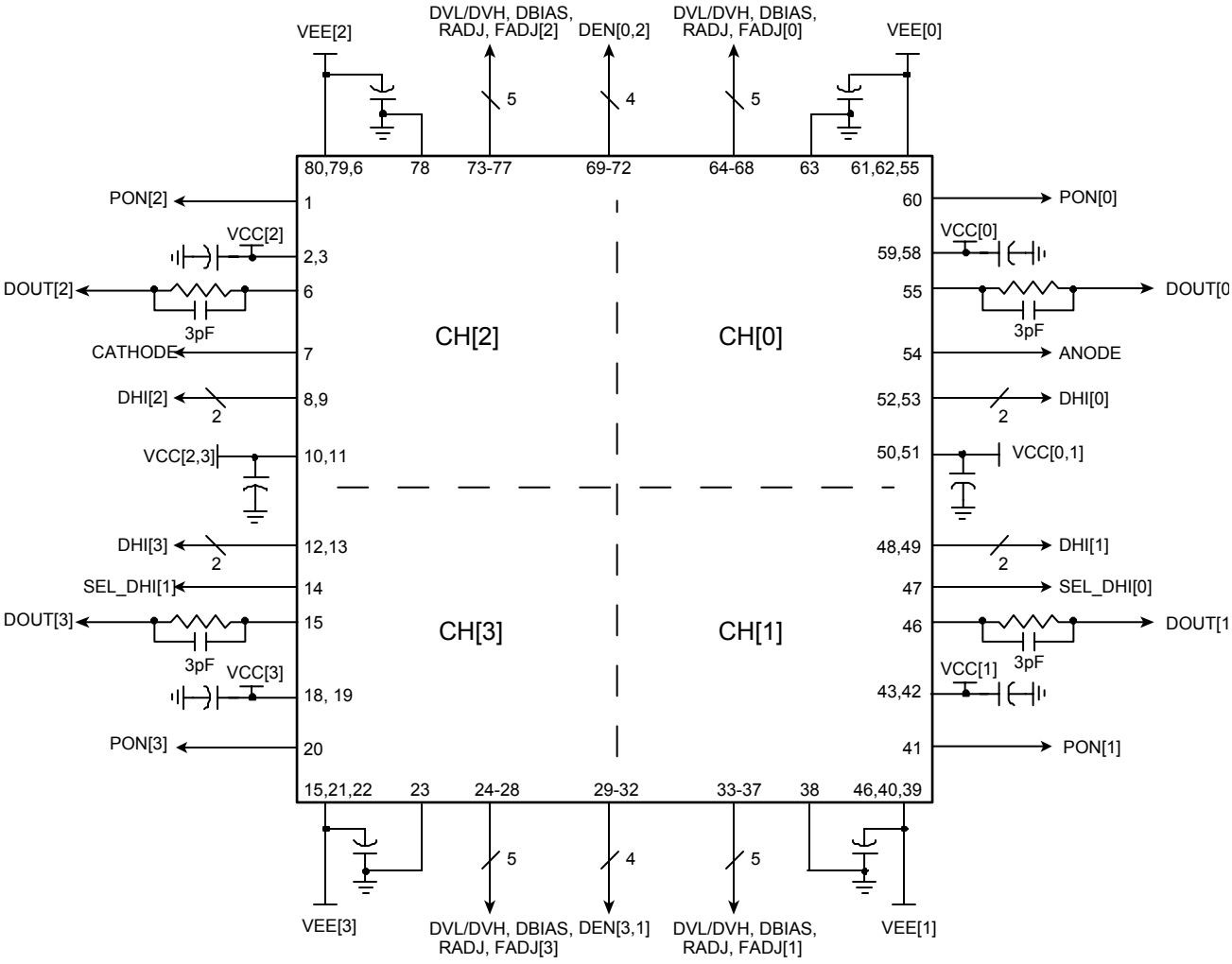
Care needs to be taken when increasing the operating DBIAS, RADJ, FADJ inputs. Monitoring the die temperature to insure adequate heatsinking and airflow is very important.



More information on heatsink system selections can be read on heatsink vendors' web sites and in the Semtech Application Note #ATE-A2 *Cooling High Power, High Density Pin Electronics*.

Application Information *(continued)*

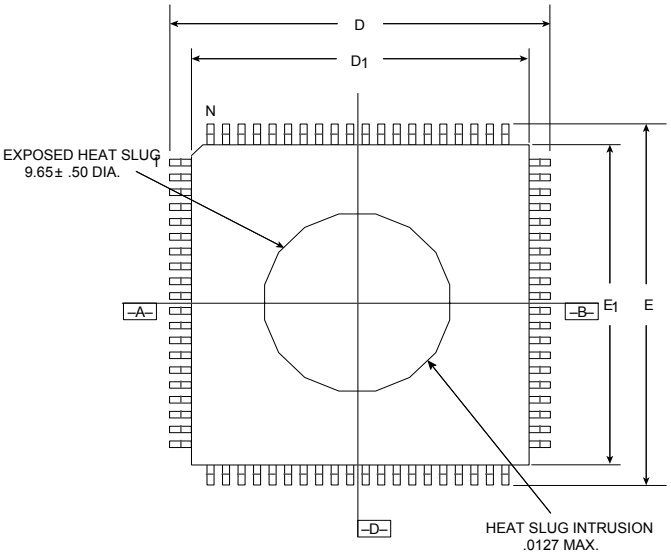
E7765 Hookup



VEEs, VCCs and GNDs of all channels must be connected together.
All capacitors shown are 0.1µF unless otherwise noted.

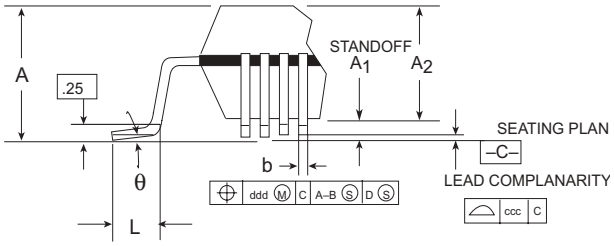
Package Information

14 x 14 x 1.4 mm, 80-Pin LQFP Package (Die Down)
(with Exposed Metal Heat Slug)



Top View

DIMS.	TOL.	
A	MAX	1.60
A_1		.05 min/.15 max
A_2	±.05	1.40
D	±.20	16.00
D_1	±.05	14.00
E	±.20	16.00
E_1	±.05	14.00
L	+.15/-.10	0.60
e	BASIC	0.65
b	±.05	0.30
θ		0° - 7°
ddd	MAX	0.13
ccc	MAX	0.10



NOTES:
1) All dimensions in mm.
2) Dimensions shown are nominal with tol. as indicated.
3) L/F: EFTEC 64T copper or equivalent, 0.127 mm (.005”) or 0.15 mm (.006”) THICK.
4) Foot length “L” is measured at gage plane at 0.25 above the seating plane.
5) Lead finish 85/15 Sn/Pb.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	
VCC (relative to GND)	VCC	0	11.75	V	AM1
VEE (relative to GND)	VEE	–6.5	0	V	AM2
Total Power Supply	VCC – VEE		18.25	V	AM3
Digital Input Voltages	DHI(*), DEN(*)	VEE	VCC	V	AM5
Digital Differential Input Voltages	DHI(*), DEN(*)	–2.5	2.5	V	AM6
Digital TTL Inputs	SEL_DHI, PON	–2.5	VCC	V	AM7
Input Voltages	DVH, DVL	VEE	VCC	V	AM8
Current Inputs	RADJ, FADJ, DBIAS	–0.5	2.5	V	AM10
Analog Input Currents	RADJ, FADJ, DBIAS	0	2	mA	AM12
Driver Output Current	Iout	–40	40	mA	AM15
Driver Swing	DVH – DVL	0	11.5	V	AM16
Storage Temperature	TS	–65	150	˚C	AM18
Junction Temperature	TJ		125	˚C	AM19
Soldering Temperature (5 seconds, .25" from the pin)	TSOL		260	˚C	AM20

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these, or any other conditions beyond those “recommended”, is not implied. Exposure to conditions above those “recommended” for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Positive Power Supply	VCC	8	10	11.6	V
Negative Power Supply (Note 1)	VEE	–6.25	–5	–4.2	V
Total Analog Supply	VCC – VEE	12.2	15	17.85	V
Analog Inputs					
Driver Bias Current	DBIAS		0.6		mA
Driver Slew Rate Adjustments	RADJ, FADJ		0.9		mA
Thermal Resistance of Package (Note 2)			0.8		˚C/W
Junction Temperature	TJ	40		100	˚C

Note 1: For 'Negative' ECL "Flex" inputs (DHI, DEN) with range down to –2V input voltage, VEE - –4.75V.
Note 2: Measured at top of package on exposed heat slug.

DC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
Control Inputs (SEL_DHI, PON)					
Input Low Level	VIL	0		0.8	V
Input High Level	VIH	2		5	V
Input Bias Current	IIN	–50		50	µA

Parameter	Symbol	Min	Typ	Max	Units
DRIVER Circuit					
Output Range	DOUT	–2.0		+7.0	V
	DOUT	VEE + 3.7		VCC – 3.8	V
Analog Inputs					
High Level	DVH	VEE + 4.0		VCC – 3.5	V
	DVH	–1.5		+7.4	V
Low Level	DVL	VEE + 3.5		VCC – 4.0	V
	DVL	–2.25		+6.5	V
Driver Swing	DOUTSW	0.1		8.0	V
Input Current	I_in	–35		+35	µA
Driver Bias	DBIAS	0.5		1.5	mA
Slew Rate Adjustments	RADJ, FADJ	0.3		1.5	mA
RADJ, FADJ, DBIAS Voltage Compliance	VDBIAS, VRADJ, VFADJ	–0.2		+2.0	V
Driver Output (Note 1)					
DC Output Current	Imax	–35		+35	mA
Output Impedance (@ ±25mA) (Note 3)	Rout	4.0	4.7	8.0	Ω
HiZ Leakage (Driver HiZ, Powered Up)		–1		+1	µA
HiZ Leakage (Driver HiZ, Powered Down)		–500		+500	nA
DC Accuracy (Note 1)					
{DESIGN_SPEC: Determine Offset + Gain}					
Offset Voltage (@ DVH = DVL = 0)	DVH, DVL – DOUT	–265		+265	mV
Offset Tempco (DVL = 0V, DVH = 3V)	ΔDOUT/C		0.5		mV/C
Gain (Measured @ allowable –FS and +FS)	ΔDOUT/ΔDVH, ΔDOUT/ΔDVL	0.965		1.0	V/V
Linearity (Full Range @ 0V and 75% of DVH/L max input calibration points) (Note 4)	DOUT INL	–10		+10	mV
Digital Inputs (DHI/DHI*, DEN/DEN*)					
Input Voltage Range (Note 2)	DHI(*), DEN(*)	–2.0		+5.0	V
Differential Input Swing	|Input – Input*|	0.24		2.0	V
Input Current	Iin	–300		+300	µA
Input Capacitance	Cin			3.0	pF

DC Characteristics *(continued)*

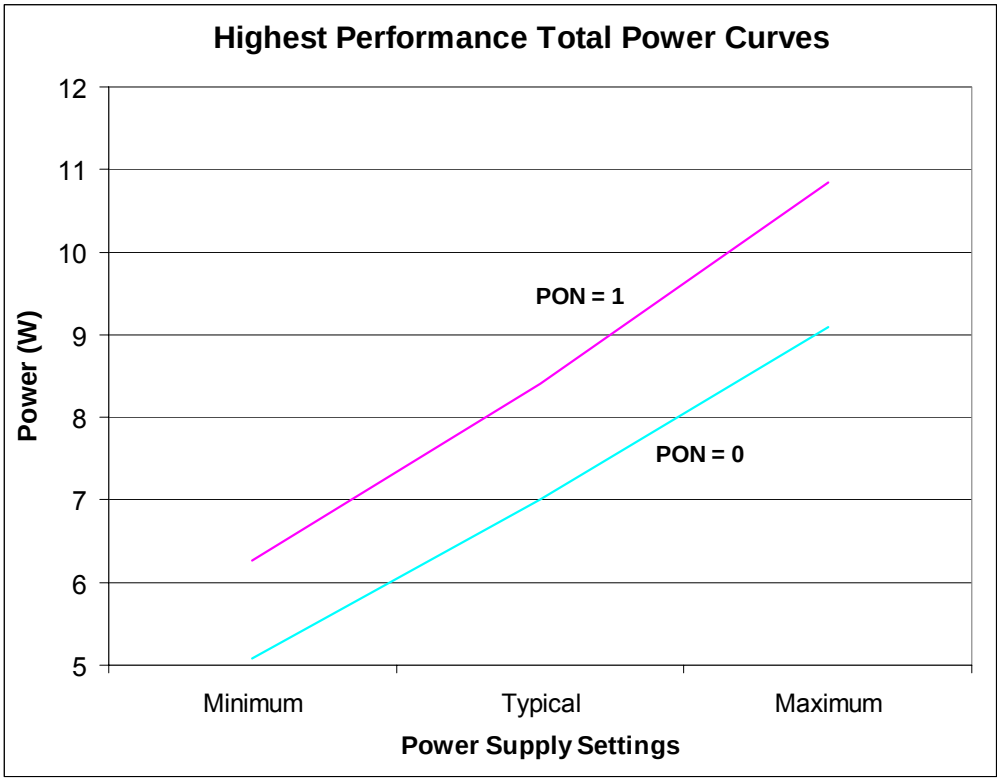
DC conditions (unless otherwise specified): Over the full "Recommended Operating Conditions".

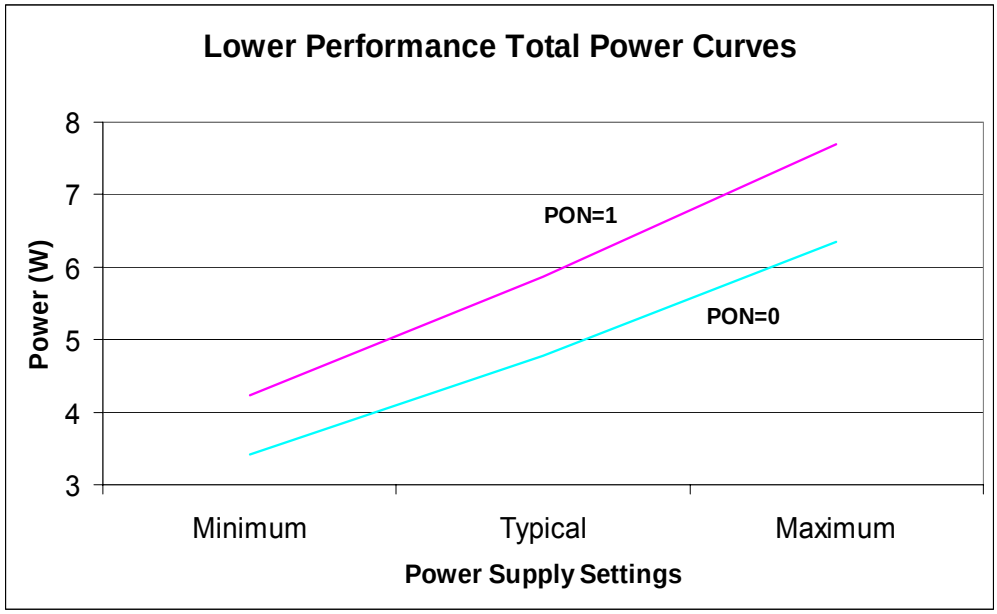
Note 1: See Applications Section describing the applicable “DRIVER OUTPUT RANGE” as a function of VCC and VEE.
Note 2: Digital Input Voltage Range also ≥ VEE + 2.75V.
Note 3: The typical value for Rout should be used to calculate the external resistor for matching to the application’s transmission line impedance.
Note 4: The 2-point calibration for full range should be done at 0V and 75% of the maximum DVH and DVL input. While the 1st calibration point (0V) will be the same for both DVH and DVL, the 2nd calibration point will be different (ie. DVH: 75% * (VCC - 3.5), DVL: 75% * (VCC - 4.0)).

Parameter	Symbol	Min	Typ	Max	Units
Power Supply Currents					
All Drivers Powered ON (PON = 1)					
Positive Supply	ICC		390	430	mA
Negative Supply	IEE	–490	–450		mA
All Drivers Powered Down (PON = 0)					
Positive Supply	ICC		340	370	mA
Negative Supply	IEE	–420	–350		mA

DC conditions: DVL = 0V, DVH = 3V, SEL_DHI[0:1] and DHI[0:3] at logical low.
DBIAS = 0.6mA, RADJ = FADJ = 0.9mA.

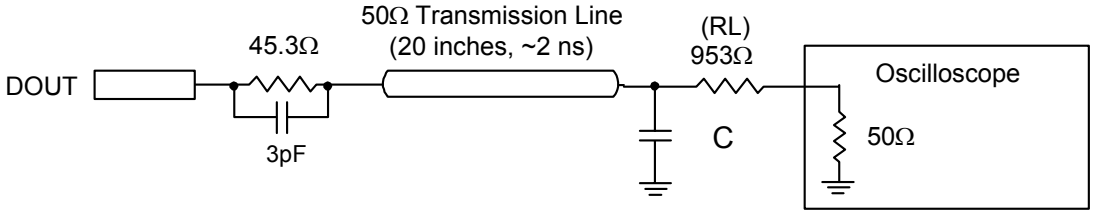
DC Characteristics *(continued)*





AC Characteristics

AC Test Circuit



C	V_{SWING}
3 pF	0.8V (ECL)
3 pF	0.3V (LVDS)
5 pF	3.0V (LVTTL)
8 pF	5.0V (CMOS/TTL)

AC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
DRIVER Circuit (DBIAS = 0.6mA) **(RADJ = FADJ = 0.9 mA unless otherwise noted)**					
Output Impedance (@ ±25mA over temperature and power supplies)	Rout	4.0	6.0	8.0	Ω
Propagation Delay (0 to 1V Output) (Note 1)					
Data (DHI) to Output (Figure 5)	TPLH, TPHL	0.5		1.5	ns
Output Active to HiZ (Figure 4)	TPAZ	0.75		1.5	ns
HiZ to Output Active (Figure 4)	TPZA	1.0		2.0	ns
Rise/Fall Times (Figure 6)					
0 to 1V (20% - 80%)	Tr/Tf		0.13	0.25	ns
0 to 3V (10% - 90%)	Tr/Tf		0.55	0.6	ns
Crossover Voltage Error (Figure 9)	VXOVER	45		55	%
Fmax (R_L=50Ω, swing=programmed value) (Note 2) (Figure 7)					
0 to 1V	Fmax	1200	1300		MHz
0 to 3V	Fmax	600	700		MHz
Pulse Width (R_L=50Ω, swing=programmed value) (Note 2) (Figure 3)	Tpw				
0 to 1V				0.6	ns
0 to 3V				0.9	ns
Pulse Width Dispersion to Minimum Pulse Width (PWmin = 0.5 ns, 50Ω terminated) (Figure 2)	ΔTpw			50	ps
Driver-to-Driver Skew (Diff. Driver Mode) (Note 3)			10	30	ps
Output Capacitance	Cout		4.6		pF
Delay Tempco (Figure 5) (Switching DVH and DVL)	ΔTpd/°C		1	1.5	ps/°C
Delay Symmetry (same driver, 1.0V swing) (Figure 5)	|TPHL – TPLH|			50	ps
Trans. Time Matching (same driver) (Figure 6)					
DOUT = 1.0V	ΔTr,f			50	ps
DOUT = 3.0V	ΔTr,f			100	ps
Overshoot/Undershoot (Figure 8)					
DOUT = 1.0V		0		300	mV
DOUT = 3.0V		0		250	mV
Ringback (Figure 8)					
DOUT = 1.0V				250	mV
DOUT = 3.0V				150	mV
Voltage Crosstalk (when switching adjacent channel)					
DOUT = 1.0V			±9	±20	mV
DOUT = 3.0V			±12	±30	mV
Timing Crosstalk					
DOUT = 1.0V				±12	ps
DOUT = 3.0V				±30	ps

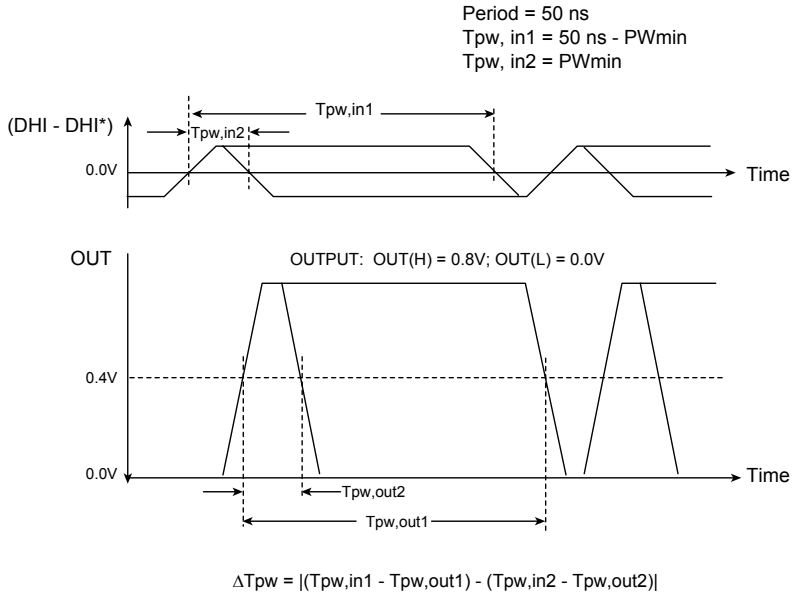
AC test conditions (unless otherwise specified): "Recommended Operating Conditions". VCC = +10V, VEE = –5V.
Note 1: Propagation delays for LV_PECL differential logic inputs.
Note 2: At 10% output amplitude attenuation. CLOAD in AC test circuit = 0 pF.
Note 3: 0 to 800 mV outputs.

AC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
Control Logic					
SEL_DHI (Note 1)	T_{DIFF_D}			50	ns

Note 1: Includes the time needed to settle new drive levels to within 10% of programmed values.

AC Characteristics *(continued)*



The measured result is the absolute value of the change in [Tpw,in – Tpw,out] as the P.W. changes from 25 ns to the end points of PW_{min} and [50ns – PW_{min}].

Figure 2. Driver DIN to OUT Dispersion Measurement Definition

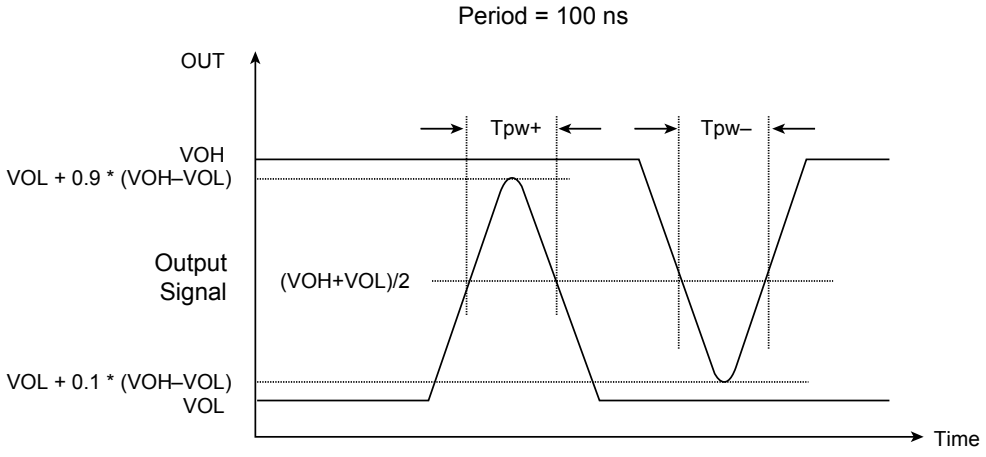


Figure 3. Driver Minimum Pulse Width Measurement Definition

AC Characteristics *(continued)*

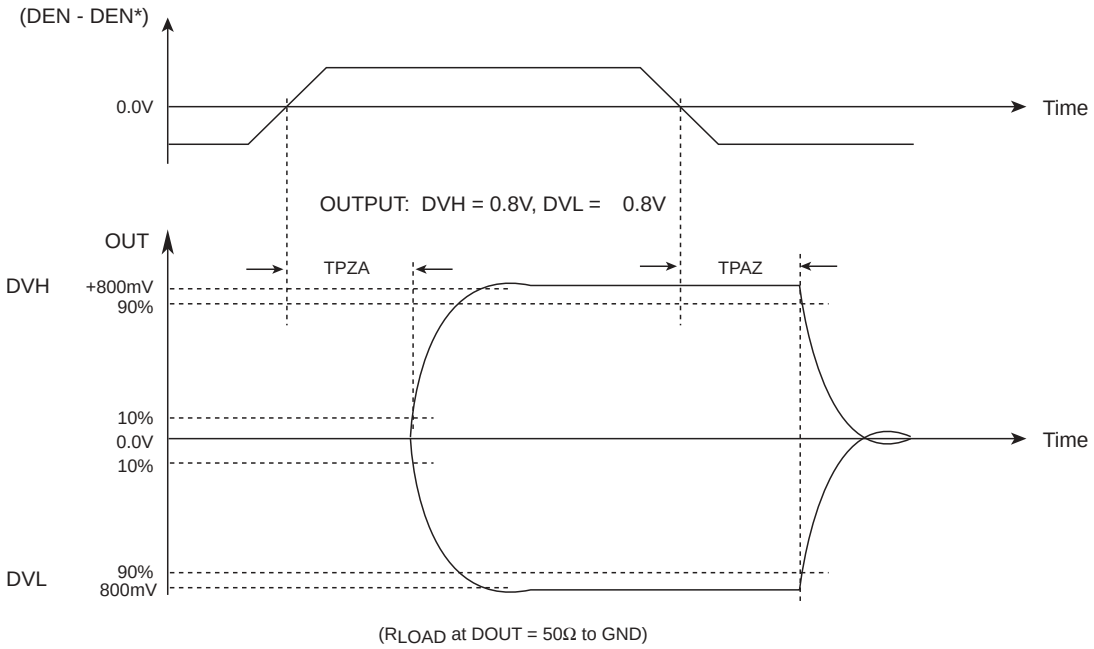


Figure 4. Driver HiZ Enable/Disable Delay Measurement Definition

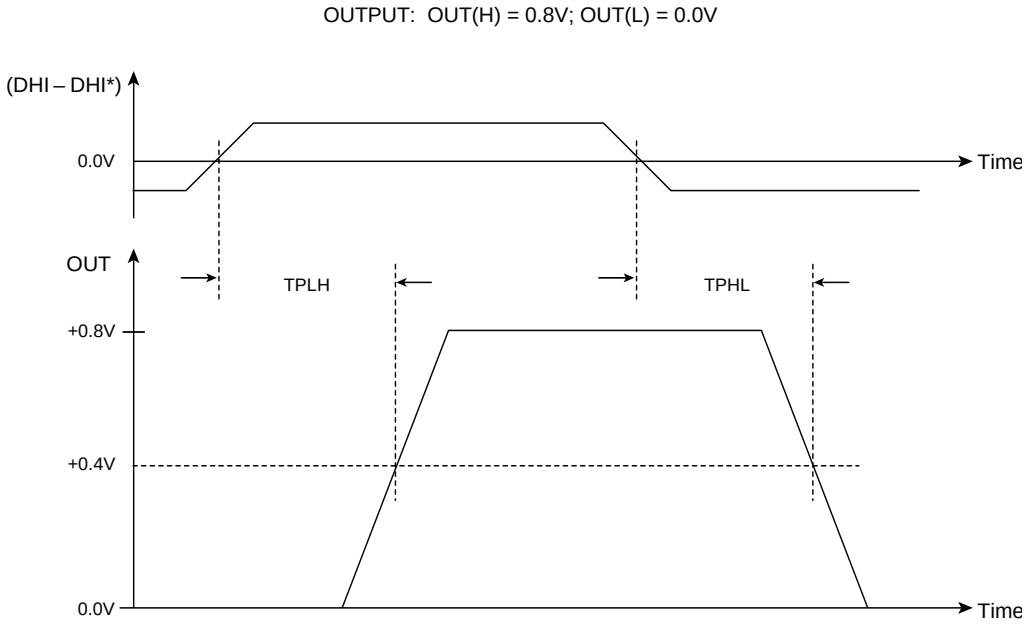
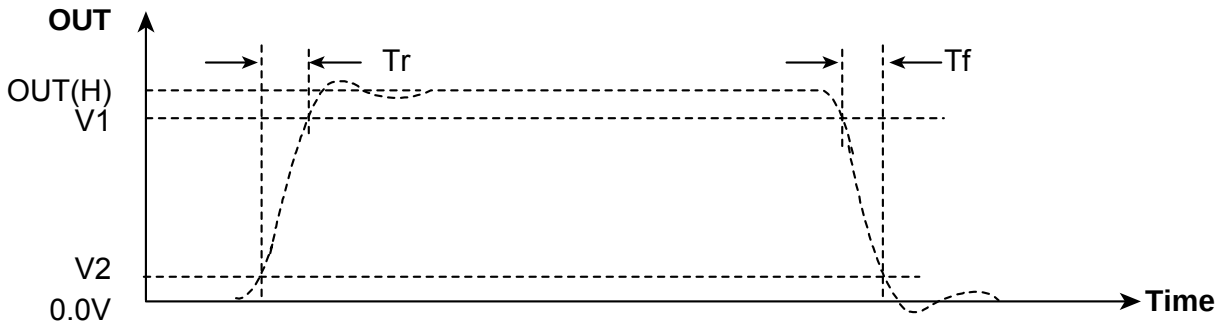


Figure 5. Driver Tpd: DHI to OUT, Symmetry, and Tracking Skew Measurement Definition

AC Characteristics *(continued)*



V2 is 0.1 * OUT(H) for 3V and 5V, 0.2* OUT(H) for 0.8V and lower
V1 is 0.9 * OUT(H) for 3V and 5V, 0.8* OUT(H) for 0.8V and lower

Figure 6. Driver Transition Times and Transition Time Matching Measurement Definition

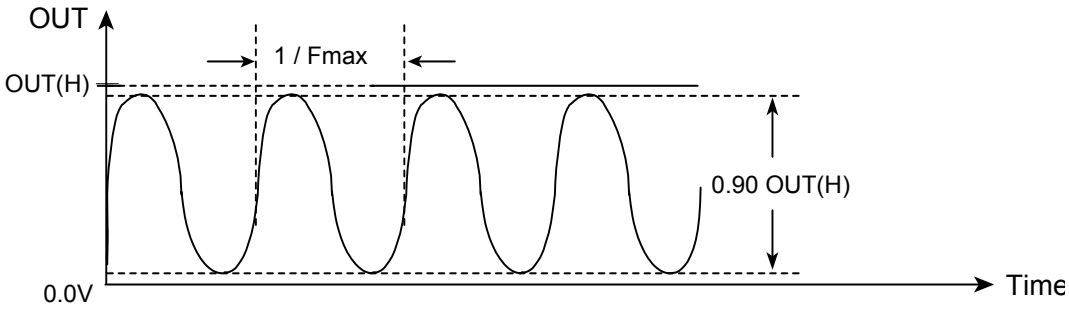


Figure 7. Driver Fmax Measurement Definition

AC Characteristics *(continued)*

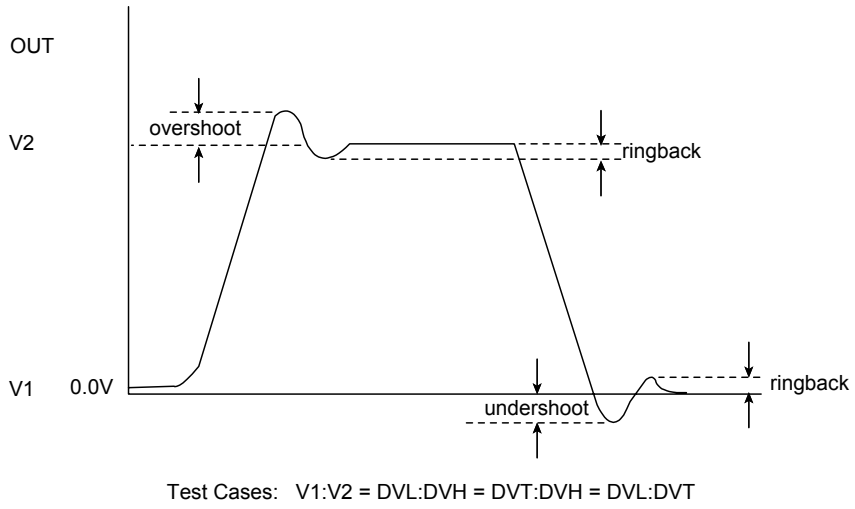


Figure 8. Driver Overshoot, Undershoot, and Ringback

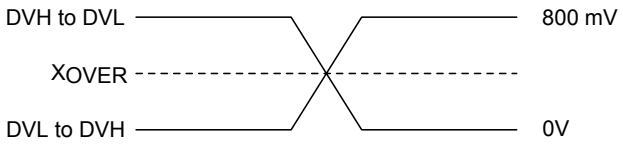


Figure 9. Driver Output Crossover Voltage Measurement

Ordering Information

Model Number	Package
E7765AXF	14 x 14 x 1.4mm, 80-Pin LQFP with Exposed Heat Slug
EVM7765AXF	Edge7765 Evaluation Board

Contact Information

Semtech Corporation
Test and Measurement Division
10021 Willow Creek Rd., San Diego, CA 92131
Phone: (858)695-1808 FAX (858)695-2633