

Complementary N- and P-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY				
	V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
N-Channel	40	0.037 at V _{GS} = 10 V	8	26
		0.046 at V _{GS} = 4.5 V	8	
P-Channel	- 40	0.040 at V _{GS} = - 10 V	- 8	25.5
		0.050 at V _{GS} = - 4.5 V	- 8	

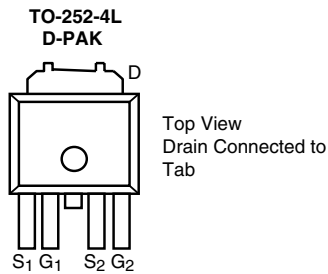
FEATURES

- TrenchFET[®] Power MOSFET
- 100 % UIS Tested

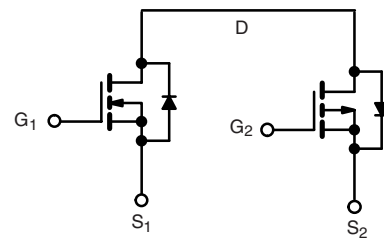


APPLICATIONS

- Backlight Inverter for LCD Display
- Full Bridge DC/DC Converter



Ordering Information: SUD50NP04-77P-T4-E3 (Lead (Pb)-free)



N-Channel MOSFET P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted					
Parameter	Symbol	N-Channel	P-Channel	Unit	
Drain-Source Voltage	V _{DS}	40	- 40	V	
Gate-Source Voltage	V _{GS}	± 20			
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	8 ^a	- 8 ^a	A
		T _C = 70 °C	8 ^a	- 8 ^a	
		T _A = 25 °C	8 ^{a, b, c}	- 8 ^{a, b, c}	
		T _A = 70 °C	7 ^{b, c}	- 7 ^{b, c}	
Pulsed Drain Current (10 μs Pulse Width)	I _{DM}	30	- 30	A	
Source-Drain Current Diode Current	I _S	T _C = 25 °C	8 ^a		- 8 ^a
		T _A = 25 °C	4.3 ^{b, c}		- 4.6 ^{b, c}
Pulsed Source-Drain Current	I _{SM}	30	- 30	mJ	
Single Pulse Avalanche Current	I _{AS}	7	15		
Single Pulse Avalanche Energy	E _{AS}	2.45	11.25	W	
Maximum Power Dissipation	P _D	T _C = 25 °C	10.8		24
		T _C = 70 °C	6.9		15.3
		T _A = 25 °C	5.2 ^{b, c}		5.6 ^{b, c}
		T _A = 70 °C	3.3 ^{b, c}	3.6 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C	

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	N-Channel		P-Channel		Unit
			Typ.	Max.	Typ.	Max.	
Maximum Junction-to-Ambient ^{b, d}	t ≤ 10 s	R _{thJA}	20	24	18	22	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	9.4	11.5	4.3	5.2	

Notes:

- a. Package Limited.
- b. Surface Mounted on 1" x 1" FR4 Board.
- c. t = 10 s.
- d. Maximum under Steady State conditions is 60 °C/W (N-Channel) and 52 °C/W (P-Channel).

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	N-Ch	40			V
		$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-40			
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	N-Ch		44		mV/ $^\circ\text{C}$
		$I_D = -250\text{ }\mu\text{A}$	P-Ch		-41		
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	N-Ch		-5.5		
		$I_D = -250\text{ }\mu\text{A}$	P-Ch		4.3		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	N-Ch	1.4		2.5	V
		$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-1.4		-2.7	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	N-Ch			100	nA
			P-Ch			-100	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$	N-Ch			1	μA
		$V_{DS} = -40\text{ V}, V_{GS} = 0\text{ V}$	P-Ch			-1	
		$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	N-Ch			10	
		$V_{DS} = -40\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	P-Ch			-10	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = 5\text{ V}, V_{GS} = 10\text{ V}$	N-Ch	10			A
		$V_{DS} = -5\text{ V}, V_{GS} = -10\text{ V}$	P-Ch	-10			
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 5\text{ A}$	N-Ch		0.0305	0.037	Ω
		$V_{GS} = -10\text{ V}, I_D = -5\text{ A}$	P-Ch		0.030	0.040	
		$V_{GS} = 4.5\text{ V}, I_D = 4\text{ A}$	N-Ch		0.037	0.046	
		$V_{GS} = -4.5\text{ V}, I_D = -4\text{ A}$	P-Ch		0.036	0.050	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 5\text{ A}$	N-Ch		22		S
		$V_{DS} = -15\text{ V}, I_D = -5\text{ A}$	P-Ch		20		
Dynamic^a							
Input Capacitance	C_{iss}	N-Channel $V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch		640		pF
			P-Ch		1555		
Output Capacitance	C_{oss}	P-Channel $V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch		73		
			P-Ch		176		
Reverse Transfer Capacitance	C_{rss}		N-Ch		41		
			P-Ch		142		
Total Gate Charge	Q_g	$V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V}, I_D = 5\text{ A}$	N-Ch		11.7	20	nC
		$V_{DS} = -20\text{ V}, V_{GS} = -10\text{ V}, I_D = -5\text{ A}$	P-Ch		38.5	60	
Gate-Source Charge	Q_{gs}	N-Channel $V_{DS} = 20\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 5\text{ A}$	N-Ch		5.3	9.0	
			P-Ch		17	27	
Gate-Drain Charge	Q_{gd}	P-Channel $V_{DS} = -20\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -5\text{ A}$	N-Ch		1.9		
			P-Ch		4.2		
Gate Resistance	R_g	$f = 1\text{ MHz}$	N-Ch		2.2		Ω
			P-Ch		3.0		



SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit	
Dynamic^a							
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 20\text{ V}$, $R_L = 4\text{ }\Omega$ $I_D \cong 5\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\text{ }\Omega$	N-Ch		9	18	ns
Rise Time	t_r		P-Ch		10	20	
Turn-Off Delay Time	$t_{d(off)}$	P-Channel $V_{DD} = -20\text{ V}$, $R_L = 4\text{ }\Omega$ $I_D \cong -5\text{ A}$, $V_{GEN} = -10\text{ V}$, $R_g = 1\text{ }\Omega$	N-Ch		11	20	
Fall Time	t_f		P-Ch		14	25	
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 20\text{ V}$, $R_L = 4\text{ }\Omega$ $I_D \cong 5\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\text{ }\Omega$	N-Ch		14	25	
Rise Time	t_r		P-Ch		36	60	
Turn-Off Delay Time	$t_{d(off)}$	P-Channel $V_{DD} = -20\text{ V}$, $R_L = 4\text{ }\Omega$ $I_D \cong -5\text{ A}$, $V_{GEN} = -10\text{ V}$, $R_g = 1\text{ }\Omega$	N-Ch		8	16	
Fall Time	t_f		P-Ch		10	20	
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 20\text{ V}$, $R_L = 4\text{ }\Omega$ $I_D \cong 5\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\text{ }\Omega$	N-Ch		18	30	
Rise Time	t_r		P-Ch		47	80	
Turn-Off Delay Time	$t_{d(off)}$	P-Channel $V_{DD} = -20\text{ V}$, $R_L = 4\text{ }\Omega$ $I_D \cong -5\text{ A}$, $V_{GEN} = -4.5\text{ V}$, $R_g = 1\text{ }\Omega$	N-Ch		14	25	
Fall Time	t_f		P-Ch		60	110	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$	N-Ch			8	A
Pulse Diode Forward Current ^a	I_{SM}		P-Ch			-8	
Body Diode Voltage	V_{SD}	$I_S = 2\text{ A}$	N-Ch		0.805	1.2	V
		$I_S = -2\text{ A}$	P-Ch		-0.76	-1.2	
Body Diode Reverse Recovery Time	t_{rr}	N-Channel $I_F = 2\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$	N-Ch		19	30	ns
Body Diode Reverse Recovery Charge	Q_{rr}		P-Ch		22	40	
Reverse Recovery Fall Time	t_a	P-Channel $I_F = -2\text{ A}$, $di/dt = -100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$	N-Ch		14	25	nC
Reverse Recovery Rise Time	t_b		P-Ch		22	40	
			N-Ch		13		ns
			P-Ch		15		
			N-Ch		6		
			P-Ch		7		

Notes:

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

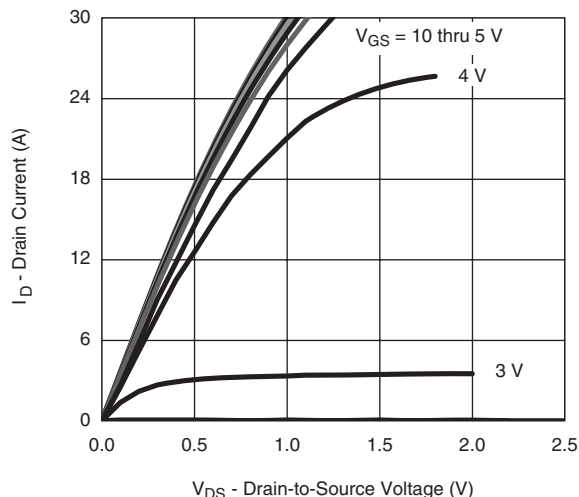
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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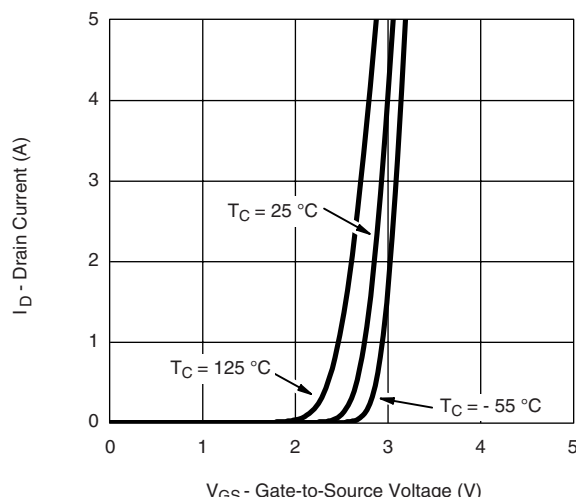


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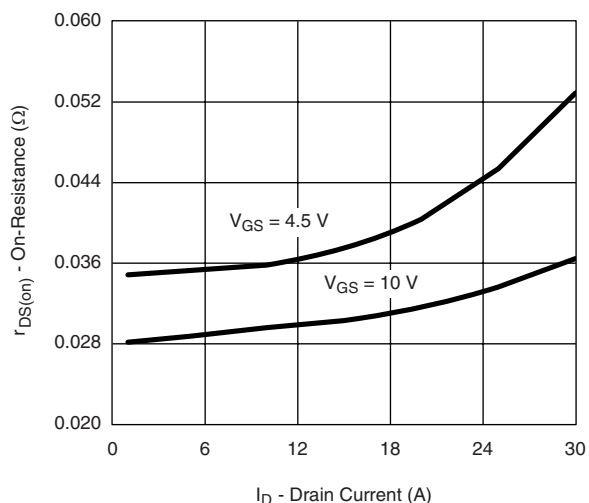
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



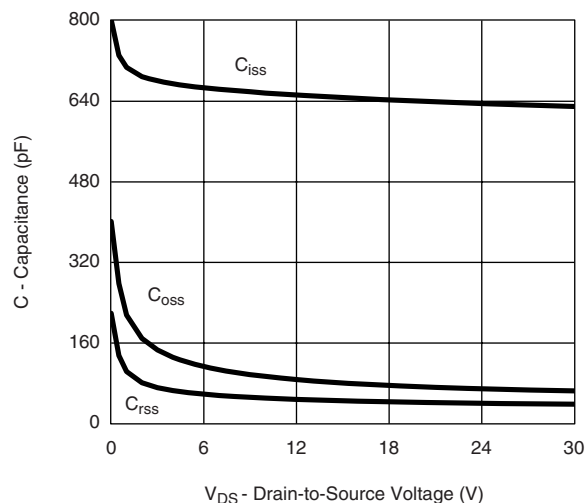
Output Characteristics



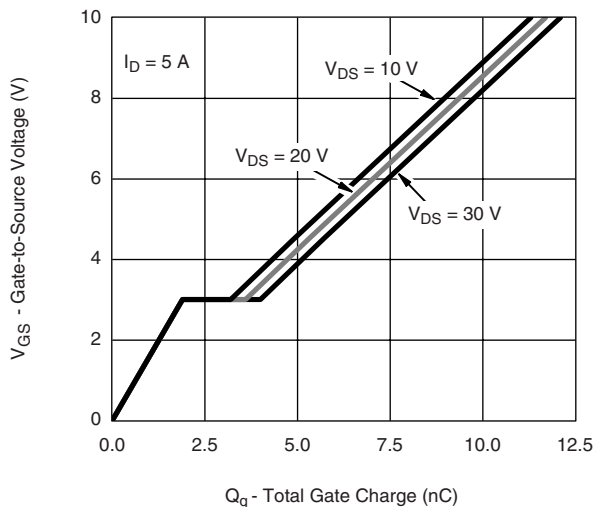
Transfer Characteristics



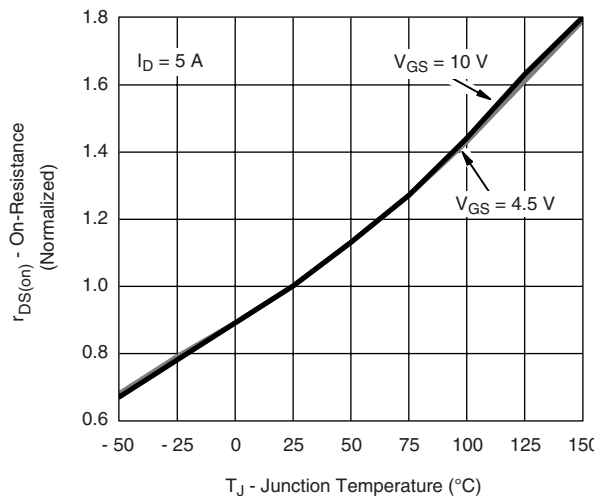
On-Resistance vs. Drain Current



Capacitance



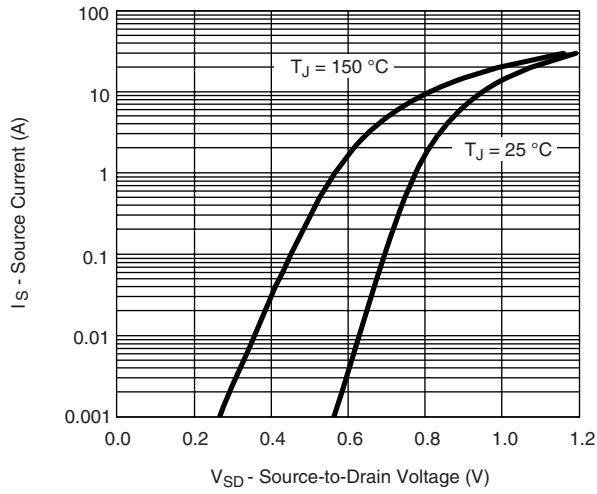
Gate Charge



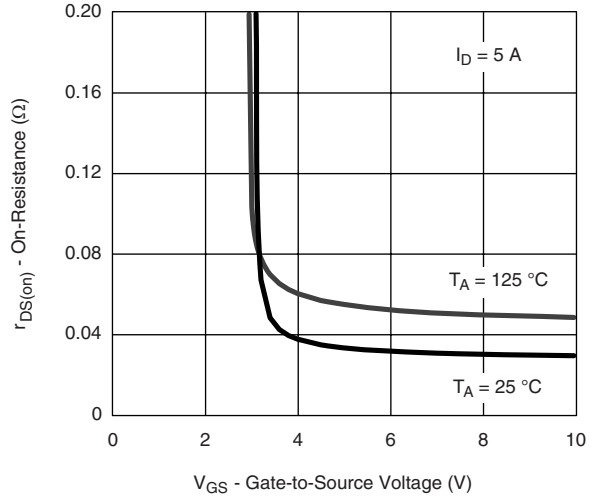
On-Resistance vs. Junction Temperature



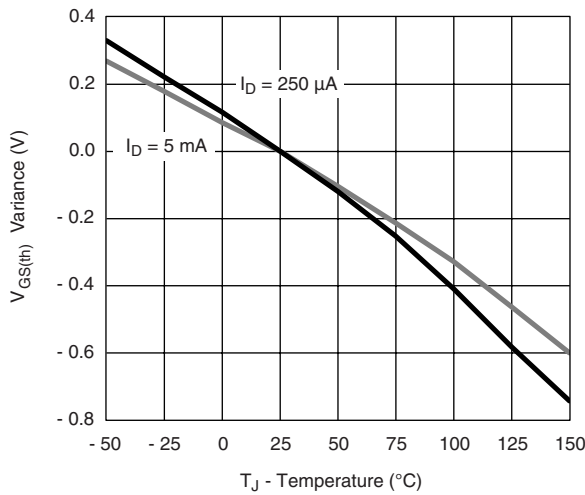
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



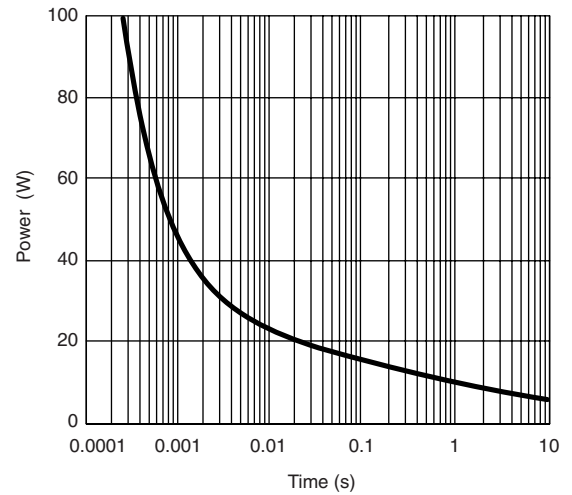
Source-Drain Diode Forward Voltage



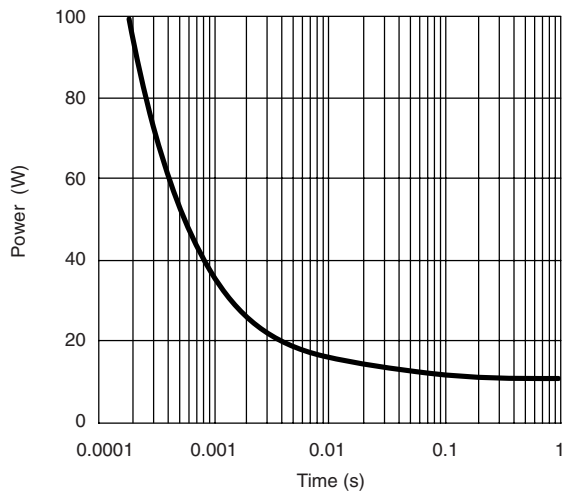
On-Resistance vs. Gate-to-Source Voltage



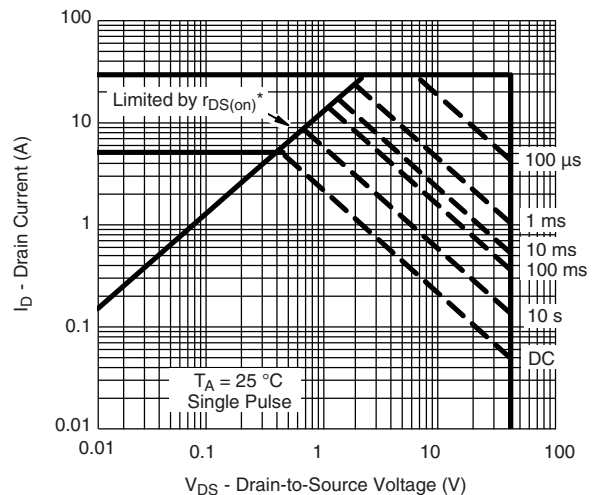
Threshold Voltage



Single Pulse Power, Junction-to-Ambient



Single Pulse Power, Junction-to-Case



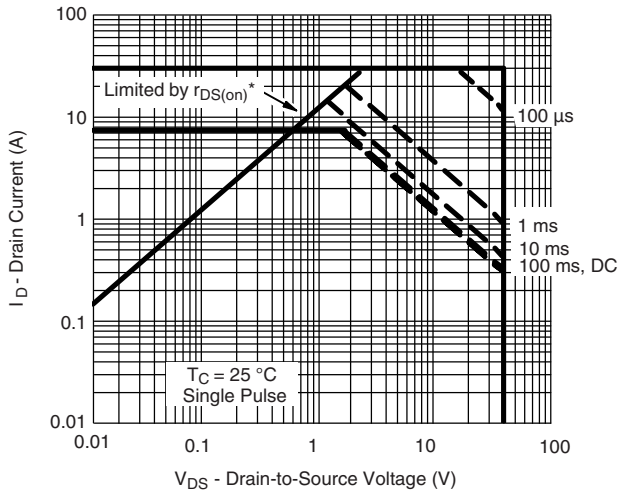
Safe Operating Area, Junction-to-Ambient

SUD50NP04-77P



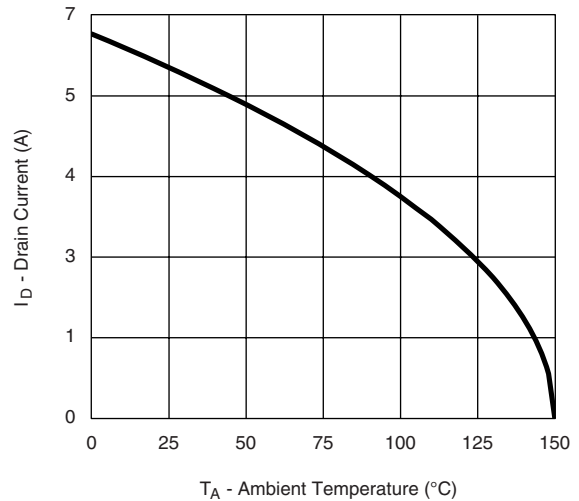
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N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

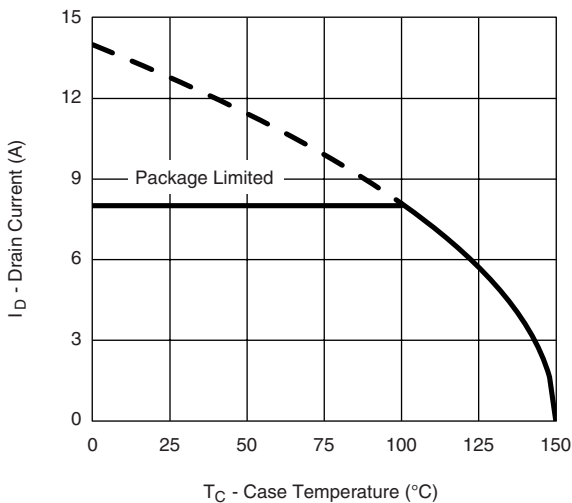


V_{DS} - Drain-to-Source Voltage (V)
* $V_{GS} >$ minimum V_{GS} at which $r_{DS(on)}$ is specified

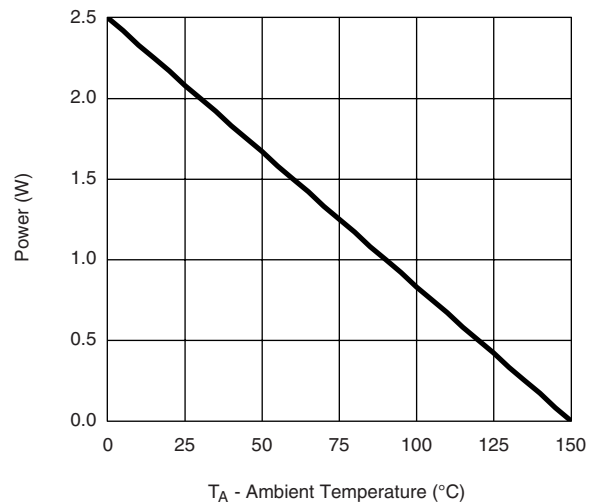
Safe Operating Area, Junction-to-Case



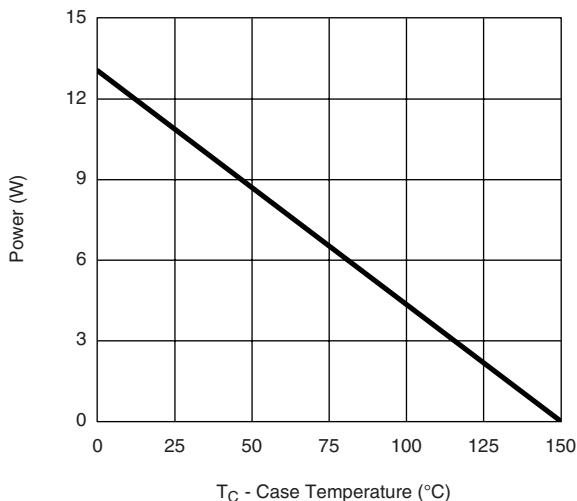
Current Derating, Junction-to-Ambient**



Current Derating, Junction-to-Case**



Power Derating, Junction-to-Ambient

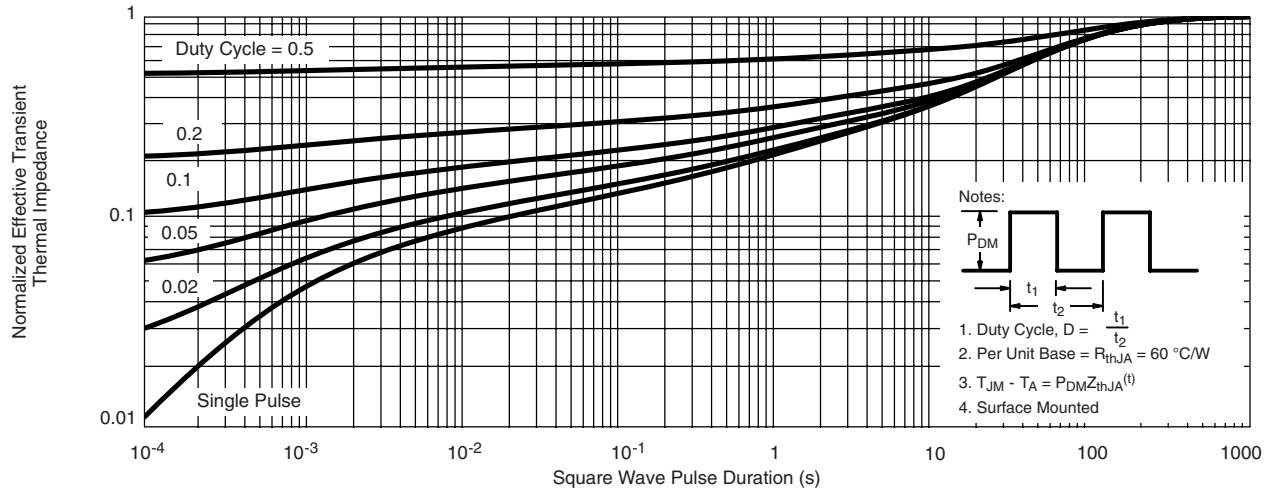


Power Derating, Junction-to-Case

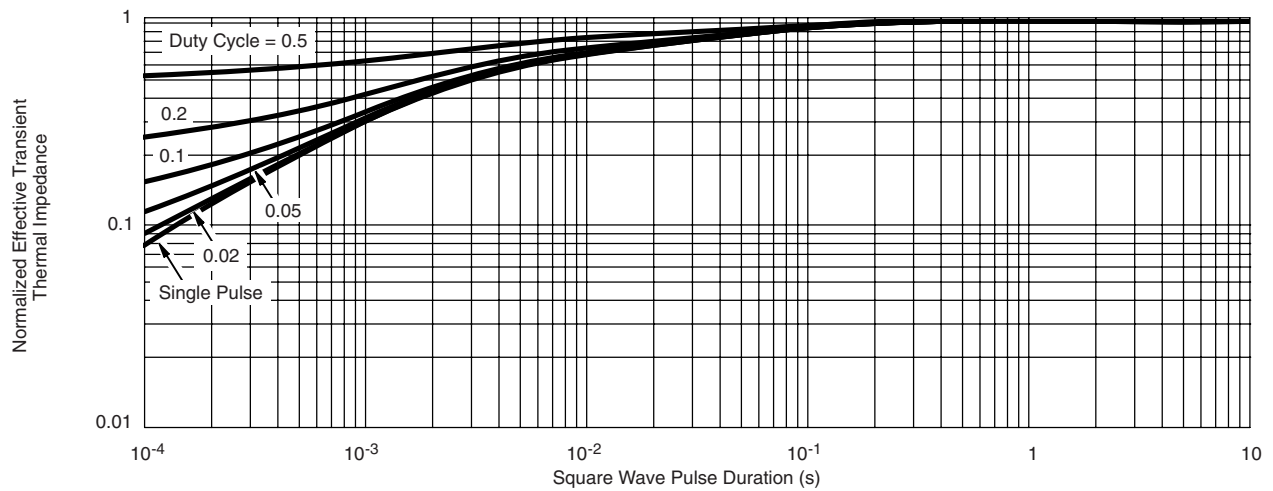
** The power dissipation P_D is based on $T_{J(max)} = 150\text{ }^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



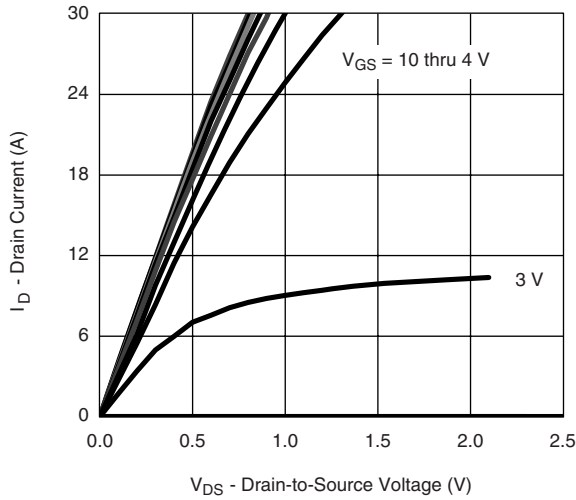
Normalized Thermal Transient Impedance, Junction-to-Case

SUD50NP04-77P

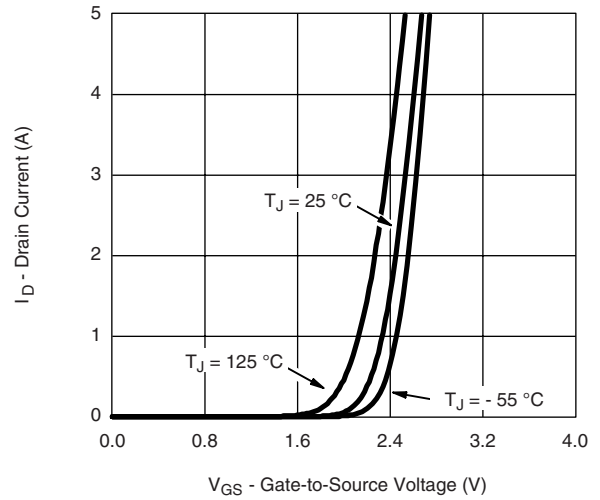


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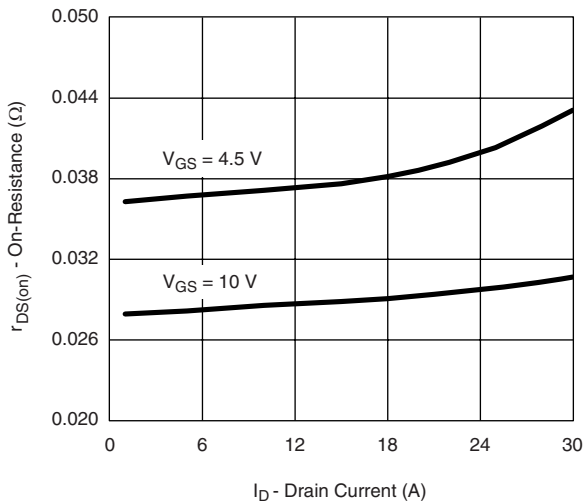
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



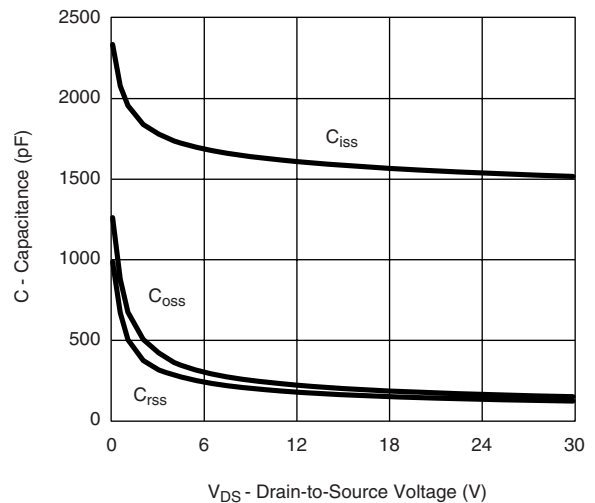
Output Characteristics



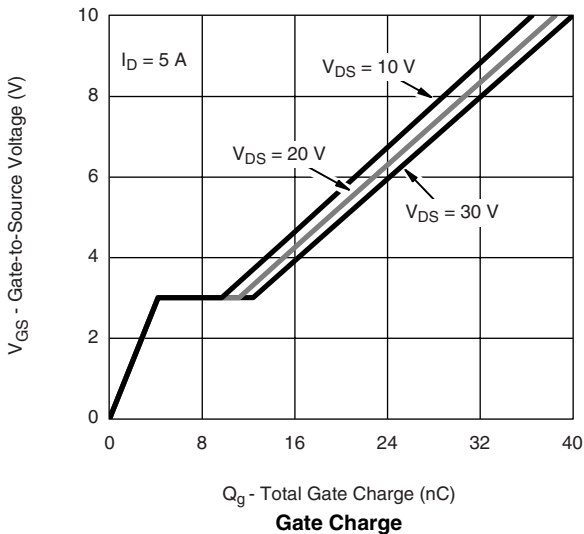
Transfer Characteristics



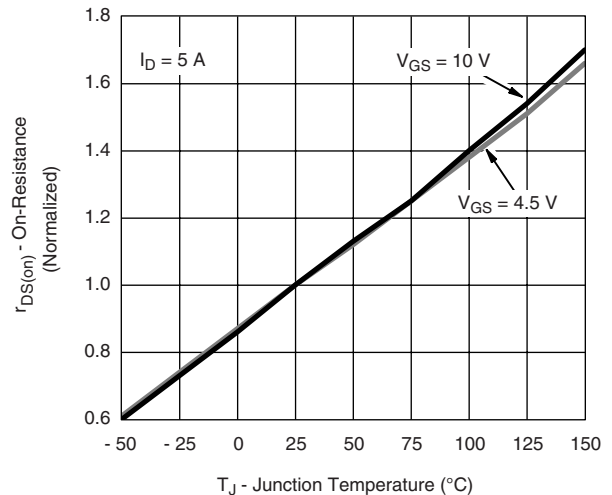
On-Resistance vs. Drain Current



Capacitance



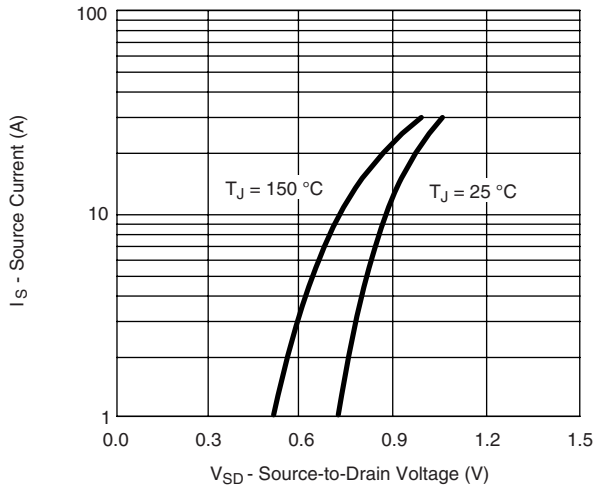
Gate Charge



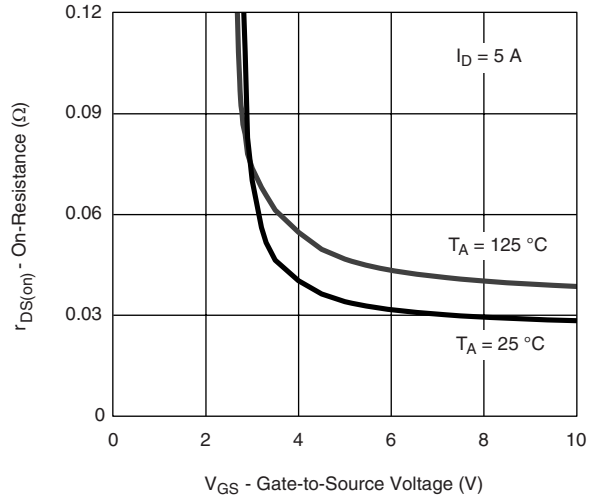
On-Resistance vs. Junction Temperature



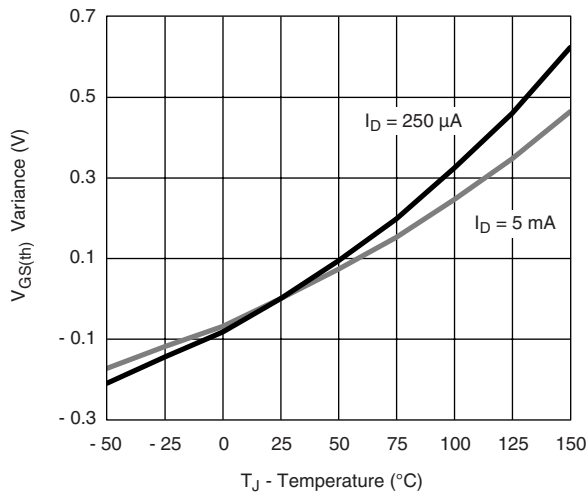
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



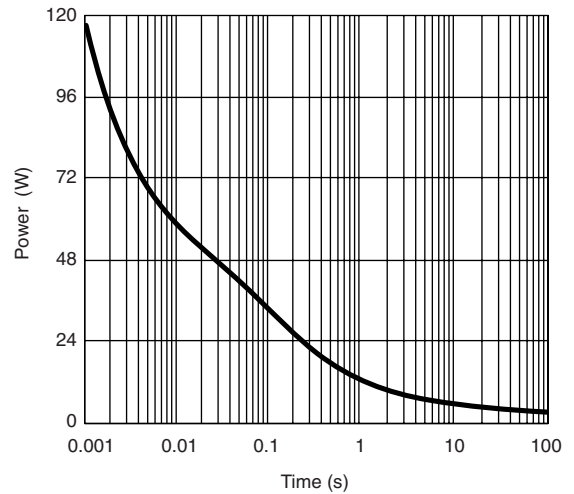
Source-Drain Diode Forward Voltage



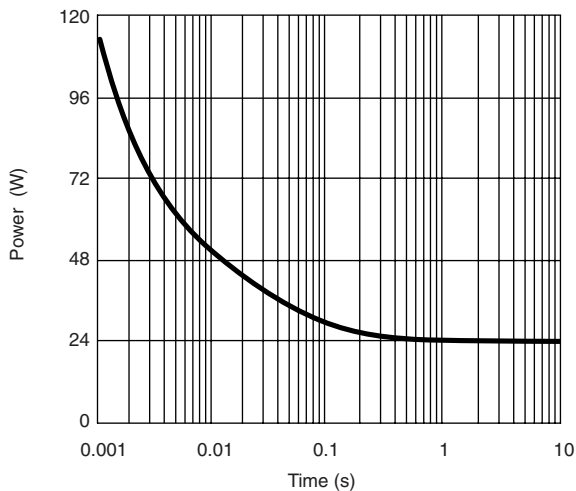
On-Resistance vs. Gate-to-Source Voltage



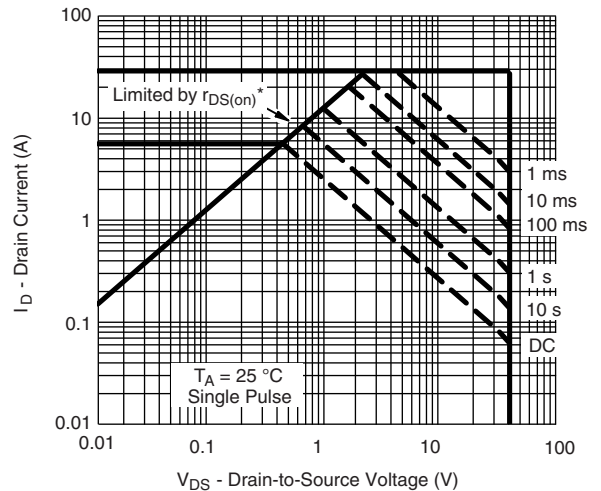
Threshold Voltage



Single Pulse Power, Junction-to-Ambient



Single Pulse Power, Junction-to-Case



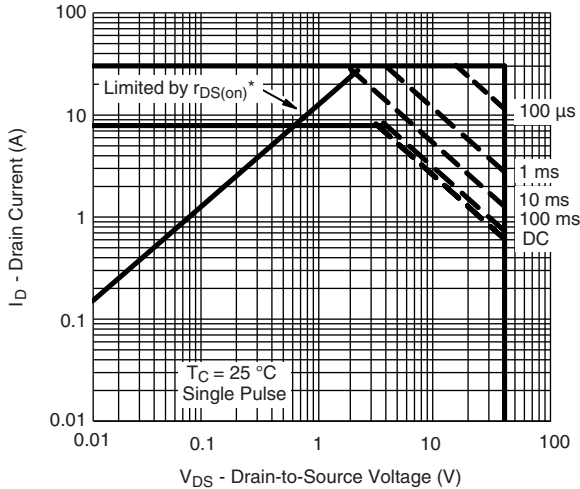
Safe Operating Area, Junction-to-Ambient

SUD50NP04-77P



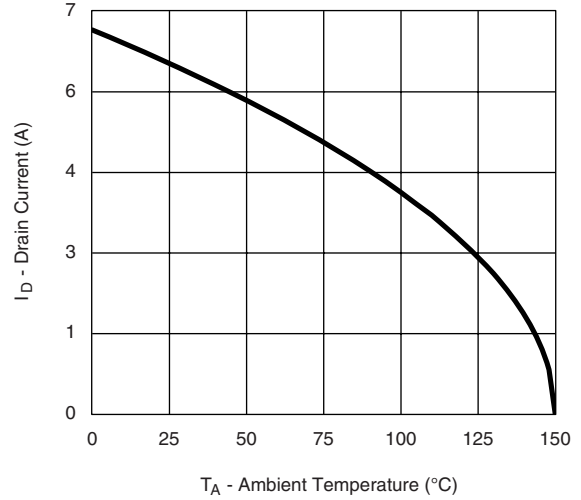
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P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

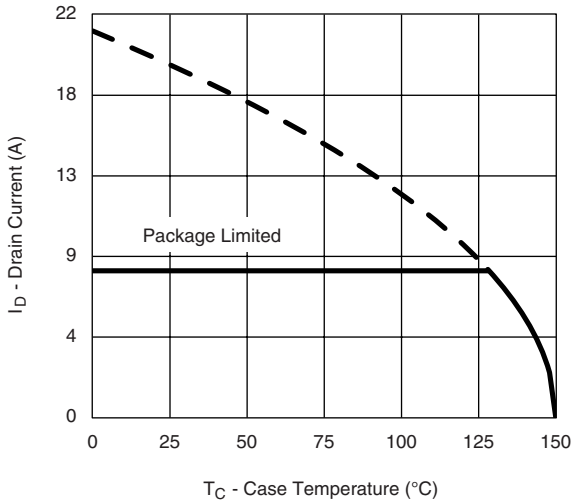


V_{DS} - Drain-to-Source Voltage (V)
* $V_{GS} >$ minimum V_{GS} at which $r_{DS(on)}$ is specified

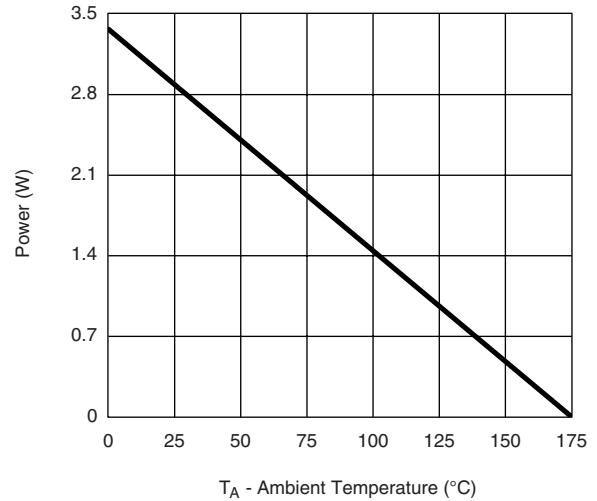
Safe Operating Area, Junction-to-Case



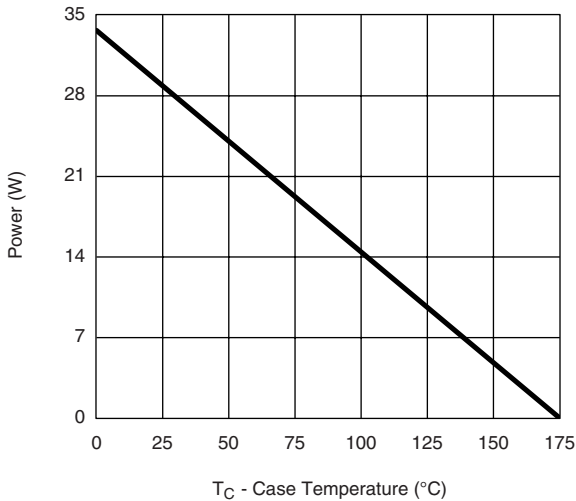
Current Derating, Junction-to-Ambient**



Current Derating, Junction-to-Case**



Power Derating, Junction-to-Ambient

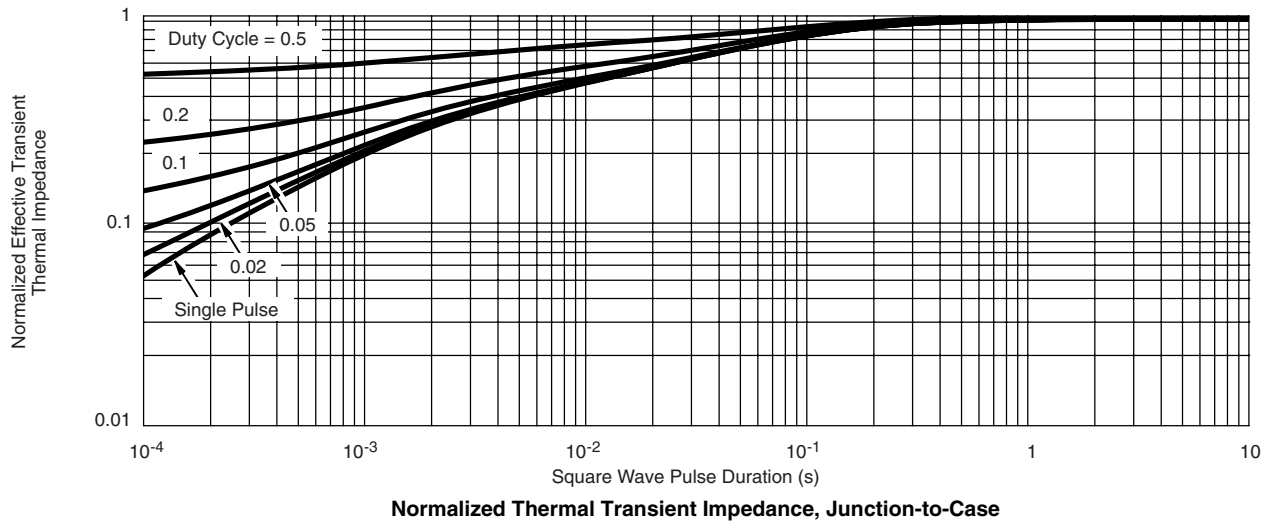
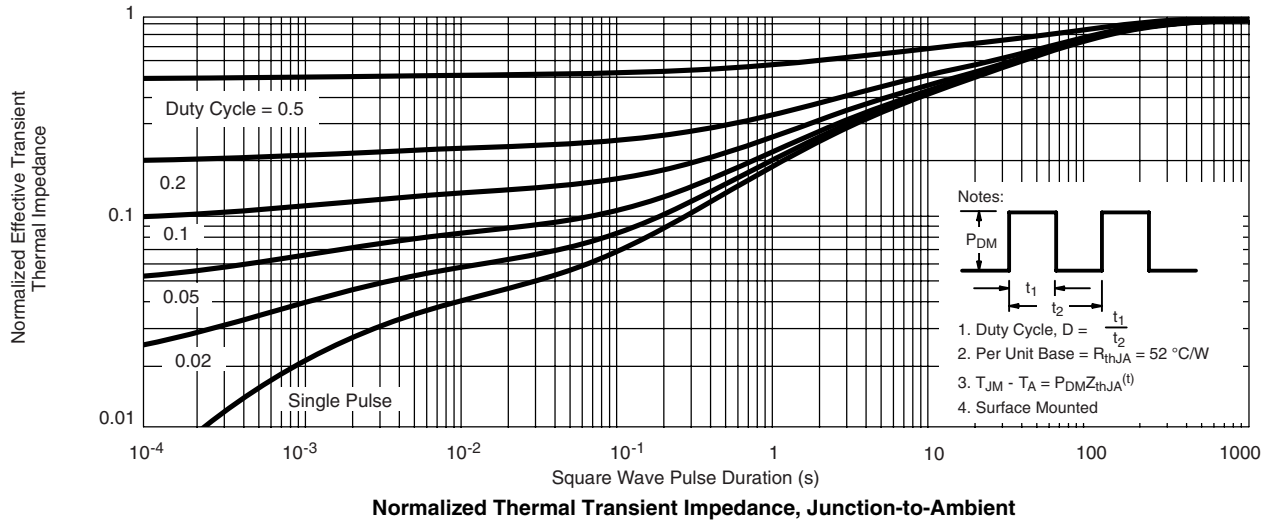


Power Derating, Junction-to-Case

** The power dissipation P_D is based on $T_{J(max)} = 150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?73989>.



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