

F75133**F75133S**

LOADING GAUGE IC

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Version: V0.28P

F75133 Datasheet Revision History

Version	Date	Page	Revision History
V0.23P	2005	-	Release Version
V0.24P	18/04/2005	-	Added Un-Hysteresis Function
V0.25P	26/07/2005	-	Modified Hysteresis Mode Application.
V0.26P	24/01/2006	11	Modified CR04 bit4 Description.
V0.27P	20/12/2006	1	Add Patent Note.
V0.28P	06/07/2007	-	Company readdress

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LIFE SUPPORT APPLICATIONS

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1. General Description

The F75133S is a “Loading Gauge IC”. Loading detection and current monitor are the major applications of the F75133S. The F75133S is following the PWM signal change of duty cycle to react related functions for user application. For instance, the F75133S can be used to sense CPU loading for FAN speed control to cool down the temperature of CPU surface. It also can be used to implement Over/Under-Clocking and Over/Under-Voltage (Vcore) with higher performance/Lower power consumption. Anyway, the F75133S can be implemented by user differential application.

In the past, if engineer would like to measure the parts consumption. He could connect a resistance between power and parts, and then they detected ΔV and capitalized the value to understand the loading condition. Although the method is convenient and needs just a cheap resistance, but some of the accuracy issues and power consumption problem will be the critical points. For example, the resistance will cause more consumption and heat questions if the end-equipment needs mass current to implement. Depends on these problems, more accuracy and more efficiency sensor chip is necessary. The F75133S will handle previous trouble.

The F75133S supports automatic PWM duty cycle detection, follows the result of detection to issue TURBO#, FAULT# and PME# signals for end-application, provides I2C interface for communication, the programmable Cycle-Length of detection rise the measurement accuracy.

The F75133S is packaged in 8-pin SOP and powered by 3.3V.

2. Feature List

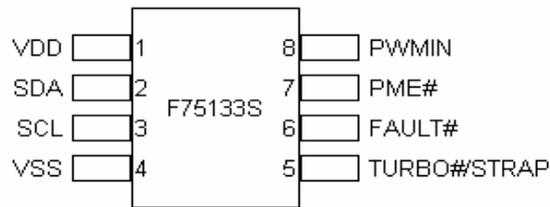
- Automatic PWM Duty Cycle Detect
- Follows the Result of Detection to Issue TURBO#, FAULT# and PME# Signals for End-application
- Programmable Cycle-Length of Detection for Flexible Use and Accuracy
- 4 Steps 5 Stages Over-Clocking Machine
- Un-Hysteresis Function for CPU Over/Under-Clocking/Voltage Implementation
- Internal Oscillator for System Implement.
- 2-Wire I2C Interface
- 3.3V operation voltage.
- 8-pin SOP package.

3. Key Specification

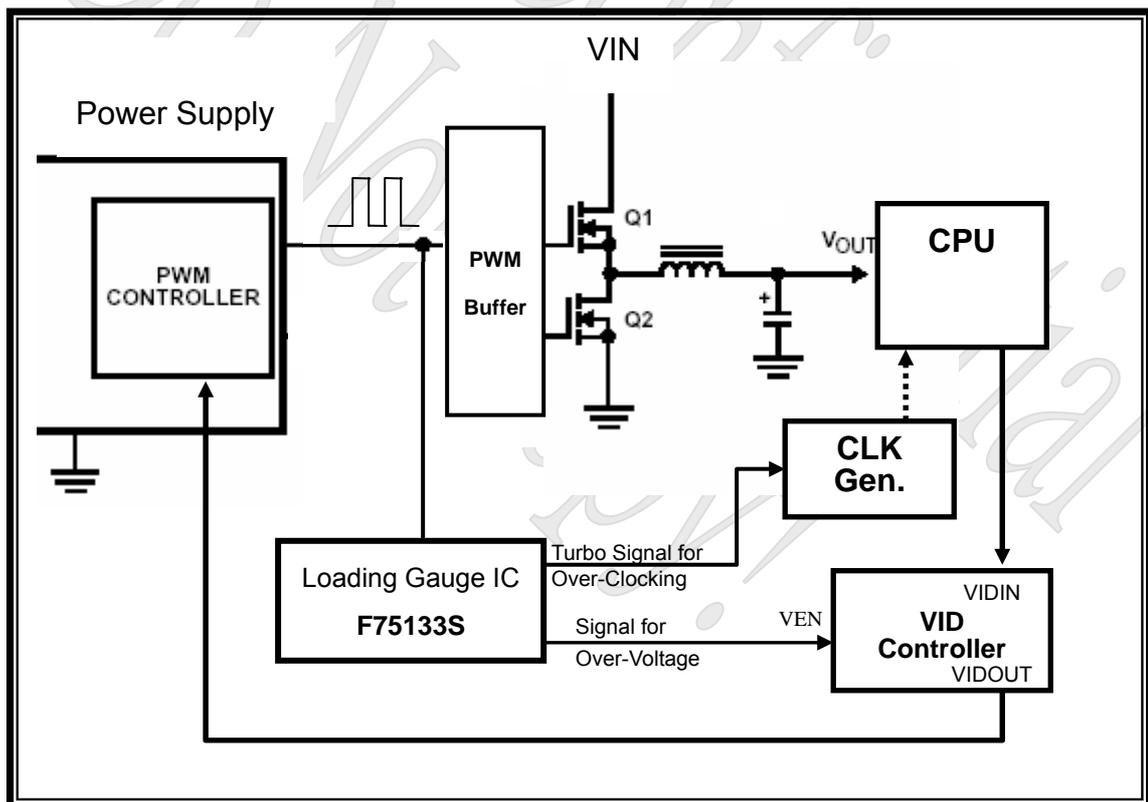
- | | |
|----------------------------|--------------|
| ● Supply Voltage | 3.0V to 3.6V |
| ● Operating Supply Current | 2 mA typ. |

Noted: Patented TWI235553

4. Pin Configuration



5. Application Block Diagram



Application Block Diagram

6. Pin Description

- I/OD_{12st} - TTL level bi-directional pin with schmitt trigger., Open-drain output with 12 mA sink capability.
- O₁₂ - Output pin with 12 mA source-sink capability.
- OD₁₂ - Open-drain output pin with 12 mA sink capability.
- IN_{st} - TTL level input pin with schmitt trigger.
- P - Power.

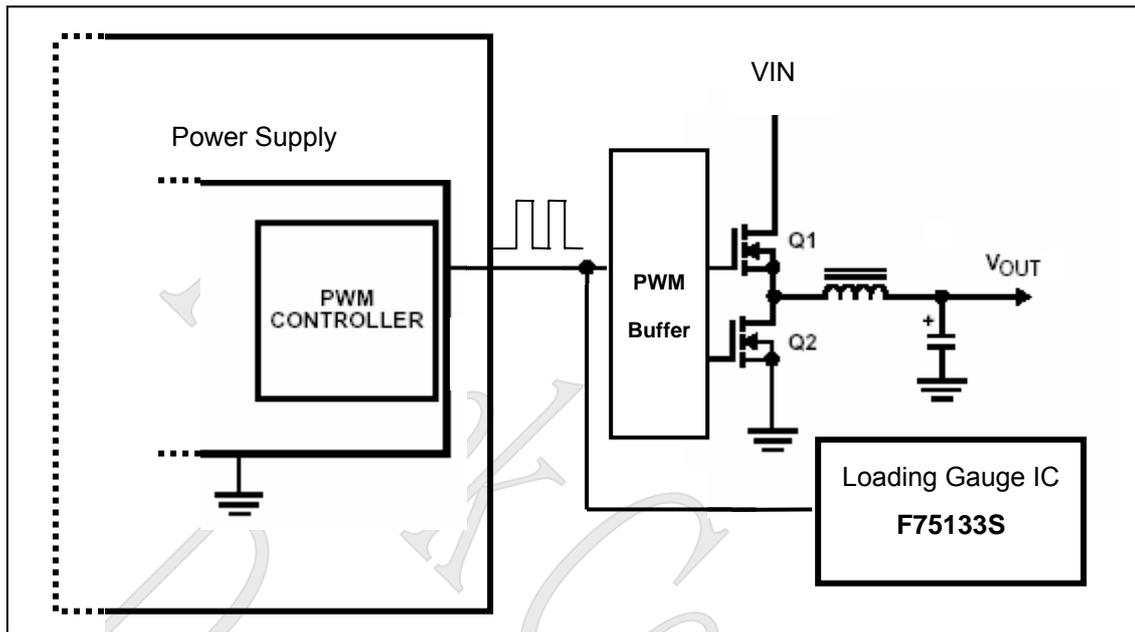
Pin No	Pin Name	Type	PWR	Description
1	VDD	P	-	Main power supply voltage input with 3.3V.
2	SDA	I/OD _{12st}	VDD	Serial data input/output. (5V Tolerance)
3	SCL	IN _{st}	VDD	Serial clock input. (5V Tolerance)
4	VSS	P	-	Ground.
5	TURBO#/STRAP	O ₁₂	VDD	General TURBO signal output pin. (5V Tolerance)
				Power on strapping pin. (5V Tolerance)
6	FAULT#	OD ₁₂	VDD	General FAULT event pin. (5V Tolerance)
7	PME#	OD ₁₂	VDD	General PME event pin. (5V Tolerance)
8	PWMIN	IN _{st}	VDD	PWM input sensor pin. (5V Tolerance)

7. Function Description

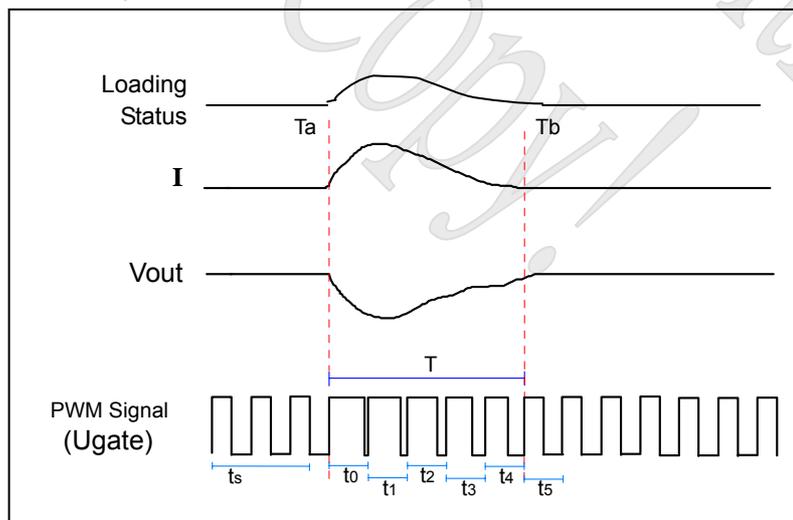
7.1 General Description

As the below circuit, the F75133S can directly sense PWM controller's duty cycle to find out the current loading of equipments. In the past, if engineer would like to measure the consumption of parts, could put a resistance between power and parts, then detected ΔV and capitalized the value to understand the loading condition. Although the method is convenient and needs just a cheap resistance, but some of the accurate issues and power consumption problem will be the critical points. For example, the resistance will cause more consumption and heat questions if the end-equipment needs mass current to implement. Depends on these problems, more accuracy and more efficiency sensor chip is necessary. The F75133S will handle previous trouble.

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The signal of PWM controller is as below illustration. When the end-equipment works steady, the electric current I , voltage V , Loading status and PWM signal (ex. Duty cycle = 50%) are stable simultaneously during t_s . If now the loading of equipment increases at T_a point. The duty cycle of PWM signal will automatic adjust the duty cycle (ex Duty cycle = 90%) for controlling the external switch MOS to stabilize V to original position. And the voltage V will resume to pre-value after T_b point duration. In the same reason, the duty cycle of PWM signal will return to 50%. In this case can easy to recognize the relationship between Loading and PWM signal. The F75133S can capitalize the duty cycle of PWM to find out the equipment loading, and the F75133S also decreases the power consumption issues and solves heat problem.



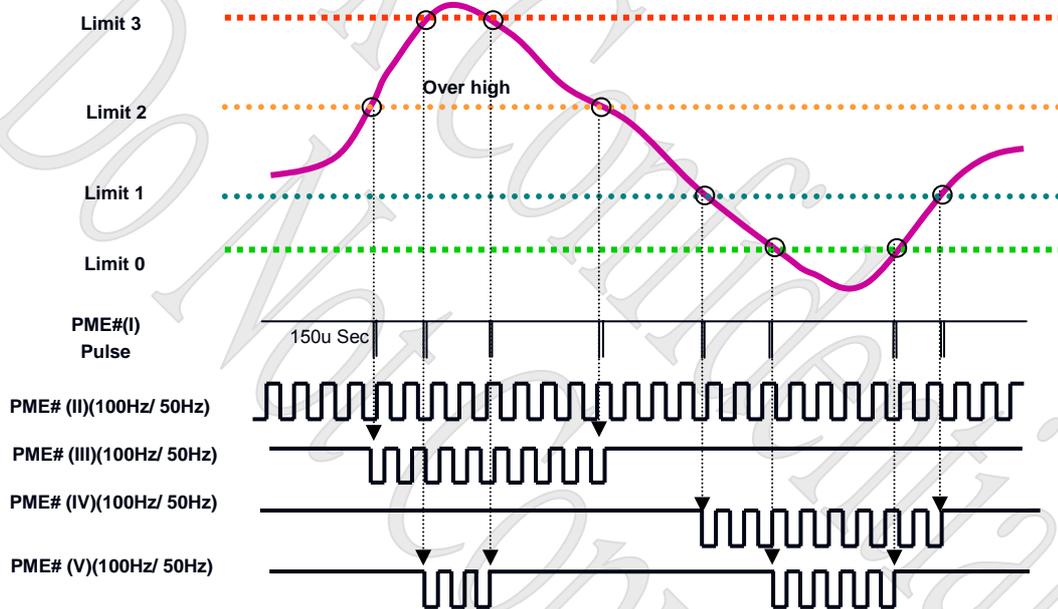
In detail applications, F75133S provides 16bits-resolution sensor to detect the PWM duty cycle and supports 12bits-resolution engine for related limitation setting. User can decide monitor cycle via register setting (default value is about 0.554 Sec). Besides, the F75133S product can be used to calculate multiple phases loading value by 1, 2, 3 or 4 phases. Otherwise, user can select different application from F75133S as TURBO Mode, TURBO_SEL 0 Mode and TURBO_SEL 1 Mode. As much as these features, the F75133S also provides special

PME#/TURBO# Pin Mode output for particular usages.

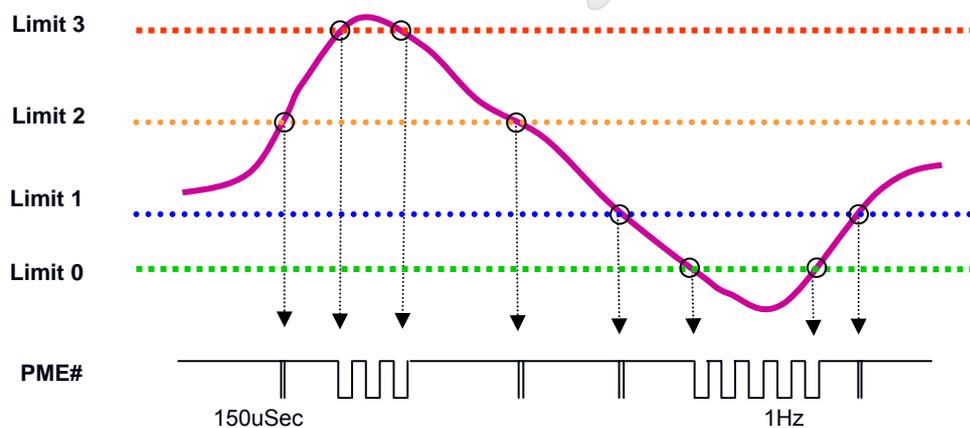
7.2 PME# pin function

As the description as above, there are some functions on each pin of different mode. On PME# pin, there are six options in PME Multiple Function and PME Special modes. The sketch shows as below. User can choose one of those PME functions by register if you need. For instance, if user choose PME#(1) function, PME# pin will issue negative pulse when the loading over anyone of the limits. (More detail, please refer the register description).

PME Multiple Function:



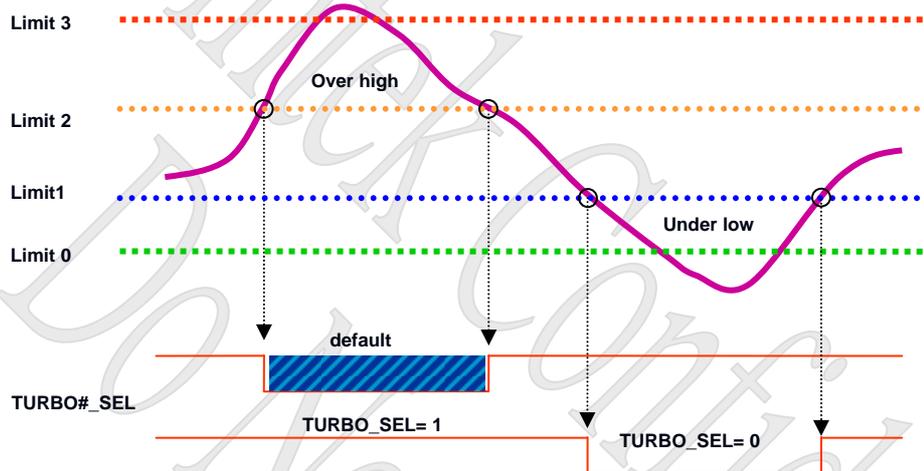
PME Special mode:



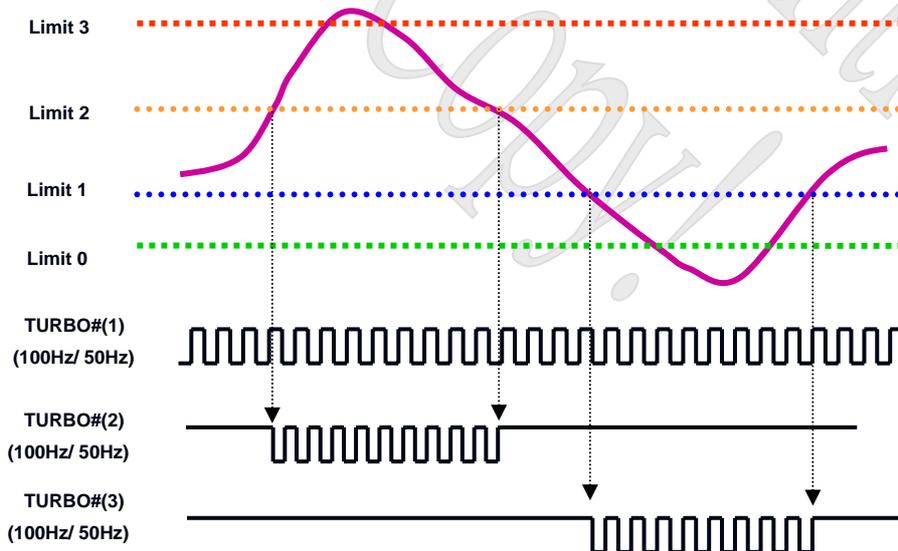
7.3 TURBO# pin function

As same as the PME# pin, there are five options in Turbo normal function and Turbo multiple function modes. The sketch shows as below. (More detail, please refer the register description).

Turbo normal function:



Turbo multiple function:

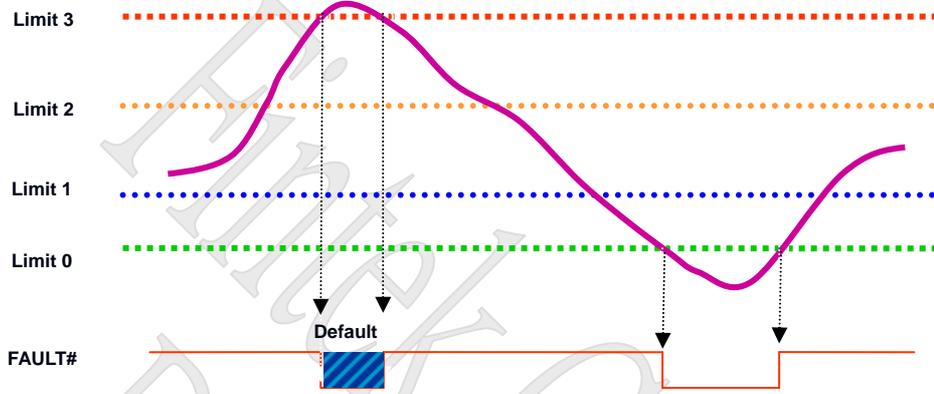


7.4 Fault# pin function

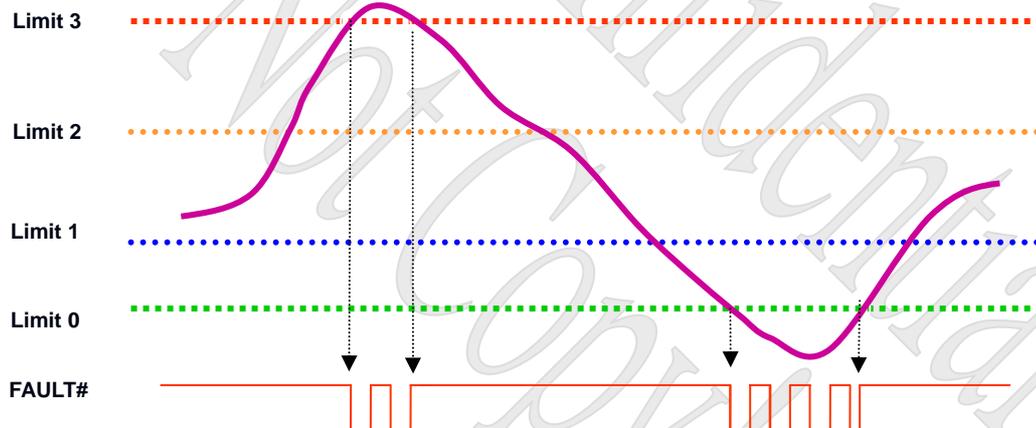
As same as above, there are several options in Turbo normal function and Turbo multiple function modes.

The sketch shows as below. (More detail, please refer the register description).

Fault normal function:



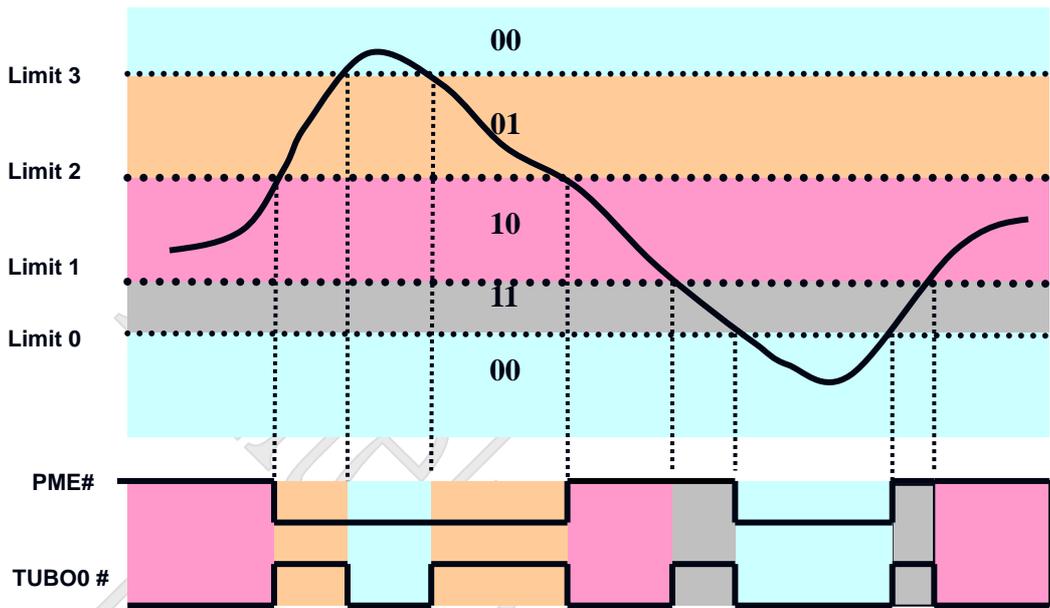
Fault LED mode function:



7.5 Turbo mode pin PME and pin TURBO function

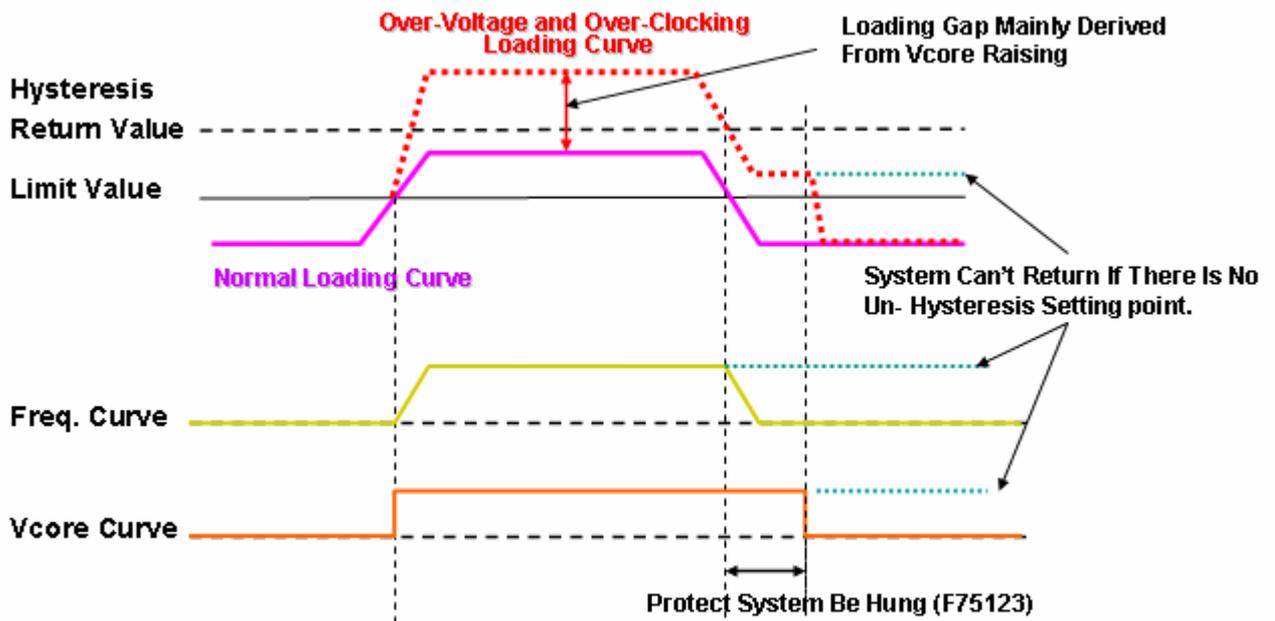
In Turbo mode, the PME#/TRUBO# pins will be TURBO1/TURBO0 pins for CLK Gen. over-clocking usage. User can couple these two pins to CLK Gen. to implement performance. If user chooses this mode, there are four steps and five stages for different frequency use for over-clocking or under-clocking. (More detail, please refer the register description).

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7.6 Un-Hysteresis function

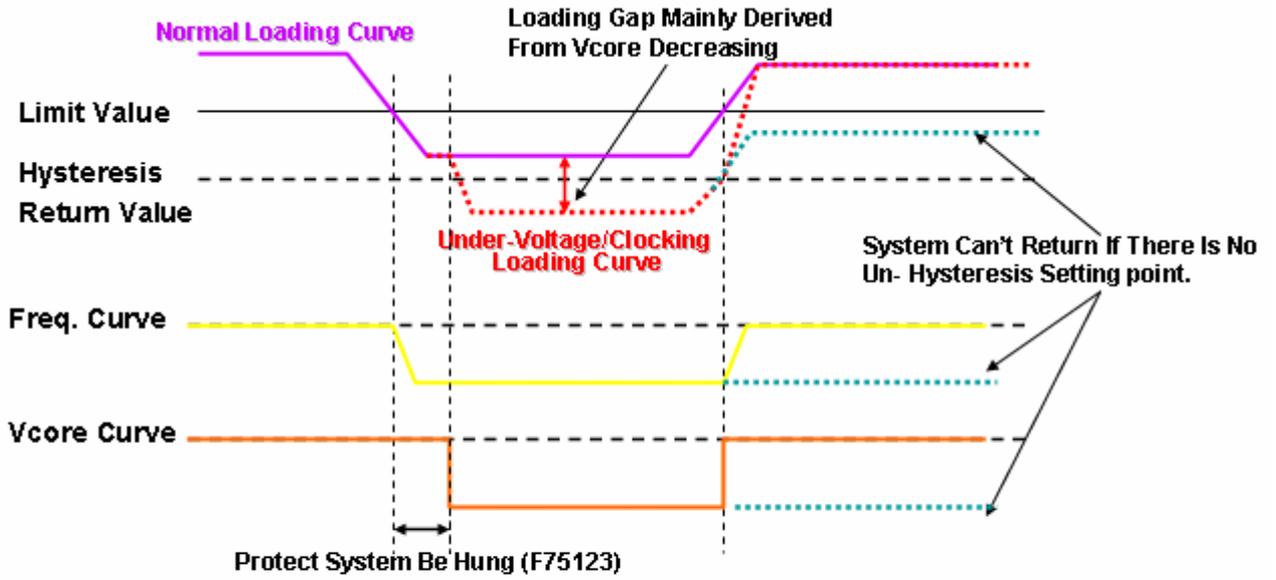
The Un-Hysteresis function shows as below sketch. This function mainly remove the loading gap from the Over-Voltage implementation. If user would like to Over-Voltage and Over-Clocking synchronous, must take care the gap effect in your system. As the sketch shows, system can't return if there is no Un-Hysteresis function. (More detail, please refer the register description).



Each Limit Step Match An Un-Hysteresis Setting Point Which Also Can Be Programmed.

F75133 Can Be Implemented with F75123 for Over-Clocking and Over-Voltage (Vcore) Simultaneously.

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F75133 Can Be Implemented with F75123 for Under-Clocking and Under-Voltage Simultaneously. Power Consumption Can Be Saved More and System Will Be More Stable.

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8. Register Description

8.1 Control Register — Index 00h

Bit	Name	R/W	Default	Description
7	INIT	R/W	0	Soft ware reset device, if write 1 to this bit will reset this IC and then it will auto clear to 0.
6-5	Reserved.	R/W	0	Reserved
4	CLK_SEL	R/W	0	Set to 1 the output clock frequency will select to 50HZ, the default frequency is 100HZ. User can select clock duty cycle from CR06 bit 7~4
3-1	MONITOR_TIME	R/W	100	Set these bits to decide how many time to be one monitor cycle, and after one cycle finish, it will auto update average duty to PWM duty register (CR02). 000: (About 8.858 Sec) 001: (About 4.429 Sec) 010: (About 2.215 Sec) 011: (About 1.107 Sec) 100: (About 0.554 Sec) (Default value) 101: (About 0.277 Sec) 110: (About 0.138 Sec) 111: (About 0.069 Sec)
0	POWER_DOWN	R/W	0	Set to 1 to stop PWM duty monitor and power down this IC.

8.2 Pins Control Register — Index 01h

Bit	Name	R/W	Default	Description
7	INV_TURBO	R/W	0	If set this bit to 1, invert TURBO# pin output polarity.
6	INV_FAULT	R/W	0	If set this bit to 1, invert FAULT# pin output polarity.
5	INV_PME	R/W	0	If set this bit to 1, invert PME# pin output polarity.

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4	TURBO_MODE	R/W	0	<p>TURBO_MODE: If set bit4 to 1, will be in TURBO_MODE.</p> <p>PWM_DUTY(CR02, 08) > LIMIT3_VAL(CR03, 0A):</p> <p>DIS_LIMIT3_VAL set to 0 (CR0D bit1): PME#, TURBO# → 2'b00.</p> <p>DIS_LIMIT3_VAL set to 1 (CR0D bit1): PME#, TURBO# → 2'b01.</p> <p>LIMIT3_VAL (CR03, 0A) > PWM_DUTY(CR02, 08) > LIMIT2_VAL (CR04, 0B):</p> <p>PME#, TURBO# → 2'b01.</p> <p>LIMIT2_VAL (CR04, 0B) > PWM_DUTY(CR02, 08) > LIMIT1_VAL (CR05, 0B):</p> <p>PME#, TURBO# → 2'b10.</p> <p>LIMIT1_VAL (CR05, 0B) > PWM_DUTY(CR02, 08) > LIMIT0_VAL (CR09, 0A)</p> <p>PME#, TURBO# → 2'b11.</p> <p>LIMIT0_VAL (CR09, 0A) > PWM_DUTY (CR02, 08)</p> <p>DIS_LIMIT0_VAL set to 0 (CR0D bit0): PME#, TURBO# → 2'b00.</p> <p>DIS_LIMIT0_VAL set to 1 (CR0D bit0): PME#, TURBO# → 2'b11.</p>
3	TURBO_SEL	R/W	0	<p>If TURBO_SEL (bit3) set to 0 and TURBO_MODE (bit4) is 0, will be in “Under LIMIT1 Mode”.</p> <ol style="list-style-type: none"> When PWM_DUTY (CR02, CR08) value is under then LIMIT1_VAL (CR05, CR0B), the TURBO# pin will be asserted The PME# pin will be asserted when PWM_DUTY (CR02, CR08) value over (under) or return to normal value (as the figure), and the PME_STS (CR06 bit 3) bit will be set to 1, users need write 1 to PME_STS (CR06 bit 3) to clear it, else PME# will not be asserted again. <p>If TURBO_SEL (bit3) set to 1 and TURBO_MODE (bit4) is 0, will be in “Over LIMIT2 Mode”.</p> <ol style="list-style-type: none"> When PWM_DUTY (CR02, CR08) value is over then LIMIT2 (CR04, CR0B), the TURBO# pin will be asserted The PME# pin will be asserted when PWM_DUTY (CR02, CR08) value over (under) or return to normal value, and the PME_STS (CR06 bit 3) bit will be set to 1, users need write 1 to PME_STS (CR06 bit 3) to clear it, else PME# will not be asserted again.

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				<p>HYS_MODE1 enable(CR0D bit3 set to 1)</p> <p>If TURBO_SEL (bit3) set to 0 and TURBO_MODE (bit4) is 0, will be in “Over Clocking Mode”.</p> <p>1. When PWM_DUTY (CR02, CR08) value is over then LIMIT1_VAL (CR05, CR0B), the TURBO# pin will be asserted after PWM_DUTY (CR02, CR08) value is under LIMIT2_VAL(CR04, CR0B), or LIMIT1_VAL (CR05, CR0B), the TURBO# pin will be return.</p> <p>If TURBO_SEL (bit3) set to 1 and TURBO_MODE(bit4) is 0, will be in “Power save Mode”.</p> <p>1. When PWM_DUTY (CR02, CR08) value is under then LIMIT2_VAL (CR04, CR0B), the TURBO# pin will be asserted after PWM_DUTY (CR02, CR08) value is over then LIMIT1_VAL(CR05, CR0B), or LIMIT2_VAL (CR04, CR0B), the TURBO# pin will be return.</p>
2	EN_TURBO	R/W	0	Set to 1 to enable TURBO# function.
1	EN_FAULT	R/W	1	Set to 1 to enable FAULT# function, when PWM_DUTY (CR02, CR08) value is over then LIMIT3_VAL (CR03, CR0A), the FAULT# pin will be asserted (low active) in TURBO_MODE .
0	EN_PME	R/W	0	Set to 1 to enable PME# function, when PWM_DUTY (CR02, CR08) value over or under then any LIMIT_VAL value, the PME# pin will be asserted.

8.3 PWM Duty Count Register (MSB) — Index 02h

Bit	Name	R/W	Default	Description
7-0	PWM_DUTY[15:8]	R	00h	Average duty cycle count. Divide this count value to 256 is duty cycle.

8.4 LIMIT3 Value Register (MSB)— Index 03h

Bit	Name	R/W	Default	Description
7-0	LIMIT3_VAL[11:4]	R/W	-	Duty cycle count LIMIT3, if average duty count over this value will assert FAULT function. The default value of this is Strapping by TURBO# pin : Pull-down 4.7K: default value F3h (95%) and now I2C ID is 66h. Pull-up 100k: default value E6h (90%) and now I2C ID is 68h. Pull-down 100K: default value CCh (80%) and now I2C ID is 6Ah. Pull-up 4.7k: default value B3h (70%) and now I2C ID is 6Ch.

8.5 LIMIT2 Value Register (MSB)— Index 04h

Bit	Name	R/W	Default	Description
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7-0	LIMIT2_VAL[11:4]	R/W	3Ch	Duty cycle count LIMIT2, if average duty count over this value and TURBO_SEL is 1, then it will assert TURBO# pin.
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8.6 LIMIT1 Value Register (MSB)— Index 05h

Bit	Name	R/W	Default	Description
7-0	LIMIT1_VAL[11:4]	R/W	0Fh	Duty cycle count LIMIT1, if average duty count under this value and TURBO_SEL is 0, then it will assert TURBO# pin.

8.7 Event Status Register — Index 06h

Bit	Name	R/W	Default	Description
7-4	DUTY_SEL	R/W	4'h4	When CR00H bit4 set to 0, the pin TURBO# will output 100Hz clock, and users can use these registers to program the output duty cycle, (default is 50%) For example: 0: 10% duty cycle. 1: 20% duty cycle. 2: 30% duty cycle. 8: 90% duty cycle. 9: 100% duty cycle. (always high) 10~15: reserved.
3	PME_STS	R/W	0	When Duty cycle value (PWM_DUTY) over (under) or return to normal value, it will trigger PME# and set this bit to 1. Users need write 1 to clear it , else PME# will not be asserted again.
2	OVER_UNDER_FAULT	R	0	1. PWM duty cycle value (PWM_DUTY) over LIMIT3 count (CR03, CR0A) and DIS_LIMIT3 set to 0(CR0D), this bit will set to 1, else will auto return to 0. 2. PWM duty cycle value (PWM_DUTY) under LIMIT0 count (CR09, CR0A) and DIS_LIMIT0 set to 0(CR0D), this bit will set to 1, else will auto return to 0
1	OVER_HIGH	R	0	PWM duty cycle value (PWM_DUTY) over LIMIT2 count (CR04, CR0B), this bit will set to 1, else will auto return to 0.
0	UNDER_LOW	R	0	PWM duty cycle value (PWM_DUTY) under LIMIT1 count (CR05, CR0B), this bit will set to 1, else will auto return to 0.

8.8 I2C_ADDRESS Register — Index 07h

Bit	Name	R/W	Default	Description
7-0	I2C_ADDR	R/W	X	Pull-down 4.7K: default I2C ID is 66h. In this strapping value the PWM input will be inverted. Pull-up 100K: default I2C ID is 68h. Pull-down 100k: default I2C ID is 6Ah. In this strapping value the PWM input will be inverted. Pull-up 4.7k: default I2C ID is 6Ch.

8.9 PWM Duty Count Register(LSB) — Index 08h

Bit	Name	R/W	Default	Description
7-0	PWM_DUTY [7:0]	R	X	Average duty cycle count bit 7~0. Divide the PWM_DUTY [15:0] to 65536 is mean present duty cycle.

8.10 LIMIT0 Value Register (MSB)— Index 09h

Bit	Name	R/W	Default	Description
7-0	LIMIT0_VAL[11:4]	R/W	0Dh	Duty cycle count LIMIT0, if average duty count under this value will assert FAULT function. The default value of this is 8'h0D.

8.11 LIMIT0 and LIMIT3 Value Register (LSB) — Index 0Ah

Bit	Name	R/W	Default	Description
7-4	LIMIT3_VAL[3:0]	RO	0h	Duty cycle count LIMIT3, if average duty count over this value will assert FAULT function. The default value of this is Strapping by TURBO# pin:
3-0	LIMIT0_VAL[3:0]	R/W	0h	Duty cycle count LIMIT0, if average duty count over this value will assert FAULT function. The default value of this is Strapping by TURBO# pin :

8.12 LIMIT1 and LIMIT2 Value Register(LSB) — Index 0Bh

Bit	Name	R/W	Default	Description
7-4	LIMIT2_VAL[3:0]	R/W	0h	Duty cycle count LIMIT2, if average duty count over this value and TURBO_SEL is 1, then it will assert TURBO# pin.
3-0	LIMIT1_VAL[3:0]	R/W	0h	Duty cycle count LIMIT1, if average duty count under this value and TURBO_SEL is 0, then it will assert TURBO# pin.

8.13 Pin Mode Select Register — Index 0Ch

Bit	Name	R/W	Default	Description
7	PME_LEDMODE	R/W	0	If PWM duty value over (under) LIMIT3(LIMIT0), and this bit set to 1 then the PME# pin will output 1HZ clock, else it will be the function that select in PME_MODE_SEL (CR0Cbit4-2).
6	Reserved	R/W	0	Reserved.
5	Reserved	R/W	0	Reserved.

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4-2	PME_PIN_SEL	R/W	0h	These registers use to select PME# pin clock output function. 000: PME# pin will use as normal function. 001: PME# pin will output 100HZ or 50HZ clock (select by CR00 bit4) 010: When PWM duty over LIMIT 2, PME# pin will output 100HZ or 50HZ clock. 011: When PWM duty under Limit1, PME# pin will output 100HZ or 50HZ clock 100~111: When PWM duty over or under LIMIT3/0, PME# pin will output 1HZ clock
1-0	TURBO_PIN_SEL	R/W	0h	These registers use to select Turbo# pin clock output function. 00: Turbo pin will use as normal function. 01: Turbo pin will output 100HZ or 50HZ clock (select by CR00 bit4) 10: When PWM duty over LIMIT2, Turbo pin will output 100HZ or 50HZ clock. 11: When PWM duty under LIMIT1, Turbo pin will output 100HZ or 50HZ clock

8.14 Event and mode control Register — Index 0Dh

Bit	Name	R/W	Default	Description
7-6	Reserved	R0	0	Always return 0.
5	FAULT_DIS_TURBO	R/W	0	When this bit enable, pin Fault # will become input mode, and input low will disable turbo output.
4	FAULT_LED	R/W	0	Set to 1 fault function will alert by LED mode.
3	HYS_MODE_EN	R/W	0	Hysteresis mode
2	Reserved	R/W	0	Reserved. (Do Not change the value)
1	DIS_LIMIT3_VAL	R/W	0	Set this bit to 1 to disable over LIMIT3 compare.
0	DIS_LIMIT0_VAL	R/W	1	Set this bit to 1 to disable under LIMIT0 compare.

8.15 PME# Event Control Register — Index 0Eh

Bit	Name	R/W	Default	Description
7-4	Reserved	R0	0	Always return 0.
3	LIMIT3_PME_EN	R/W	1	Enable over/under LIMIT3 event to trigger PME
2	LIMIT2_PME_EN	R/W	1	Enable over/under LIMIT2 event to trigger PME
1	LIMIT1_PME_EN	R/W	1	Enable over/under LIMIT1 event to trigger PME
0	LIMIT0_PME_EN	R/W	1	Enable over/under LIMIT0 event to trigger PME

8.16 Watchdog timer Control Register — Index 0Fh

Bit	Name	R/W	Default	Description
7-6	Reserved	R0	0	Always return 0.
5	TIMEOUT_EN	R/W	1	Timeout function enables.
4-0	TIMOUT_CNT_VAL	R/W	1Fh	When HYS_MODE and PWM duty between LIMIT value and return value more then timeout count value times, it will disable turbo output.

8.17 LIMIT3 Return Value Register (MSB)— Index 13h

Bit	Name	R/W	Default	Description
7-0	RET_VAL3[11:4]	R/W	Xh	When PWM duty over/under this value and HYS_MODE2 (CR0D bit3) is enabled turbo code[2:0] will return to last value.

8.18 LIMIT2 Return Value Register (MSB)— Index 14h

Bit	Name	R/W	Default	Description
7-0	RET_VAL2 [11:4]	R/W	Xh	When PWM duty over/under this value and HYS_MODE2 (CR0D bit3) is enabled turbo code[2:0] will return to last value

8.19 LIMIT1 Return Value Register (MSB)— Index 15h

Bit	Name	R/W	Default	Description
7-0	RET_VAL1 [11:4]	R/W	Xh	When PWM duty over/under this value and HYS_MODE2 (CR0D bit3) is enabled turbo code[2:0] will return to last value

8.20 LIMIT0 Return Value Register (MSB)— Index 19h

Bit	Name	R/W	Default	Description
7-0	RET_VAL0[11:4]	R/W	Xh	When PWM duty over/under this value and HYS_MODE2 (CR0D bit3) is enabled turbo code[2:0] will return to last value

8.21 LIMIT3 and LIMIT0 Return Value Register (LSB) — Index 1Ah

Bit	Name	R/W	Default	Description
7-4	RET_VAL3[3:0]	RO	xxx0b	When PWM duty over/under this value and HYS_MODE2 (CR0D bit3) is enabled turbo code[2:0] will return to last value
3-0	RET_VAL0[3:0]	R/W	xxx0b	When PWM duty over/under this value and HYS_MODE2 (CR0D bit3) is enabled turbo code[2:0] will return to last value

8.22 LIMIT2 and LIMIT1 Return Value Register(LSB) — Index 1Bh

Bit	Name	R/W	Default	Description
7-4	RET_VAL2[3:0]	R/W	xxx0b	When PWM duty over/under this value and HYS_MODE2 (CR0D bit3) is enabled turbo code[2:0] will return to last value
3-0	RET_VAL1[3:0]	R/W	xxx0b	When PWM duty over/under this value and HYS_MODE2 (CR0D bit3) is enabled turbo code[2:0] will return to last value

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8.23 Turbo code 0-1 Register(LSB) — Index 1Ch

Bit	Name	R/W	Default	Description
7	Reserved	RO	0	Always return 0
6-4	CODE1	R/W	X	Turbo code1[2:0] when PWM duty over LIMIT 0, Turbo code value will output from pin {FAULT#, PME#, TURBO#}
3	Reserved	RO	0	Always return 0
2-0	CODE0	R/W	X	Turbo code0[2:0] when PWM duty under LIMIT 0, Turbo code value will output from pin {FAULT#, PME#, TURBO#}

8.24 Turbo code 2-3 Register(LSB) — Index 1Dh

Bit	Name	R/W	Default	Description
7	Reserved	RO	0	Always return 0
6-4	CODE3	R/W	X	Turbo code3[2:0] when PWM duty over LIMIT 2, Turbo code value will output from pin {FAULT#, PME#, TURBO#}
3	Reserved	RO	0	Always return 0
2-0	CODE2	R/W	X	Turbo code2[2:0] when PWM duty over LIMIT 1, Turbo code value will output from pin {FAULT#, PME#, TURBO#}

8.25 Turbo code 4 and Standby code Register(LSB) — Index 1Eh

Bit	Name	R/W	Default	Description
7	Reserved	RO	0	Always return 0
6-4	STANDBY_CODE	R/W	X	Standby turbo code[2:0] when watchdog timer event happen or pin FAULT# input low (when FAULT_DIS_TURBO enable CR0D bit5) the output Turbo code will replace by this code.
3	Reserved	RO	0	Always return 0
2-0	CODE4	R/W	X	Turbo code4[2:0] when PWM duty over LIMIT 3. Turbo code value will output from pin {FAULT#, PME#, TURBO#}

8.26 Chip ID Register (I)— Index 5Ah

Bit	Name	R/W	Default	Description
7-0	CHIP_ID1	R	04h	Chip ID

8.27 Chip ID Register(II)— Index 5Bh

Bit	Name	R/W	Default	Description
7-0	CHIP_ID2	R	02h	Chip ID

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8.28 VENDOR ID Register(I)— Index 5Dh

Bit	Name	R/W	Default	Description
7-0	VENDOR_ID1	R	19h	19h for Fintek

8.29 VENDOR ID Register(II)— Index 5Eh

Bit	Name	R/W	Default	Description
7-0	VENDOR_ID2	R	34h	34h for Fintek

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9. DC Characteristics

(Ta = 70° C, VDD = 3.3V, VSS = 0V)

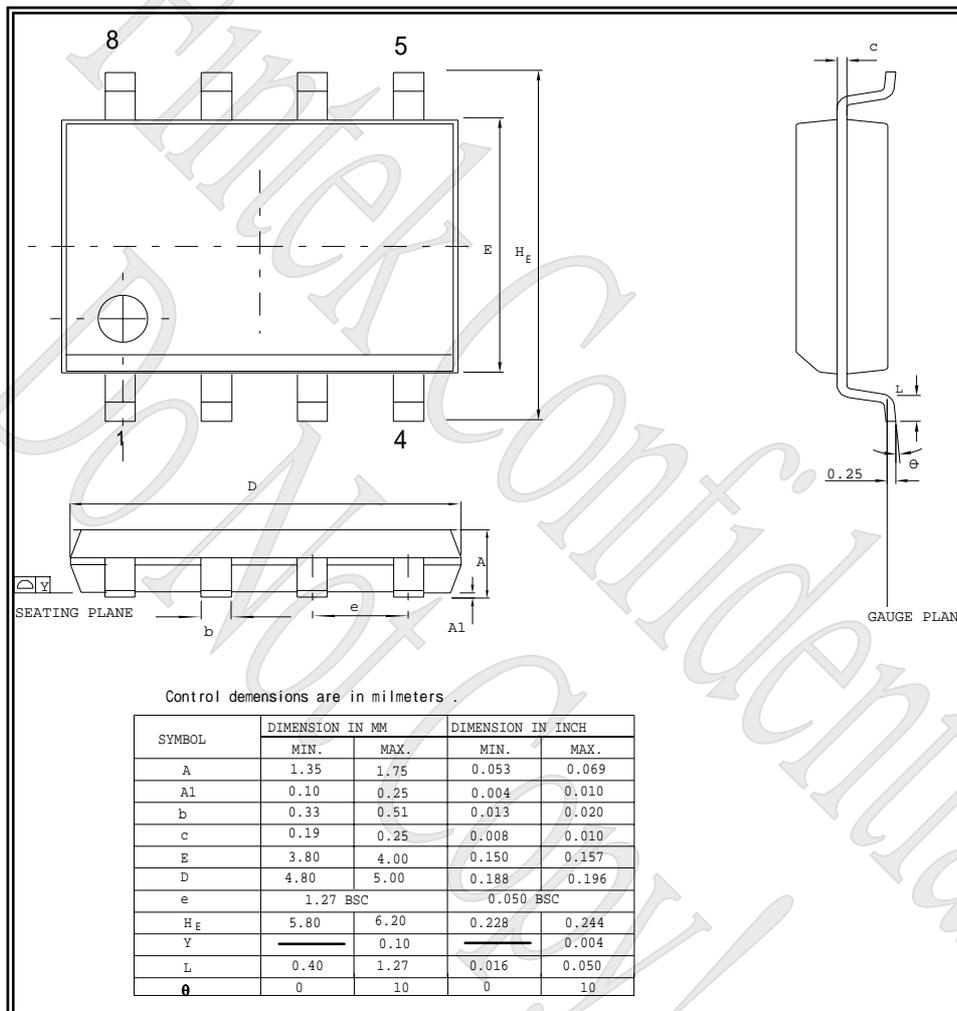
PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/OD_{12st} - TTL level bi-directional pin, with Schmitt trigger, can select to OD by register, with 12 mA source-sink capability						
Input Low Threshold Voltage	Vt-			0.8	V	VDD = 3.3 V
Input High Threshold Voltage	Vt+	2.0			V	VDD = 3.3 V
Output Low Current	IOL	12			mA	VOL = 0.4 V
Input High Leakage	ILIH			1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
O₁₂ - Output pin with 12 mA source-sink capability						
Output High Current	IOH			-20	mA	VOL = 2.4 V
Output Low Current	IOL	20			mA	VOL = 0.4 V
INs_t - TTL level , with Schmitt trigger input pin						
Input Low Threshold Voltage	Vt-			0.8	V	VDD = 3.3 V
Input High Threshold Voltage	Vt+	2.0			V	VDD = 3.3 V
Input High Leakage	ILIH			1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
OD₁₂ – Open drain output pin with 12 mA source-sink capability.						
Output Low Current	IOL	12			mA	VOL = 0.4 V

10. Ordering Information

Part Number	Package Type	Production Flow
F75133S	8-SOP Green Package	Commercial, 0°C to +70°C

11. Package Dimensions

8pin-SOP (150 mil)



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12. Application Circuit

