

# 3803 Group (Spec.H QzROM version)

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

REJ03B0166-0110

Rev.1.10

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## DESCRIPTION

The 3803 group (Spec.H QzROM version) is the 8-bit microcomputer based on the 740 family core technology. The 3803 group (Spec.H QzROM version) is designed for household products, office automation equipment, and controlling systems that require analog signal processing, including the serial interface functions, 8/16-bit timer, A/D converter and D/A converter.

## FEATURES

- Basic machine-language instructions ..... 71
- Minimum instruction execution time ..... 0.24  $\mu$ s  
(at 16.8 MHz oscillation frequency)
- Memory size
  - QzROM ..... 16 K to 48 K bytes
  - RAM ..... 2048 bytes
- Programmable input/output ports ..... 56
- Software pull-up resistors ..... Built-in
- Interrupts ..... 21 sources, 16 vectors  
(external 8, internal 12, software 1)
- Timers ..... 16-bit  $\times$  1  
8-bit  $\times$  4  
(with 8-bit prescaler)
- Serial interface ..... 8-bit  $\times$  2 (UART or Clock-synchronized)  
8-bit  $\times$  1 (Clock-synchronized)
- PWM ..... 8-bit  $\times$  1 (with 8-bit prescaler)
- A/D converter ..... 10-bit  $\times$  16 channels  
(8-bit reading enabled)
- D/A converter ..... 8-bit  $\times$  2 channels
- Watchdog timer ..... 16-bit  $\times$  1
- LED direct drive port ..... 8
- Clock generating circuit ..... Built-in 2 circuits  
(connect to external ceramic resonator or quartz-crystal oscillator)

- Power source voltage
  - [In high-speed mode]
    - At 16.8 MHz oscillation frequency ..... 4.5 to 5.5 V
    - At 12.5 MHz oscillation frequency ..... 4.0 to 5.5 V
    - At 8.4 MHz oscillation frequency ..... 2.7 to 5.5 V
    - At 4.2 MHz oscillation frequency ..... 2.2 to 5.5 V
    - At 2.1 MHz oscillation frequency ..... 2.0 to 5.5 V
  - [In middle-speed mode]
    - At 16.8 MHz oscillation frequency ..... 4.5 to 5.5 V
    - At 12.5 MHz oscillation frequency ..... 2.7 to 5.5 V
    - At 8.4 MHz oscillation frequency ..... 2.2 to 5.5 V
    - At 6.3 MHz oscillation frequency ..... 1.8 to 5.5 V
  - [In low-speed mode]
    - At 32 kHz oscillation frequency ..... 1.8 to 5.5 V
- Power dissipation
  - In high-speed mode ..... 40 mW (typ.)  
(at 16.8 MHz oscillation frequency, at 5 V power source voltage)
  - In low-speed mode ..... 45  $\mu$ W (typ.)  
(at 32 kHz oscillation frequency, at 3 V power source voltage)
- Operating temperature range ..... -20 to 85  $^{\circ}$ C
- Packages
  - SP ..... PRDP0064BA-A (64-pin 750 mil SDIP)
  - HP ..... PLQP0064KB-A (64-pin 10  $\times$  10 mm LQFP)
  - KP ..... PLQP0064GA-A (64-pin 14  $\times$  14 mm LQFP)

## APPLICATION

Household products, Consumer electronics, etc.

## 3803 Group (Spec.H QzROM version)

Currently support products are listed below.

Table 1 Support products

Product name	QzROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M38039G4H-XXXHP	16384	2048	PLQP0064KB-A	QzROM version (Programmed shipment) <sup>(1)</sup>
M38039G4H-XXXKP	(16254)		PLQP0064GA-A	
M38039G6H-XXXHP	24576		PLQP0064KB-A	
M38039G6H-XXXKP	(24446)		PLQP0064GA-A	
M38039G8H-XXXHP	32768		PLQP0064KB-A	
M38039G8H-XXXKP	(32638)		PLQP0064GA-A	
M38039GCH-XXXHP	49152		PLQP0064KB-A	
M38039GCH-XXXKP	(49022)		PLQP0064GA-A	
M38039G4HSP	16384		PRDP0064BA-A	QzROM version (blank) <sup>(2)</sup>
M38039G4HHP	(16254)		PLQP0064KB-A	
M38039G4HHP			PLQP0064GA-A	
M38039G6HSP	24576		PRDP0064BA-A	
M38039G6HHP	(24446)		PLQP0064KB-A	
M38039G6HHP			PLQP0064GA-A	
M38039G8HSP	32768		PRDP0064BA-A	
M38039G8HHP	(32638)		PLQP0064KB-A	
M38039G8HHP			PLQP0064GA-A	
M38039GCHSP	49152		PRDP0064BA-A	
M38039GCHHP	(49022)		PLQP0064KB-A	
M38039GCHHP			PLQP0064GA-A	

## NOTES:

1. This means a shipment of which User ROM has been programmed.
2. The user ROM area of a blank product is blank.

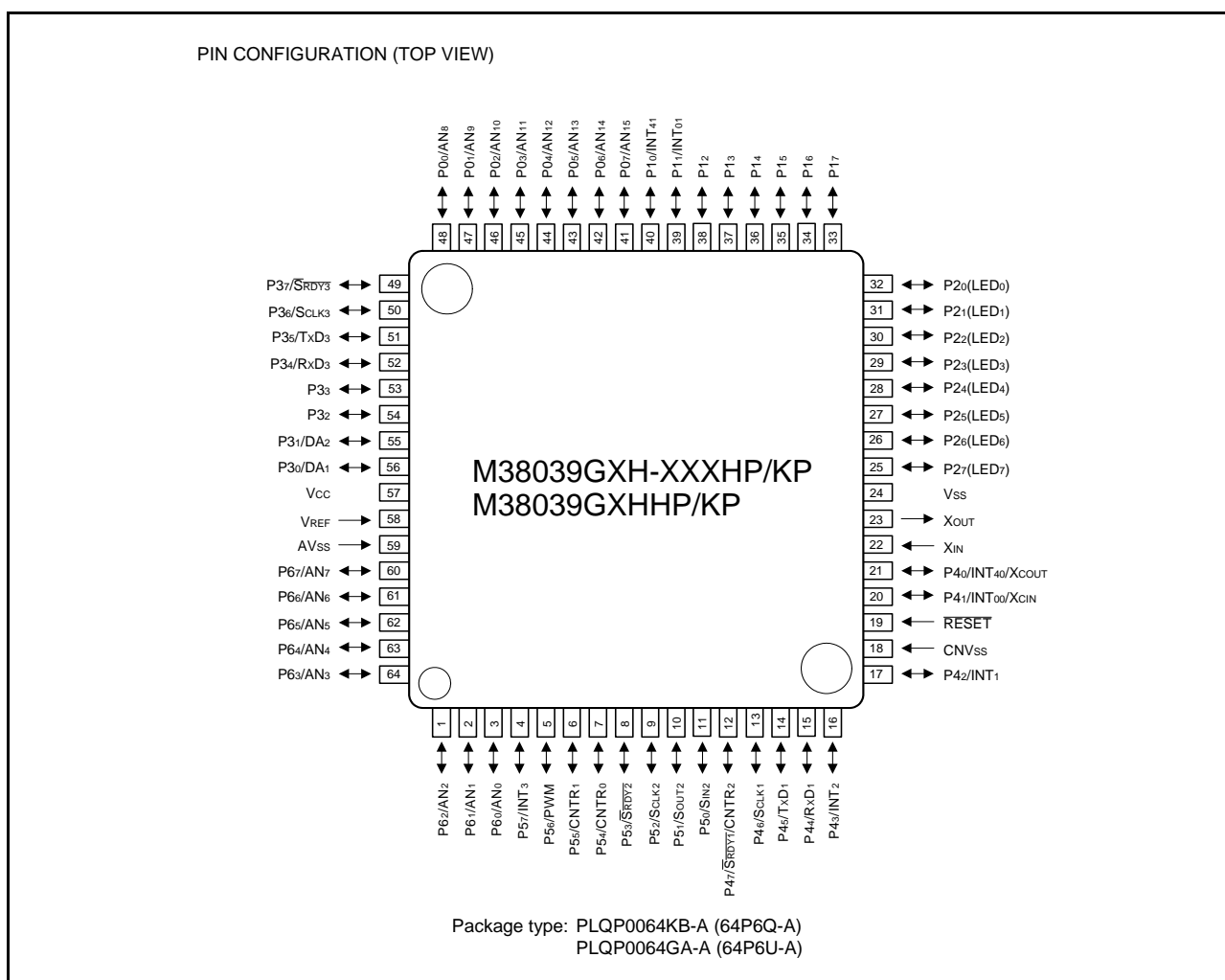


Fig 1. 3803 group (Spec.H QzROM version) pin configuration (PLQP0064KB-A/PLQP0064GA-A)

Table 2 List of package (Spec.H QzROM version) (PLQP0064KB-A/PLQP0064GA-A)

Package	Product name	QzROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Remarks
PLQP0064KB-A	M38039G4H-XXXHP	16384 (16254)	2048	QzROM version (Programmed shipment) <sup>(1)</sup>
	M38039G4HHP			QzROM version (blank) <sup>(2)</sup>
	M38039G6H-XXXHP	24576 (24446)		QzROM version (Programmed shipment) <sup>(1)</sup>
	M38039G6HHP			QzROM version (blank) <sup>(2)</sup>
	M38039G8H-XXXHP	32768 (32638)		QzROM version (Programmed shipment) <sup>(1)</sup>
	M38039G8HHP			QzROM version (blank) <sup>(2)</sup>
	M38039GCH-XXXHP	49152 (49022)		QzROM version (Programmed shipment) <sup>(1)</sup>
	M38039GCHHP			QzROM version (blank) <sup>(2)</sup>
PLQP0064GA-A	M38039G4H-XXXKP	16384 (16254)	2048	QzROM version (Programmed shipment) <sup>(1)</sup>
	M38039G4HHP			QzROM version (blank) <sup>(2)</sup>
	M38039G6H-XXXKP	24576 (24446)		QzROM version (Programmed shipment) <sup>(1)</sup>
	M38039G6HHP			QzROM version (blank) <sup>(2)</sup>
	M38039G8H-XXXKP	32768 (32638)		QzROM version (Programmed shipment) <sup>(1)</sup>
	M38039G8HHP			QzROM version (blank) <sup>(2)</sup>
	M38039GCH-XXXKP	49152 (49022)		QzROM version (Programmed shipment) <sup>(1)</sup>
	M38039GCHKP			QzROM version (blank) <sup>(2)</sup>

NOTES:

1. This means a shipment of which User ROM has been programmed.
2. The user ROM area of a blank product is blank.

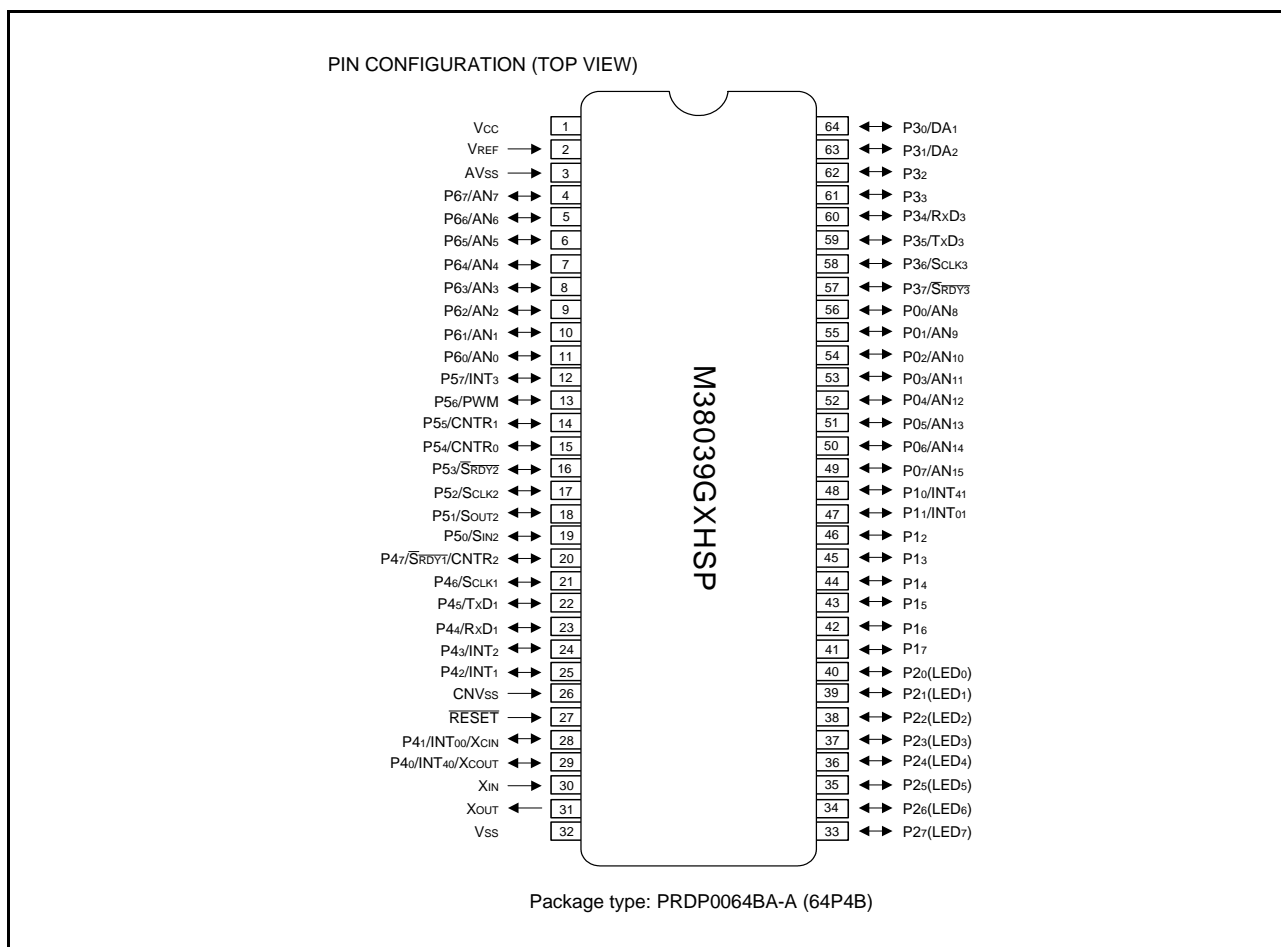


Fig 2. 3803 group (Spec.H QzROM version) pin configuration (PRDP0064BA-A)

Table 3 List of package (Spec.H QzROM version) (PRDP0064BA-A)

Package	Product name	QzROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Remarks
PRDP0064BA-A	M38039G4HSP	16384 (16254)	2048	QzROM version (blank) <sup>(1)</sup>
	M38039G6HSP	24576 (24446)		
	M38039G8HSP	32768 (32638)		
	M38039GCHSP	49152 (49022)		

NOTES:

1. The user ROM area of a blank product is blank.

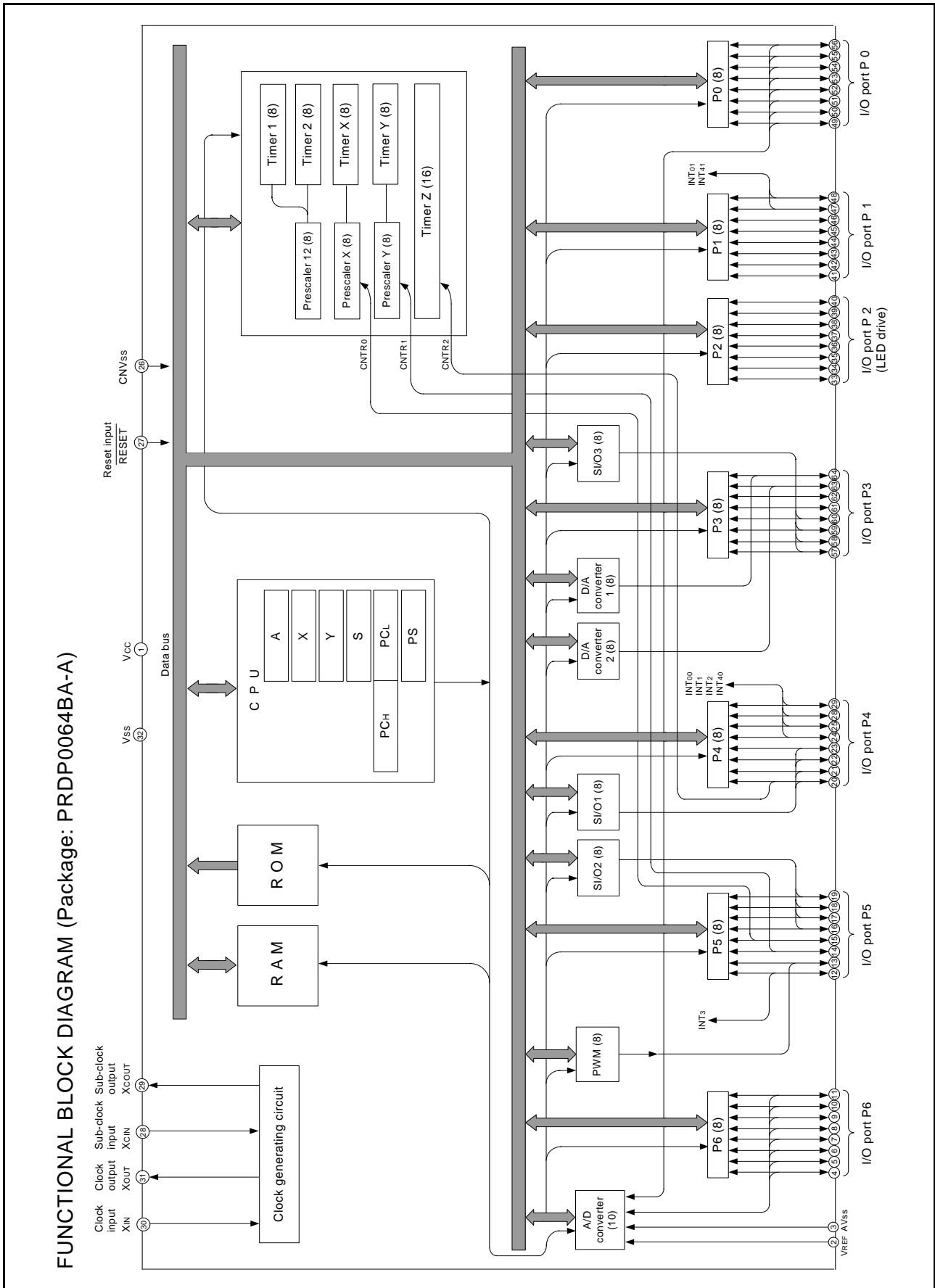


Fig 3. Functional block diagram

**PIN DESCRIPTION**

Table 4 Pin description

Pin	Name	Functions	Function except a port function
Vcc, Vss	Power source	<ul style="list-style-type: none"> <li>Apply voltage of 1.8 V – 5.5 V to Vcc, and 0 V to Vss.</li> </ul>	
CNVss	CNVss input	<ul style="list-style-type: none"> <li>This pin controls the operation mode of the chip and is shared with the VPP pin which is the power source input pin for programming the built-in QzROM.</li> <li>Normally connected to Vss.</li> </ul>	
VREF	Reference voltage	<ul style="list-style-type: none"> <li>Reference voltage input pin for A/D and D/A converters.</li> </ul>	
AVss	Analog power source	<ul style="list-style-type: none"> <li>Analog power source input pin for A/D and D/A converters.</li> <li>Connect to Vss.</li> </ul>	
RESET	Reset input	<ul style="list-style-type: none"> <li>Reset input pin for active “L”.</li> </ul>	
XIN	Clock input	<ul style="list-style-type: none"> <li>Input and output pins for the clock generating circuit.</li> <li>Connect a ceramic resonator or quartz-crystal oscillator between the XIN and XOUT pins to set the oscillation frequency.</li> <li>When an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open.</li> </ul>	
XOUT	Clock output		
P00/AN8– P07/AN15	I/O port P0	<ul style="list-style-type: none"> <li>8-bit CMOS I/O port.</li> <li>I/O direction register allows each pin to be individually programmed as either input or output.</li> <li>CMOS compatible input level.</li> <li>CMOS 3-state output structure.</li> <li>Pull-up control is enabled in a bit unit.</li> <li>P20 – P27 (8 bits) are enabled to output large current for LED drive.</li> </ul>	<ul style="list-style-type: none"> <li>A/D converter input pin</li> </ul>
P10/INT41 P11/INT01	I/O port P1		<ul style="list-style-type: none"> <li>Interrupt input pin</li> </ul>
P12–P17			
P20–P27	I/O port P2		
P30/DA1 P31/DA2	I/O port P3	<ul style="list-style-type: none"> <li>8-bit CMOS I/O port.</li> <li>I/O direction register allows each pin to be individually programmed as either input or output.</li> <li>CMOS compatible input level.</li> <li>P30, P31, P34 – P37 are CMOS 3-state output structure.</li> <li>P32, P33 are N-channel open-drain output structure.</li> <li>Pull-up control of P30, P31, P34 – P37 is enabled in a bit unit.</li> </ul>	<ul style="list-style-type: none"> <li>D/A converter input pin</li> </ul>
P32, P33			
P34/RxD3 P35/TxD3 P36/SCLK3 P37/SRDY3			<ul style="list-style-type: none"> <li>Serial I/O3 function pin</li> </ul>
P40/INT40/XCOUT P41/INT00/XCIN	I/O port P4	<ul style="list-style-type: none"> <li>8-bit CMOS I/O port.</li> <li>I/O direction register allows each pin to be individually programmed as either input or output.</li> <li>CMOS compatible input level.</li> <li>CMOS 3-state output structure.</li> <li>Pull-up control is enabled in a bit unit.</li> </ul>	<ul style="list-style-type: none"> <li>Interrupt input pin</li> <li>Sub-clock generating I/O pin (resonator connected)</li> </ul>
P42/INT1 P43/INT2			<ul style="list-style-type: none"> <li>Interrupt input pin</li> </ul>
P44/RxD1 P45/TxD1 P46/SCLK1			<ul style="list-style-type: none"> <li>Serial I/O1 function pin</li> </ul>
P47/SRDY1/CNTR2			<ul style="list-style-type: none"> <li>Serial I/O1, timer Z function pin</li> </ul>
P50/SIN2 P51/SOUT2 P52/SCLK2 P53/SRDY2			I/O port P5
P54/CNTR0			
P55/CNTR1			
P56/PWM			
P57/INT3			
P60/AN0– P67/AN7	I/O port P6		<ul style="list-style-type: none"> <li>A/D converter input pin</li> </ul>

**PART NUMBERING**

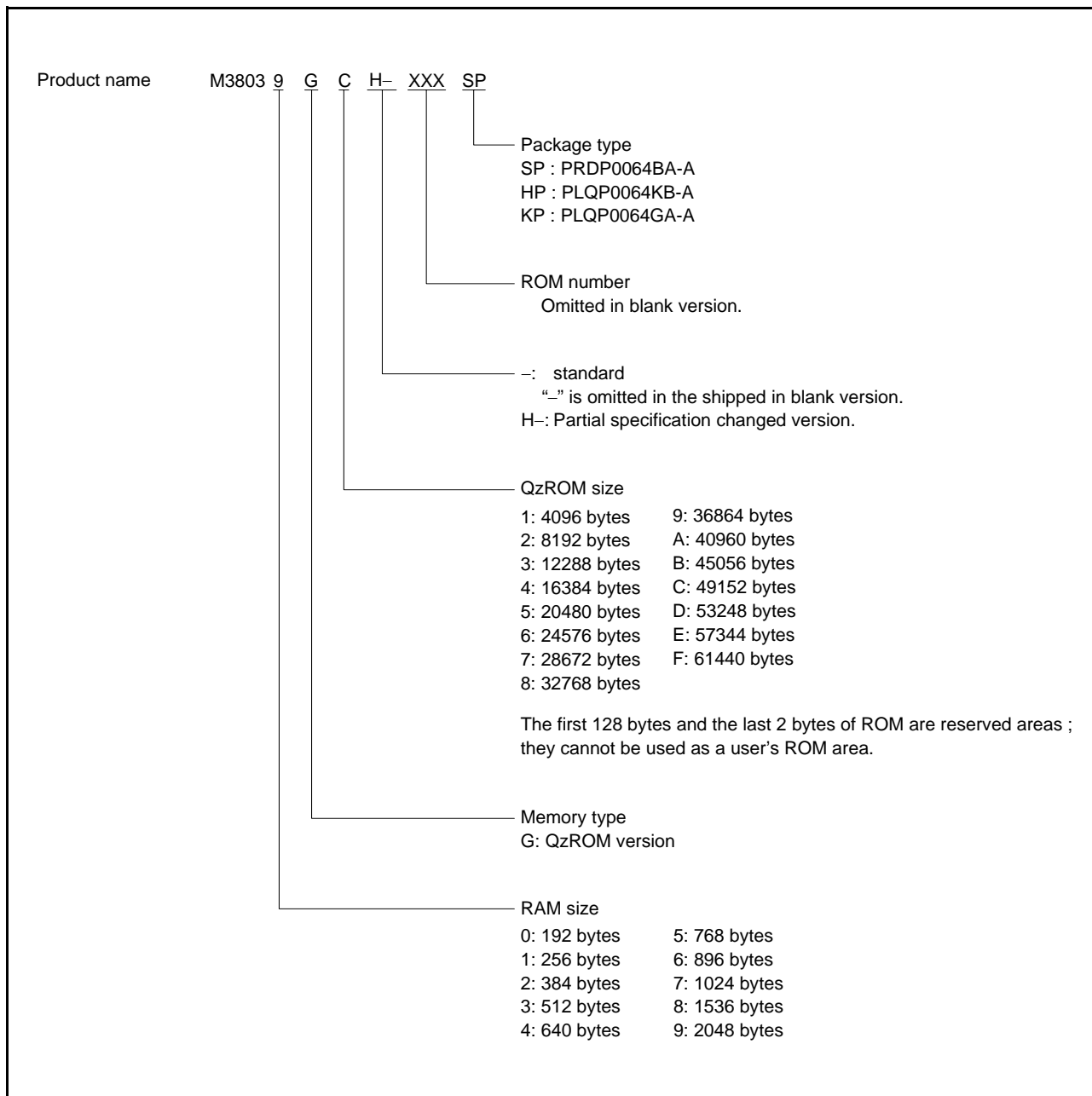


Fig 4. Part numbering

**GROUP EXPANSION**

Renesas Technology expands the 3803 group (Spec.H QzROM version) as follows.

**Memory Type**

Support for QzROM version.

**Memory Size**

- QzROM size ..... 16 K to 48 K bytes
- RAM size ..... 2048 bytes

**Packages**

- PRDP0064BA-A ..... 64-pin shrink plastic-molded DIP
- PLQP0064KB-A ..... 0.5 mm-pitch plastic molded LQFP
- PLQP0064GA-A ..... 0.8 mm-pitch plastic molded LQFP

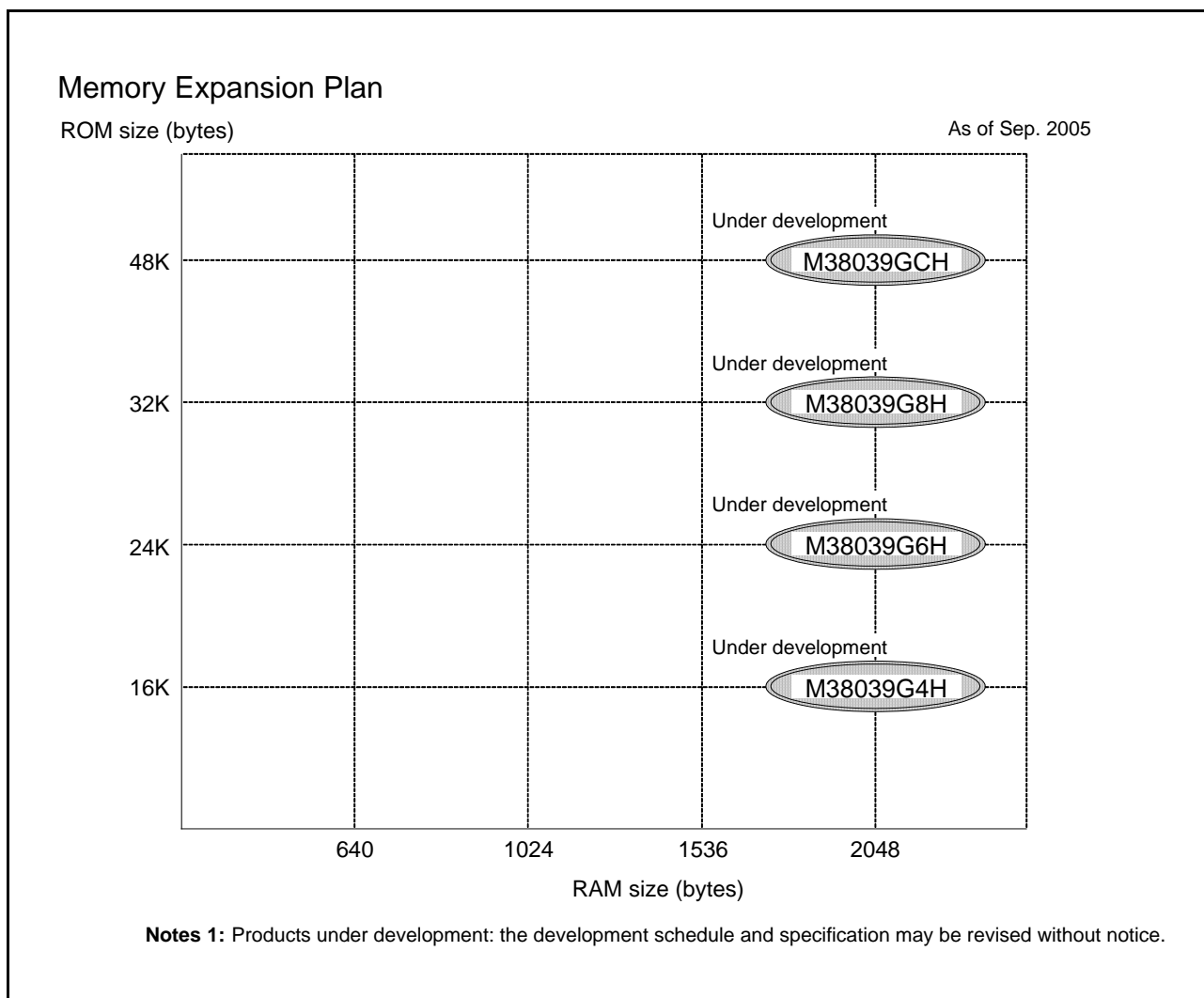


Fig 5. Memory expansion plan



**GROUP DESCRIPTION**

The QzROM version of 3803 group (Spec.H) is under development. The mask ROM version and the flash memory version are mass production. Currently support products are listed below.

Table 5 Support products (mask ROM version and flash memory version of Spec.H)

Product name	ROM/flash memory size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M38034M4H-XXXSP	16384 (16254)	640	PRDP0064BA-A (64P4B)	Mask ROM version
M38034M4H-XXXFP			PRQP0064GA-A (64P6N-A)	
M38034M4H-XXXHP			PLQP0064KB-A (64P6Q-A)	
M38034M4H-XXXKP			PLQP0064GA-A (64P6U-A)	
M38037M6H-XXXSP	24576 (24446)	1024	PRDP0064BA-A (64P4B)	
M38037M6H-XXXFP			PRQP0064GA-A (64P6N-A)	
M38037M6H-XXXHP			PLQP0064KB-A (64P6Q-A)	
M38037M6H-XXXKP			PLQP0064GA-A (64P6U-A)	
M38037M8H-XXXSP	32768 (32638)	1024	PRDP0064BA-A (64P4B)	
M38037M8H-XXXFP			PRQP0064GA-A (64P6N-A)	
M38037M8H-XXXHP			PLQP0064KB-A (64P6Q-A)	
M38037M8H-XXXKP			PLQP0064GA-A (64P6U-A)	
M38039MCH-XXXSP	49152 (49022)	2048	PRDP0064BA-A (64P4B)	
M38039MCH-XXXFP			PRQP0064GA-A (64P6N-A)	
M38039MCH-XXXHP			PLQP0064KB-A (64P6Q-A)	
M38039MCH-XXXKP			PLQP0064GA-A (64P6U-A)	
M38039MFH-XXXSP	61440 (61310)	2048	PRDP0064BA-A (64P4B)	
M38039MFH-XXXFP			PRQP0064GA-A (64P6N-A)	
M38039MFH-XXXHP			PLQP0064KB-A (64P6Q-A)	
M38039MFH-XXXKP			PLQP0064GA-A (64P6U-A)	
M38039MFH-XXXWG			PTLG0064JA-A (64F0G)	
M38039FFHSP	61440	2048	PRDP0064BA-A (64P4B)	Flash memory version (Vcc=2.7–5.5V)
M38039FFHFP			PRQP0064GA-A (64P6N-A)	
M38039FFHHP			PLQP0064KB-A (64P6Q-A)	
M38039FFHHP			PLQP0064GA-A (64P6U-A)	Flash memory version (Vcc=4.0–5.5V)
M38039FFHWG			PTLG0064JA-A (64F0G)	
M38039FFSP			PRDP0064BA-A (64P4B)	
M38039FFFP	PRQP0064GA-A (64P6N-A)	Flash memory version (Vcc=4.0–5.5V)		
M38039FFHP	PLQP0064KB-A (64P6Q-A)			

**FUNCTIONAL DESCRIPTION**

**CENTRAL PROCESSING UNIT (CPU)**

The 3803 group (Spec.H QzROM version) uses the standard 740 Family instruction set. Refer to the table of 740 Family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 Family instructions are as follows:

- The FST and SLW instructions cannot be used.
- The STP, WIT, MUL, and DIV instructions can be used.

**[Accumulator (A)]**

The accumulator is an 8-bit register. Data operations such as data transfer, etc. are executed mainly through the accumulator.

**[Index Register X (X)]**

The index register X is an 8-bit register. In the index addressing modes, the value of the OPERAND is added to the contents of register X and specifies the real address.

**[Index Register Y (Y)]**

The index register Y is an 8-bit register. In partial instruction, the value of the OPERAND is added to the contents of register Y and specifies the real address.

**[Stack Pointer (S)]**

The stack pointer is an 8-bit register used during subroutine calls and interrupts. This register indicates start address of stored area (stack) for storing registers during subroutine calls and interrupts.

The low-order 8 bits of the stack address are determined by the contents of the stack pointer. The high-order 8 bits of the stack address are determined by the stack page selection bit. If the stack page selection bit is "0", the high-order 8 bits becomes "0016". If the stack page selection bit is "1", the high-order 8 bits becomes "0116".

The operations of pushing register contents onto the stack and popping them from the stack are shown in Figure.7.

Store registers other than those described in Figure.6 with program when the user needs them during interrupts or subroutine calls (see Table 6).

**[Program Counter (PC)]**

The program counter is a 16-bit counter consisting of two 8-bit registers PCH and PCL. It is used to indicate the address of the next instruction to be executed.

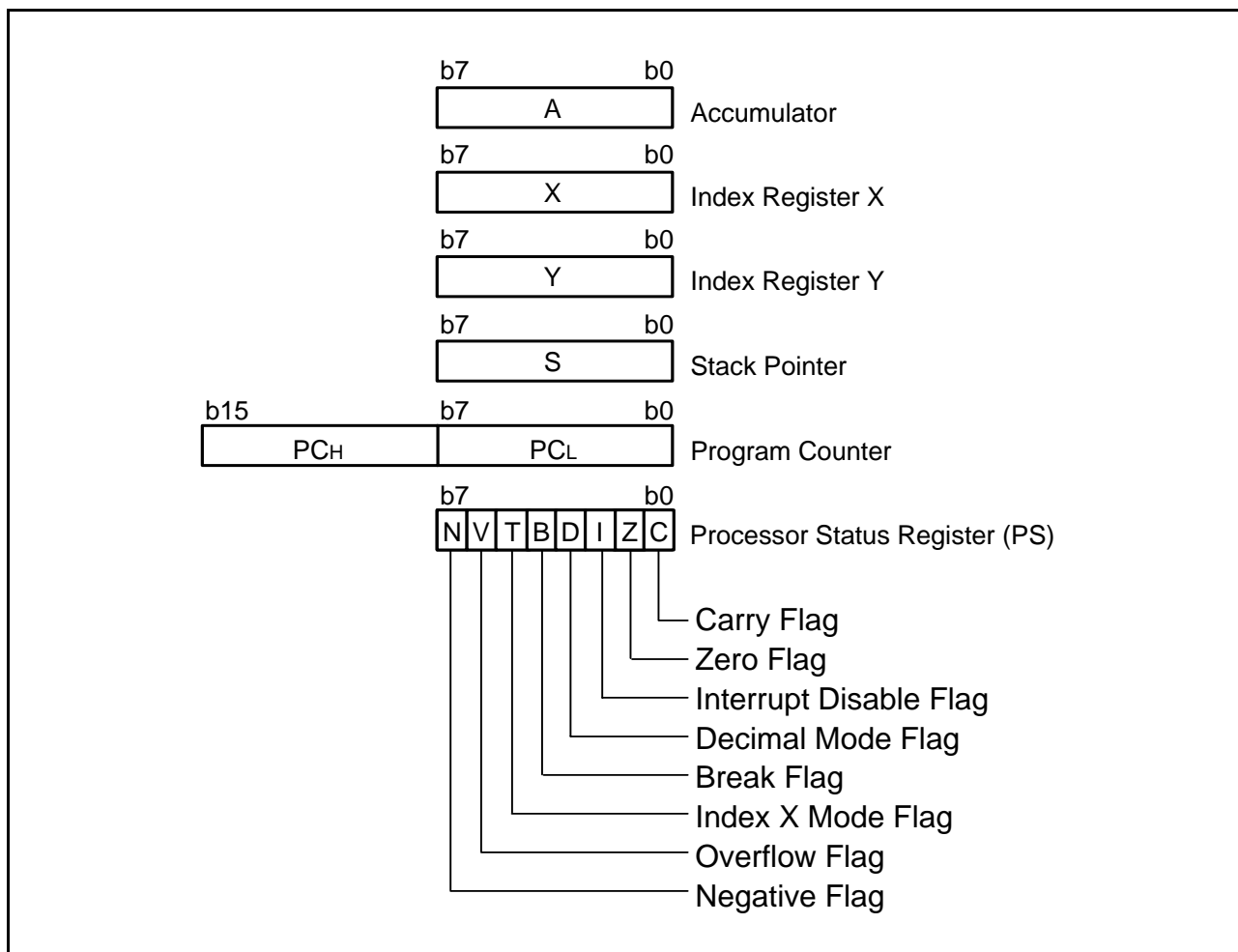


Fig 6. 740 Family CPU register structure

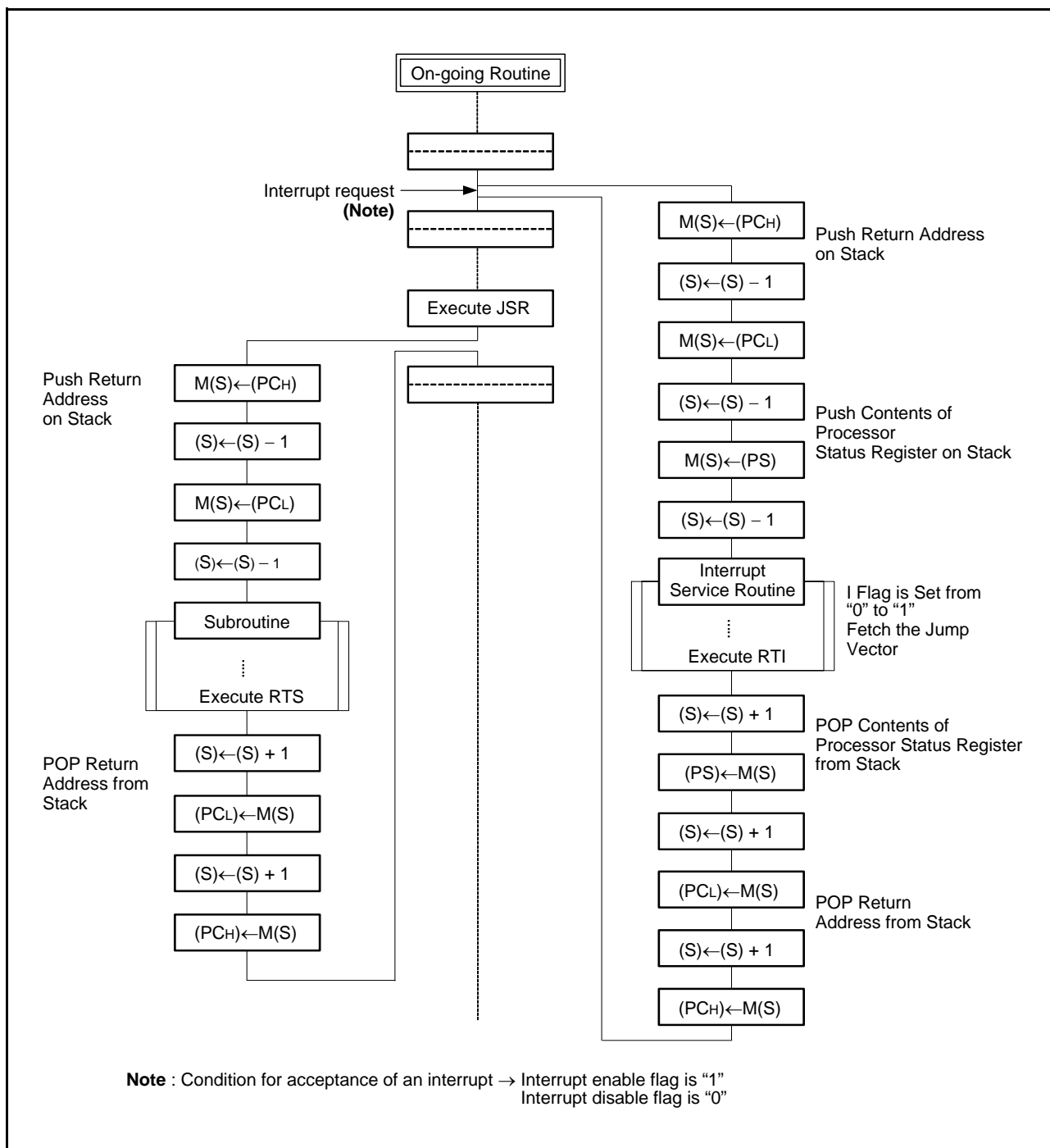


Fig 7. Register push and pop at interrupt generation and subroutine call

Table 6 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

**[Processor status register (PS)]**

The processor status register is an 8-bit register consisting of 5 flags which indicate the status of the processor after an arithmetic operation and 3 flags which decide MCU operation. Branch operations can be performed by testing the Carry (C) flag, Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

**Bit 0: Carry flag (C)**

The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

**Bit 1: Zero flag (Z)**

The Z flag is set if the result of an immediate arithmetic operation or a data transfer is "0", and cleared if the result is anything other than "0".

**Bit 2: Interrupt disable flag (I)**

The I flag disables all interrupts except for the interrupt generated by the BRK instruction. Interrupts are disabled when the I flag is "1".

**Bit 3: Decimal mode flag (D)**

The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is "0"; decimal arithmetic is executed when it is "1".

Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can execute decimal arithmetic.

**Bit 4: Break flag (B)**

The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always "0". When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to "1".

**Bit 5: Index X mode flag (T)**

When the T flag is "0", arithmetic operations are performed between accumulator and memory. When the T flag is "1", direct arithmetic operations and direct data transfers are enabled between memory locations.

**Bit 6: Overflow flag (V)**

The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

**Bit 7: Negative flag (N)**

The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 7 Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	–	SEI	SED	–	SET	–	–
Clear instruction	CLC	–	CLI	CLD	–	CLT	CLV	–

**[CPU Mode Register (CPUM)] 003B16**

The CPU mode register contains the stack page selection bit, the internal system clock control bits, etc.  
The CPU mode register is allocated at address 003B16.

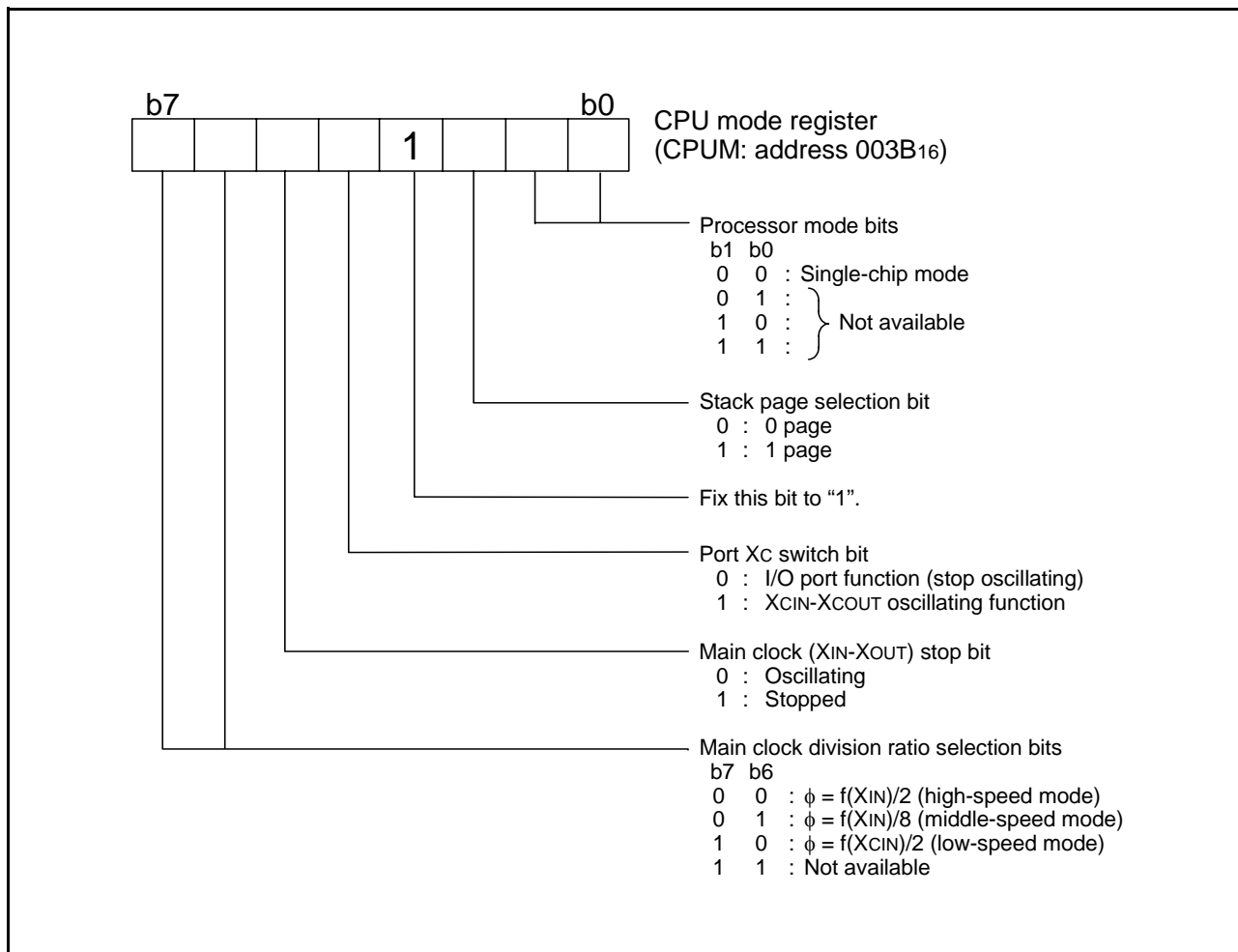


Fig 8. Structure of CPU mode register

**MISRG**

**(1) Bit 0 of address 0010<sub>16</sub>: Oscillation stabilizing time set after STP instruction released bit**

When the MCU stops the clock oscillation by the STP instruction and the STP instruction has been released by an external interrupt source, usually, the fixed values of Timer 1 and Prescaler 12 (Timer 1 = 01<sub>16</sub>, Prescaler 12 = FF<sub>16</sub>) are automatically reloaded in order for the oscillation to stabilize. The user can inhibit the automatic setting by setting "1" to bit 0 of MISRG (address 0010<sub>16</sub>).

However, by setting this bit to "1", the previous values, set just before the STP instruction was executed, will remain in Timer 1 and Prescaler 12. Therefore, you will need to set an appropriate value to each register, in accordance with the oscillation stabilizing time, before executing the STP instruction.

Figure.9 shows the structure of MISRG.

**(2) Bits 1, 2, 3 of address 0010<sub>16</sub>: Middle-speed Mode Automatic Switch Function**

In order to switch the clock mode of an MCU which has a sub-clock, the following procedure is necessary:

set CPU mode register (003B<sub>16</sub>) --> start main clock oscillation --> wait for oscillation stabilization --> switch to middle-speed mode (or high-speed mode).

However, the 3803 group (Spec.H QzROM version) has the built-in function which automatically switches from low to middle-speed mode by program.

**• Middle-speed mode automatic switch by program**

The middle-speed mode can also be automatically switched by program while operating in low-speed mode. By setting the middle-speed automatic switch start bit (bit 3) of MISRG (address 0010<sub>16</sub>) to "1" in the condition that the middle-speed mode automatic switch set bit is "1" while operating in low-speed mode, the MCU will automatically switch to middle-speed mode. In this case, the oscillation stabilizing time of the main clock can be selected by the middle-speed automatic switch wait time set bit (bit 2) of MISRG (address 0010<sub>16</sub>).

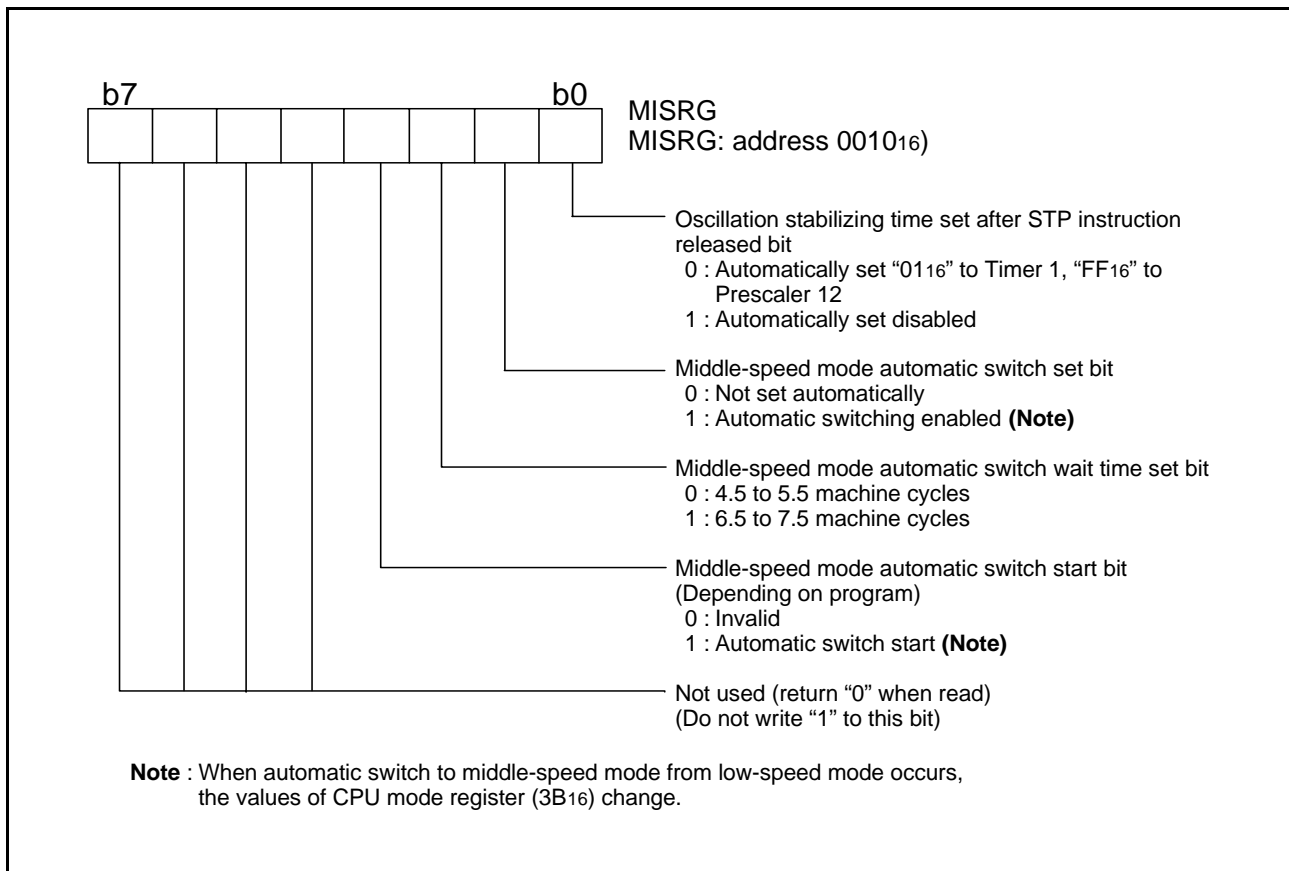


Fig 9. Structure of MISRG

**MEMORY**

**• Special Function Register (SFR) Area**

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

**• RAM**

The RAM is used for data storage and for stack area of subroutine calls and interrupts.

**• ROM**

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is a user area for storing programs. In the QzROM version, 1 byte of address FFDB<sub>16</sub> is also a reserved area.

**• Interrupt Vector Area**

The interrupt vector area contains reset and interrupt vectors.

**• Zero Page**

Access to this area with only 2 bytes is possible in the zero page addressing mode.

**• Special Page**

Access to this area with only 2 bytes is possible in the special page addressing mode.

**• ROM Code Protect Address (address FFDB<sub>16</sub>)**

Address FFDB<sub>16</sub>, which is the reserved ROM area of QzROM, is the ROM code protect address. “00<sub>16</sub>” or “FE<sub>16</sub>” is written into this address when selecting the protect bit write by using a serial programmer or selecting protect enabled for writing shipment by Renesas Technology corp.. When “00<sub>16</sub>” or “FE<sub>16</sub>” is set to the ROM code protect address, the protect function is enabled, so that reading or writing from/to QzROM is disabled by a serial programmer.

As for the QzROM product in blank, the ROM code is protected by selecting the protect bit write at ROM writing with a serial programmer.

The protect can be performed, dividing twice. The protect area 1 is from the beginning address of ROM to address “EFFF<sub>16</sub>”. As for the QzROM product shipped after writing, “00<sub>16</sub>” (protect enabled to all area), “FE<sub>16</sub>” (protect enabled to the protect area 1) or “FF<sub>16</sub>” (protect disabled) is written into the ROM code protect address when Renesas Technology corp. performs writing.

The writing of “00<sub>16</sub>”, “FE<sub>16</sub>” or “FF<sub>16</sub>” can be selected as ROM option setup (“MASK option” written in the mask file converter) when ordering.

**<Notes>**

Since the contents of RAM are undefined at reset, be sure to set an initial value before use.

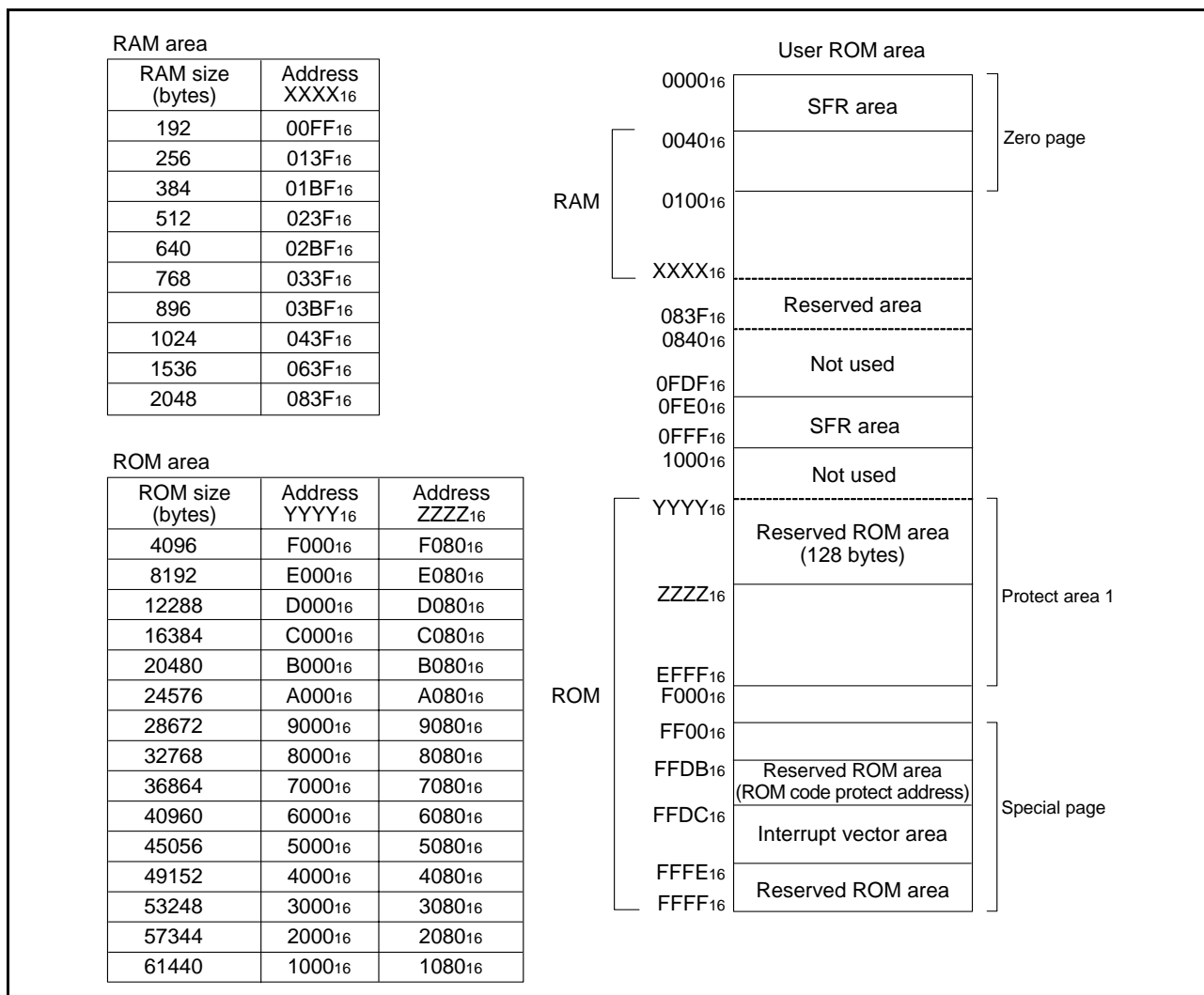


Fig 10. Memory map diagram

0000 <sub>16</sub>	Port P0 (P0)	0020 <sub>16</sub>	Prescaler 12 (PRE12)
0001 <sub>16</sub>	Port P0 direction register (P0D)	0021 <sub>16</sub>	Timer 1 (T1)
0002 <sub>16</sub>	Port P1 (P1)	0022 <sub>16</sub>	Timer 2 (T2)
0003 <sub>16</sub>	Port P1 direction register (P1D)	0023 <sub>16</sub>	Timer XY mode register (TM)
0004 <sub>16</sub>	Port P2 (P2)	0024 <sub>16</sub>	Prescaler X (PREX)
0005 <sub>16</sub>	Port P2 direction register (P2D)	0025 <sub>16</sub>	Timer X (TX)
0006 <sub>16</sub>	Port P3 (P3)	0026 <sub>16</sub>	Prescaler Y (PREY)
0007 <sub>16</sub>	Port P3 direction register (P3D)	0027 <sub>16</sub>	Timer Y (TY)
0008 <sub>16</sub>	Port P4 (P4)	0028 <sub>16</sub>	Timer Z low-order (TZL)
0009 <sub>16</sub>	Port P4 direction register (P4D)	0029 <sub>16</sub>	Timer Z high-order (TZH)
000A <sub>16</sub>	Port P5 (P5)	002A <sub>16</sub>	Timer Z mode register (TZM)
000B <sub>16</sub>	Port P5 direction register (P5D)	002B <sub>16</sub>	PWM control register (PWMCN)
000C <sub>16</sub>	Port P6 (P6)	002C <sub>16</sub>	PWM prescaler (PREPWM)
000D <sub>16</sub>	Port P6 direction register (P6D)	002D <sub>16</sub>	PWM register (PWM)
000E <sub>16</sub>	Timer 12, X count source selection register (T12XCSS)	002E <sub>16</sub>	
000F <sub>16</sub>	Timer Y, Z count source selection register (TYZCSS)	002F <sub>16</sub>	Baud rate generator 3 (BRG3)
0010 <sub>16</sub>	MISRG	0030 <sub>16</sub>	Transmit/Receive buffer register 3 (TB3/RB3)
0011 <sub>16</sub>	Reserved *	0031 <sub>16</sub>	Serial I/O3 status register (SIO3STS)
0012 <sub>16</sub>	Reserved *	0032 <sub>16</sub>	Serial I/O3 control register (SIO3CON)
0013 <sub>16</sub>	Reserved *	0033 <sub>16</sub>	UART3 control register (UART3CON)
0014 <sub>16</sub>	Reserved *	0034 <sub>16</sub>	AD/DA control register (ADCON)
0015 <sub>16</sub>	Reserved *	0035 <sub>16</sub>	AD conversion register 1 (AD1)
0016 <sub>16</sub>	Reserved *	0036 <sub>16</sub>	DA1 conversion register (DA1)
0017 <sub>16</sub>	Reserved *	0037 <sub>16</sub>	DA2 conversion register (DA2)
0018 <sub>16</sub>	Transmit/Receive buffer register 1 (TB1/RB1)	0038 <sub>16</sub>	AD conversion register 2 (AD2)
0019 <sub>16</sub>	Serial I/O1 status register (SIO1STS)	0039 <sub>16</sub>	Interrupt source selection register (INTSEL)
001A <sub>16</sub>	Serial I/O1 control register (SIO1CON)	003A <sub>16</sub>	Interrupt edge selection register (INTEDGE)
001B <sub>16</sub>	UART1 control register (UART1CON)	003B <sub>16</sub>	CPU mode register (CPUM)
001C <sub>16</sub>	Baud rate generator (BRG1)	003C <sub>16</sub>	Interrupt request register 1 (IREQ1)
001D <sub>16</sub>	Serial I/O2 control register (SIO2CON)	003D <sub>16</sub>	Interrupt request register 2 (IREQ2)
001E <sub>16</sub>	Watchdog timer control register (WDTCON)	003E <sub>16</sub>	Interrupt control register 1 (ICON1)
001F <sub>16</sub>	Serial I/O2 register (SIO2)	003F <sub>16</sub>	Interrupt control register 2 (ICON2)
0FE0 <sub>16</sub>	Reserved *	0FF0 <sub>16</sub>	Port P0 pull-up control register (PULL0)
0FE1 <sub>16</sub>	Reserved *	0FF1 <sub>16</sub>	Port P1 pull-up control register (PULL1)
0FE2 <sub>16</sub>	Reserved *	0FF2 <sub>16</sub>	Port P2 pull-up control register (PULL2)
0FE3 <sub>16</sub>	Reserved *	0FF3 <sub>16</sub>	Port P3 pull-up control register (PULL3)
0FE4 <sub>16</sub>	Reserved *	0FF4 <sub>16</sub>	Port P4 pull-up control register (PULL4)
0FE5 <sub>16</sub>	Reserved *	0FF5 <sub>16</sub>	Port P5 pull-up control register (PULL5)
0FE6 <sub>16</sub>	Reserved *	0FF6 <sub>16</sub>	Port P6 pull-up control register (PULL6)
0FE7 <sub>16</sub>	Reserved *		
0FE8 <sub>16</sub>	Reserved *		
0FE9 <sub>16</sub>	Reserved *		
0FEA <sub>16</sub>	Reserved *		
0FEB <sub>16</sub>	Reserved *		
0FEC <sub>16</sub>	Reserved *		
0FED <sub>16</sub>	Reserved *		
0FEE <sub>16</sub>	Reserved *		
0FEF <sub>16</sub>	Reserved *		

\*Reserved area: Do not write any data to these addresses, because these areas are reserved.

Fig 11. Memory map of special function register (SFR)



**I/O PORTS**

The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input port or output port.

When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

By setting the port P0 pull-up control register (address 0FF016) to the port P6 pull-up control register (address 0FF616) ports can control pull-up with a program. However, the contents of these registers do not affect ports programmed as the output ports.

Table 8 I/O port function

Pin	Name	Input/Output	I/O Structure	Non-Port Function	Related SFRs	Ref. No.	
P00/AN8–P07/AN15	Port P0	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	A/D converter input	AD/DA control register	(1)	
P10/INT41 P11/INT01	Port P1			External interrupt input	Interrupt edge selection register	(2)	
P12–P17						(3)	
P20/LED0–P27/LED7	Port P2						
P30/DA1 P31/DA2	Port P3			D/A converter output	AD/DA control register	(4)	
P32, P33				CMOS compatible input level N-channel open-drain output		(5)	
P34/RxD3 P35/TxD3 P36/SCLK3 P37/SRDY3				CMOS compatible input level CMOS 3-state output	Serial I/O3 function I/O	Serial I/O3 control register UART3 control register	(6) (7) (8) (9)
P40/INT40/XCOUT P41/INT00/XCIN	Port P4			External interrupt input Sub-clock generating circuit	Interrupt edge selection register CPU mode register	(10) (11)	
P42/INT1 P43/INT2				External interrupt input	Interrupt edge selection register	(2)	
P44/RxD1 P45/TxD1 P46/SCLK1				Serial I/O1 function I/O	Serial I/O1 control register UART1 control register	(6) (7) (8)	
P47/SRDY1/CNTR2		Serial I/O1 function I/O Timer Z function I/O	Serial I/O1 control register Timer Z mode register	(12)			
P50/SIN2 P51/SOUT2 P52/SCLK2 P53/SRDY2		Port P5	Serial I/O2 function I/O	Serial I/O2 control register	(13) (14) (15) (16)		
P54/CNTR0 P55/CNTR1	Timer X, Y function I/O		Timer XY mode register	(17)			
P56/PWM	PWM output		PWM control register	(18)			
P57/INT3	External interrupt input		Interrupt edge selection register	(2)			
P60/AN0–P67/AN7	Port P6		A/D converter input	AD/DA control register	(1)		

**NOTES:**

1. Refer to the applicable sections how to use double-function ports as function I/O ports.
2. Make sure that the input level at each pin is either 0 V or V<sub>CC</sub> during execution of the STP instruction.  
When an input level is at an intermediate potential, a current will flow from V<sub>CC</sub> to V<sub>SS</sub> through the input-stage gate.

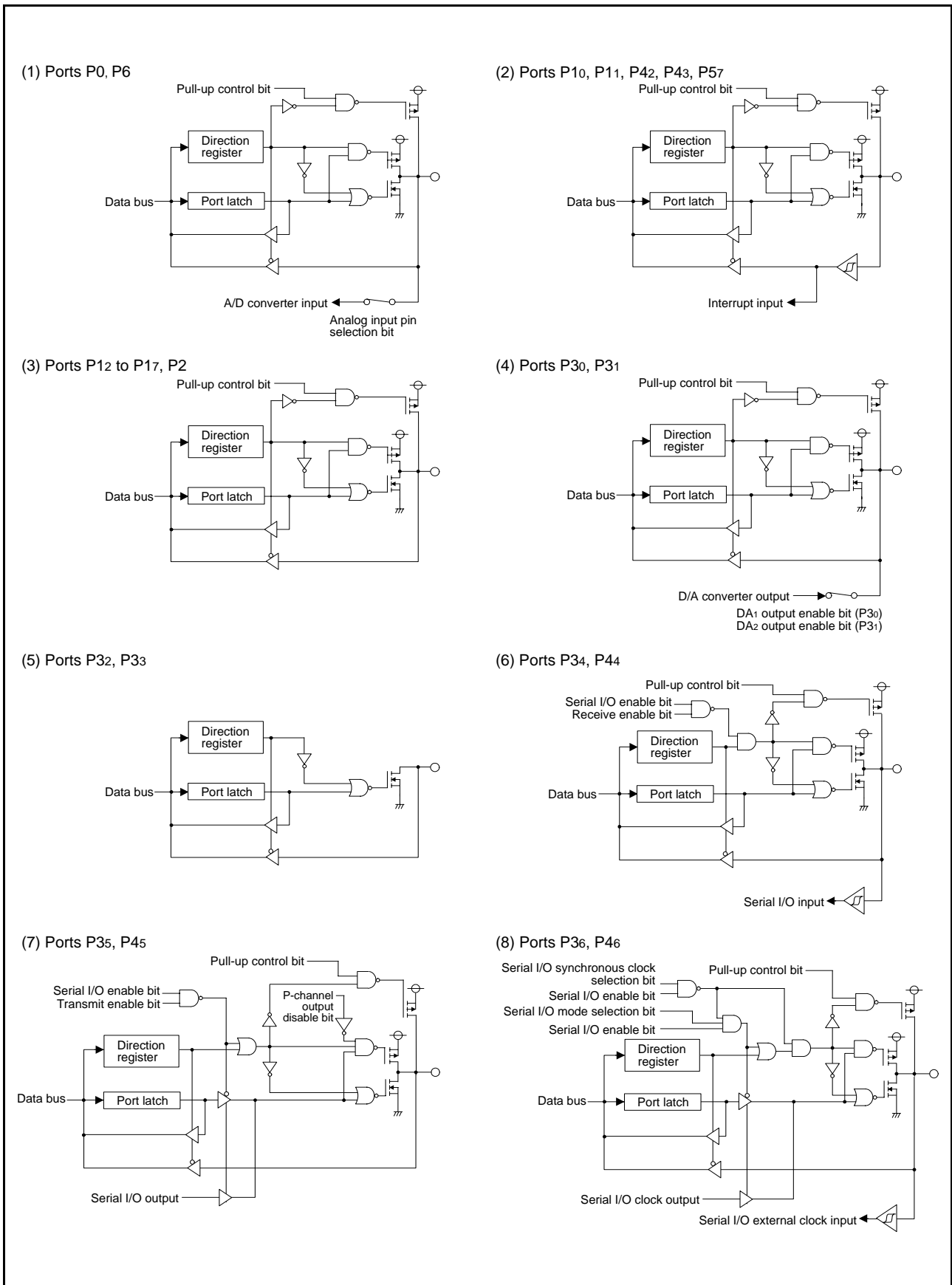


Fig 12. Port block diagram (1)

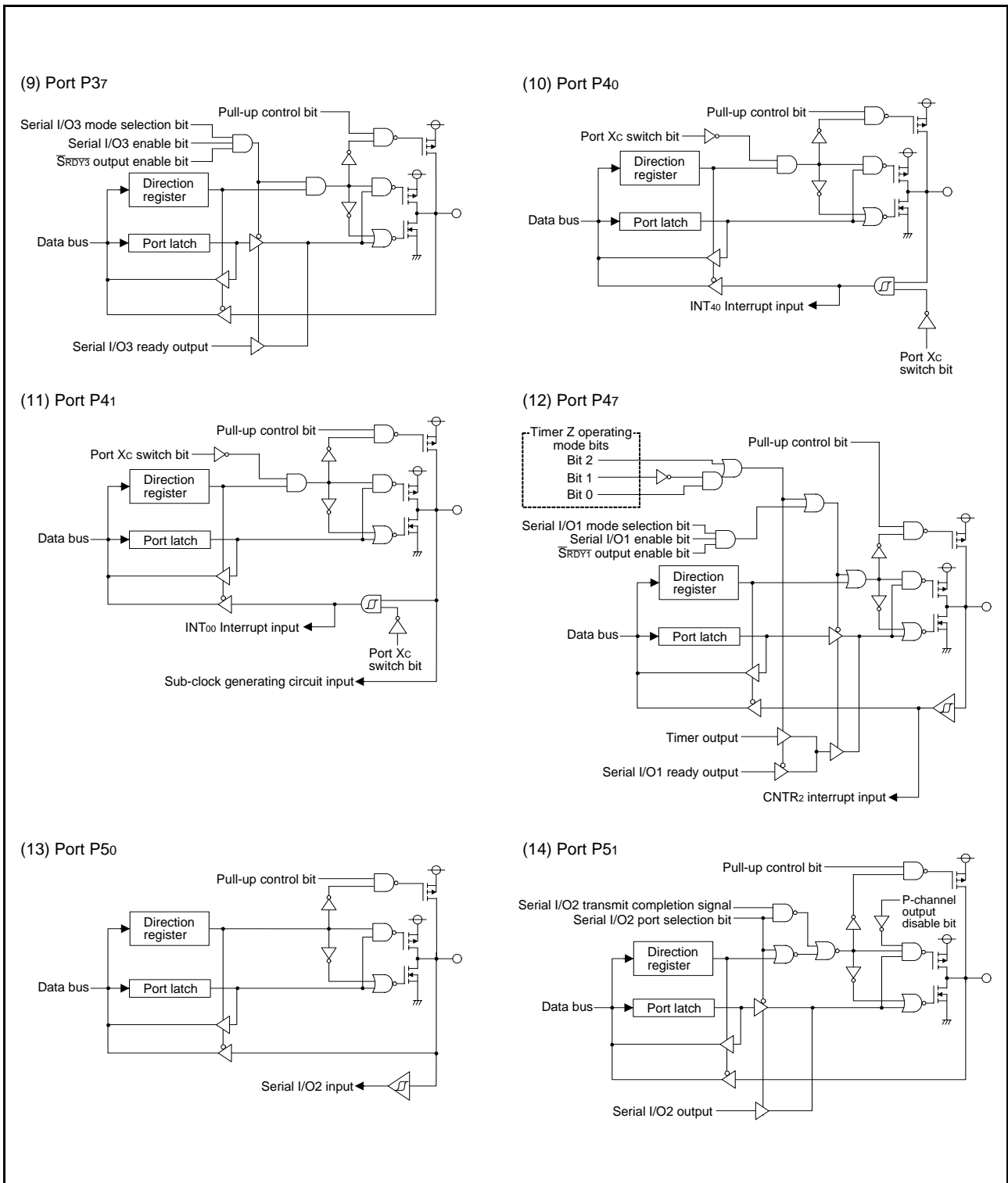


Fig 13. Port block diagram (2)

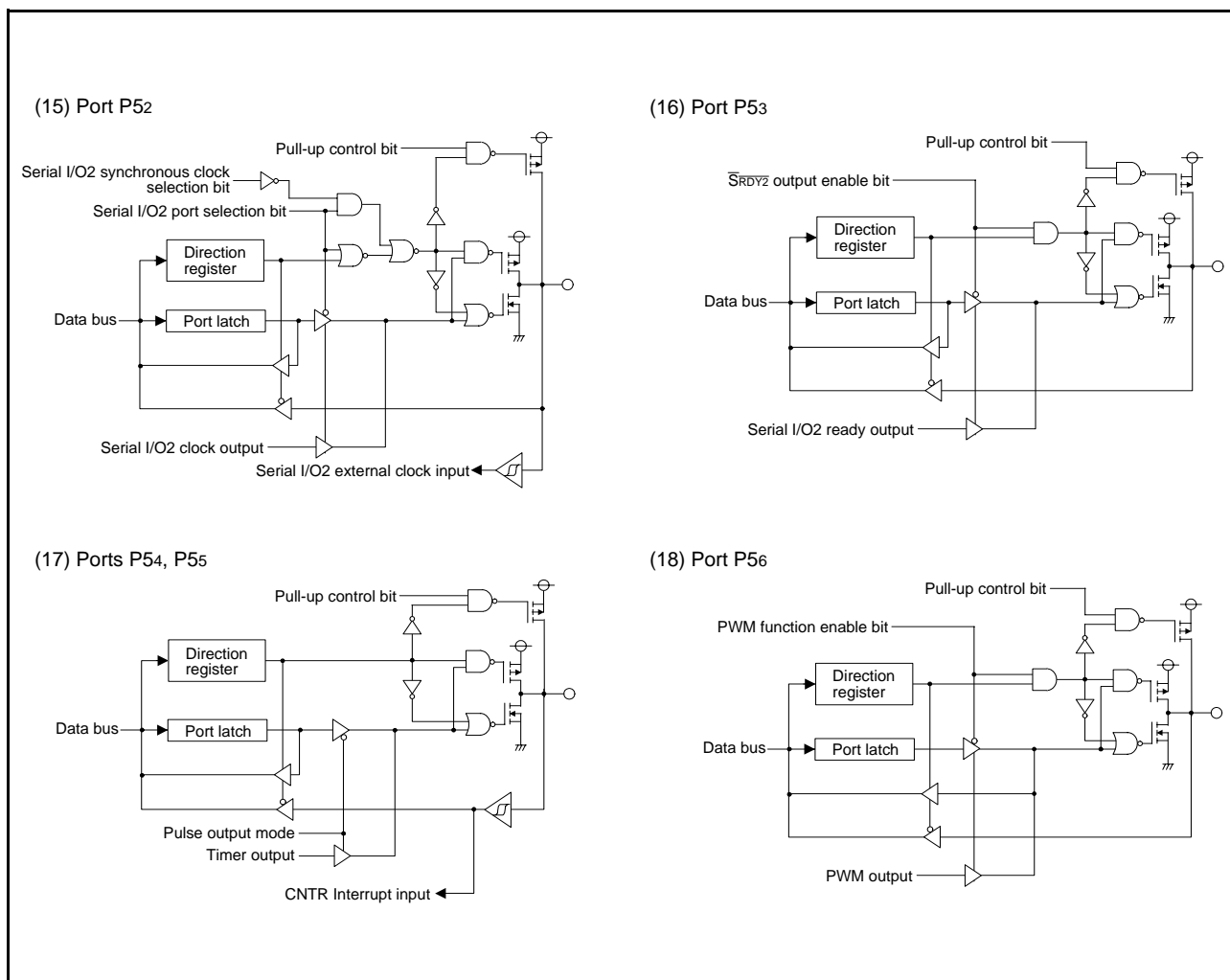


Fig 14. Port block diagram (3)



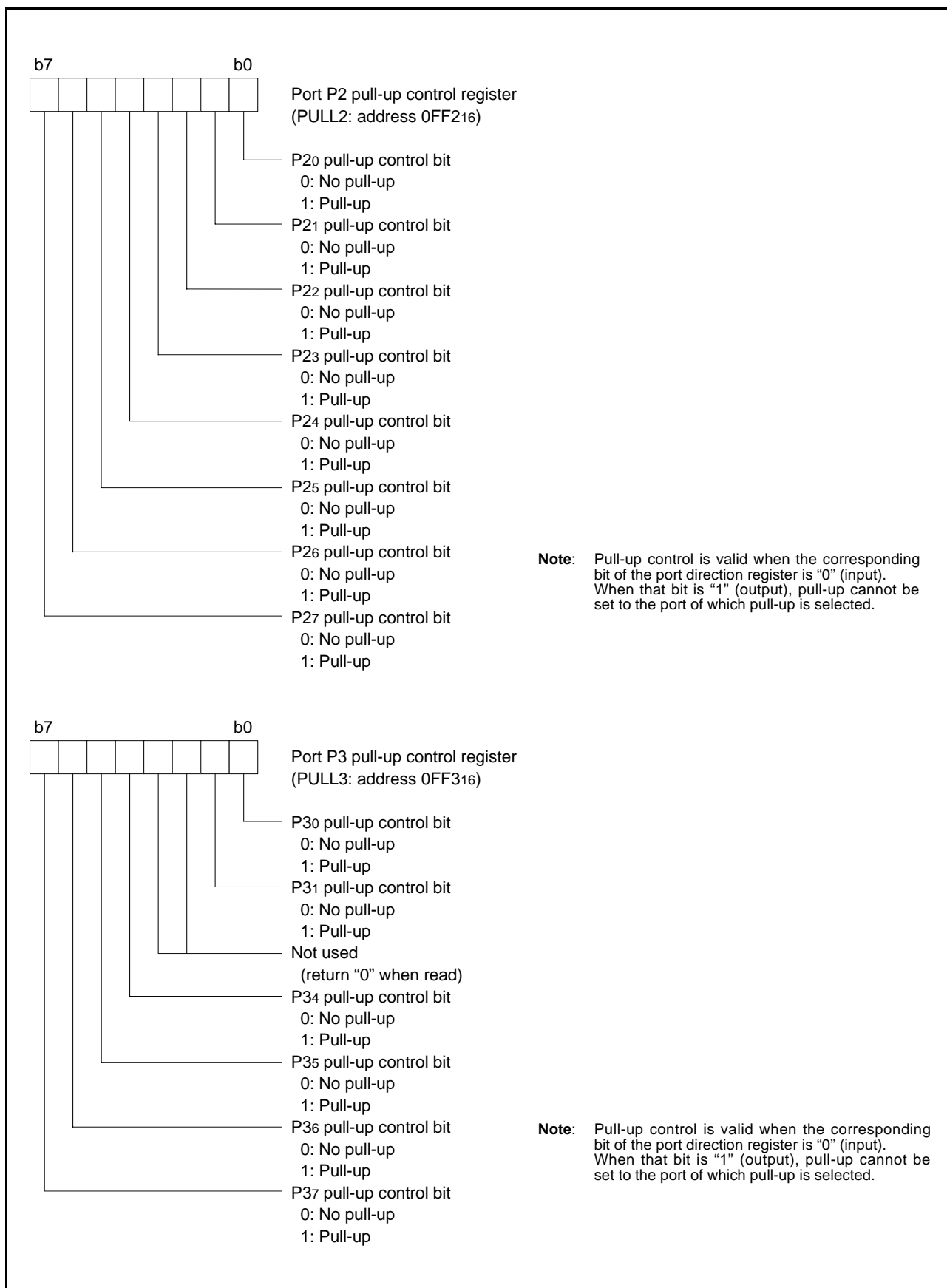


Fig 16. Structure of port pull-up control register (2)

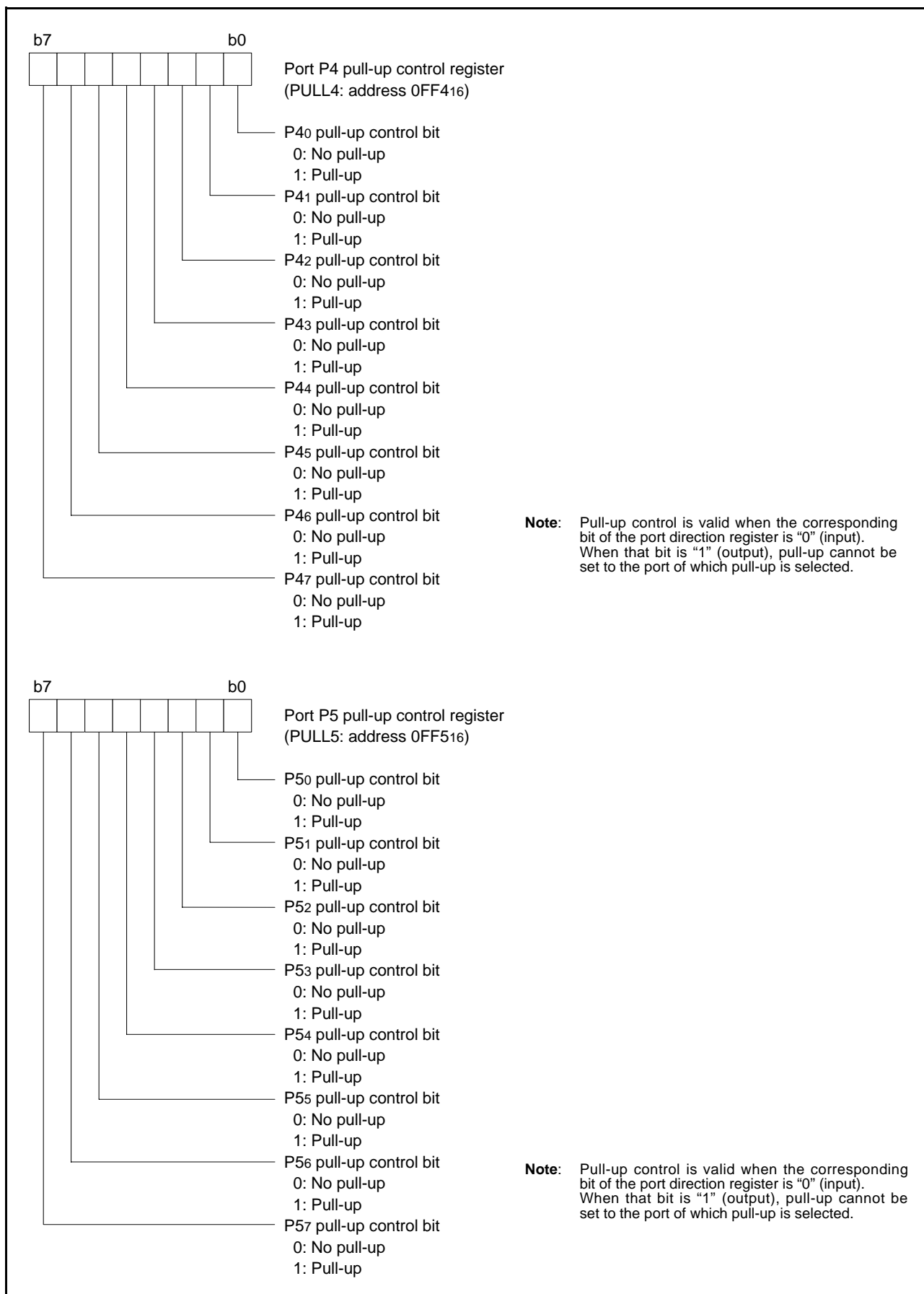


Fig 17. Structure of port pull-up control register (3)

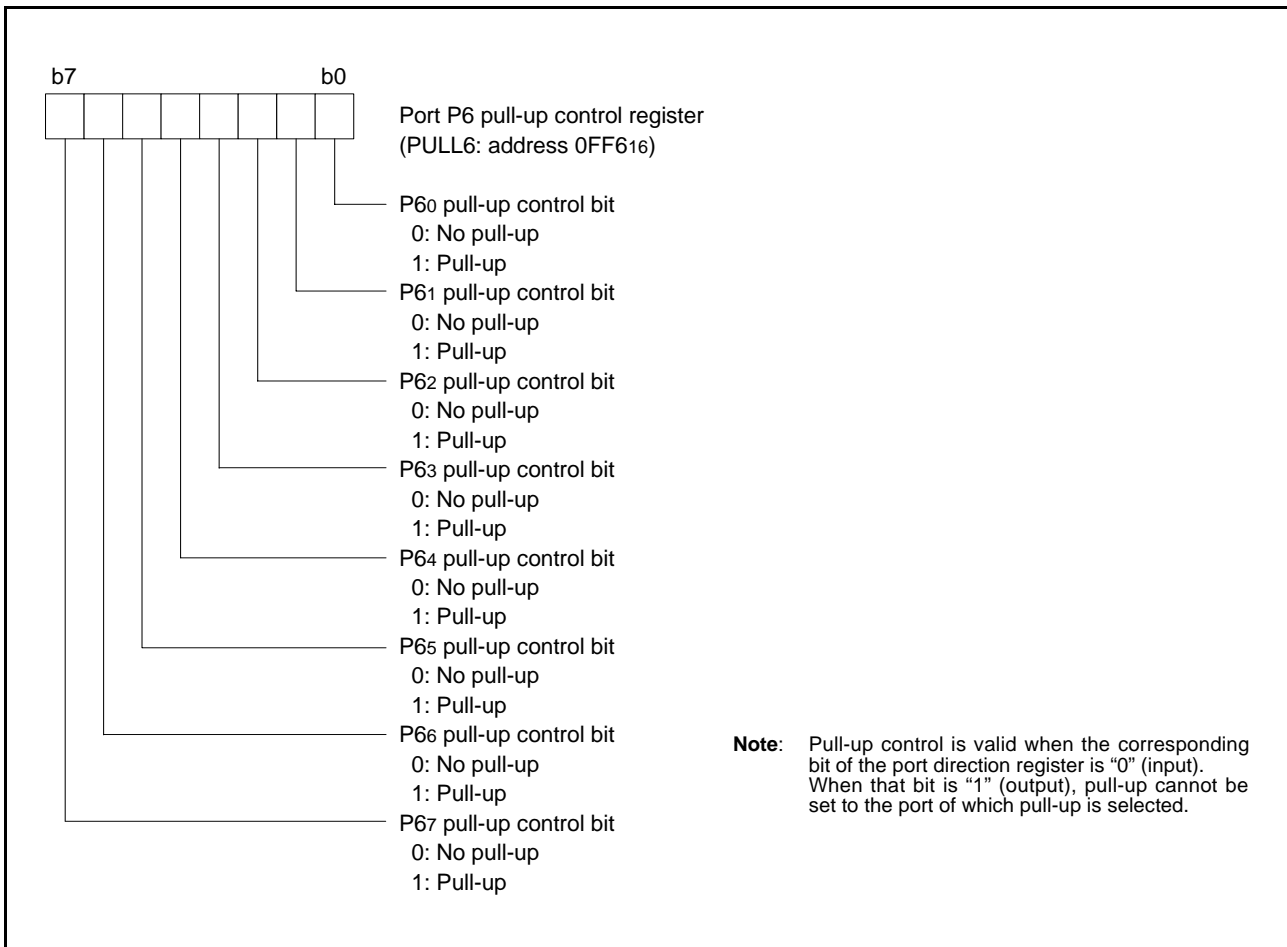


Fig 18. Structure of port pull-up control register (4)



## INTERRUPTS

The 3803 group (Spec.H QzROM version)'s interrupts are a type of vector and occur by 16 sources among 21 sources: eight external, twelve internal, and one software.

### • Interrupt Control

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt occurs if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".

Interrupt enable bits can be set or cleared by software.

Interrupt request bits can be cleared by software, but cannot be set by software.

The reset and the BRK instruction cannot be disabled with any flag or bit. The I (interrupt disable) flag disables all interrupts except the reset and the BRK instruction interrupt.

When several interrupt requests occur at the same time, the interrupts are received according to priority.

### • Interrupt Operation

By acceptance of an interrupt, the following operations are automatically performed:

1. The contents of the program counter and the processor status register are automatically pushed onto the stack.
2. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
3. The interrupt jump destination address is read from the vector table into the program counter.

### • Interrupt Source Selection

Which of each combination of the following interrupt sources can be selected by the interrupt source selection register (address 0039<sub>16</sub>).

1. INT<sub>0</sub> or Timer Z
2. CNTR<sub>1</sub> or Serial I/O<sub>3</sub> reception
3. Serial I/O<sub>2</sub> or Timer Z
4. INT<sub>4</sub> or CNTR<sub>2</sub>
5. A/D converter or serial I/O<sub>3</sub> transmission

### • External Interrupt Pin Selection

The occurrence sources of the external interrupt INT<sub>0</sub> and INT<sub>4</sub> can be selected from either input from INT<sub>00</sub> and INT<sub>40</sub> pin, or input from INT<sub>01</sub> and INT<sub>41</sub> pin by the INT<sub>0</sub>, INT<sub>4</sub> interrupt switch bit of interrupt edge selection register (bit 6 of address 003A<sub>16</sub>).

## <Notes>

When setting the followings, the interrupt request bit may be set to "1".

- When setting external interrupt active edge

Related register: Interrupt edge selection register  
(address 003A<sub>16</sub>)

Timer XY mode register (address 0023<sub>16</sub>)

Timer Z mode register (address 002A<sub>16</sub>)

- When switching interrupt sources of an interrupt vector address where two or more interrupt sources are allocated

Related register: Interrupt source selection register  
(address 0039<sub>16</sub>)

When not requiring for the interrupt occurrence synchronized with these setting, take the following sequence.

- (1) Set the corresponding interrupt enable bit to "0" (disabled).
- (2) Set the interrupt edge select bit (the active edge switch bit) or the interrupt source select bit.
- (3) Set the corresponding interrupt request bit to "0" after 1 or more instructions have been executed.
- (4) Set the corresponding interrupt enable bit to "1" (enabled).

Table 9 Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses <sup>(1)</sup>		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset <sup>(2)</sup>	1	FFFD <sub>16</sub>	FFFC <sub>16</sub>	At reset	Non-maskable
INT <sub>0</sub>	2	FFFB <sub>16</sub>	FFFA <sub>16</sub>	At detection of either rising or falling edge of INT <sub>0</sub> input	External interrupt (active edge selectable)
Timer Z				At timer Z underflow	
INT <sub>1</sub>	3	FFF9 <sub>16</sub>	FFF8 <sub>16</sub>	At detection of either rising or falling edge of INT <sub>1</sub> input	External interrupt (active edge selectable)
Serial I/O1 reception	4	FFF7 <sub>16</sub>	FFF6 <sub>16</sub>	At completion of serial I/O1 data reception	Valid when serial I/O1 is selected
Serial I/O1 transmission	5	FFF5 <sub>16</sub>	FFF4 <sub>16</sub>	At completion of serial I/O1 transmission shift or when transmission buffer is empty	Valid when serial I/O1 is selected
Timer X	6	FFF3 <sub>16</sub>	FFF2 <sub>16</sub>	At timer X underflow	
Timer Y	7	FFF1 <sub>16</sub>	FFF0 <sub>16</sub>	At timer Y underflow	
Timer 1	8	FFEF <sub>16</sub>	FFEE <sub>16</sub>	At timer 1 underflow	STP release timer underflow
Timer 2	9	FFED <sub>16</sub>	FFEC <sub>16</sub>	At timer 2 underflow	
CNTR <sub>0</sub>	10	FFEB <sub>16</sub>	FFEA <sub>16</sub>	At detection of either rising or falling edge of CNTR <sub>0</sub> input	External interrupt (active edge selectable)
CNTR <sub>1</sub>				At detection of either rising or falling edge of CNTR <sub>1</sub> input	
Serial I/O3 reception	11	FFE9 <sub>16</sub>	FFE8 <sub>16</sub>	At completion of serial I/O3 data reception	Valid when serial I/O3 is selected
Serial I/O2				At completion of serial I/O2 data transmission or reception	
Timer Z	12	FFE7 <sub>16</sub>	FFE6 <sub>16</sub>	At timer Z underflow	Valid when serial I/O2 is selected
INT <sub>2</sub>				At detection of either rising or falling edge of INT <sub>2</sub> input	
INT <sub>3</sub>	13	FFE5 <sub>16</sub>	FFE4 <sub>16</sub>	At detection of either rising or falling edge of INT <sub>3</sub> input	External interrupt (active edge selectable)
INT <sub>4</sub>	14	FFE3 <sub>16</sub>	FFE2 <sub>16</sub>	At detection of either rising or falling edge of INT <sub>4</sub> input	External interrupt (active edge selectable)
CNTR <sub>2</sub>				At detection of either rising or falling edge of CNTR <sub>2</sub> input	
A/D converter	15	FFDF <sub>16</sub>	FFDE <sub>16</sub>	At completion of A/D conversion	Valid when serial I/O3 is selected
Serial I/O3 transmission				At completion of serial I/O3 transmission shift or when transmission buffer is empty	
BRK instruction	16	FFDD <sub>16</sub>	FFDC <sub>16</sub>	At BRK instruction execution	Non-maskable software interrupt

## NOTES:

1. Vector addresses contain interrupt jump destination addresses.
2. Reset function in the same way as an interrupt with the highest priority.

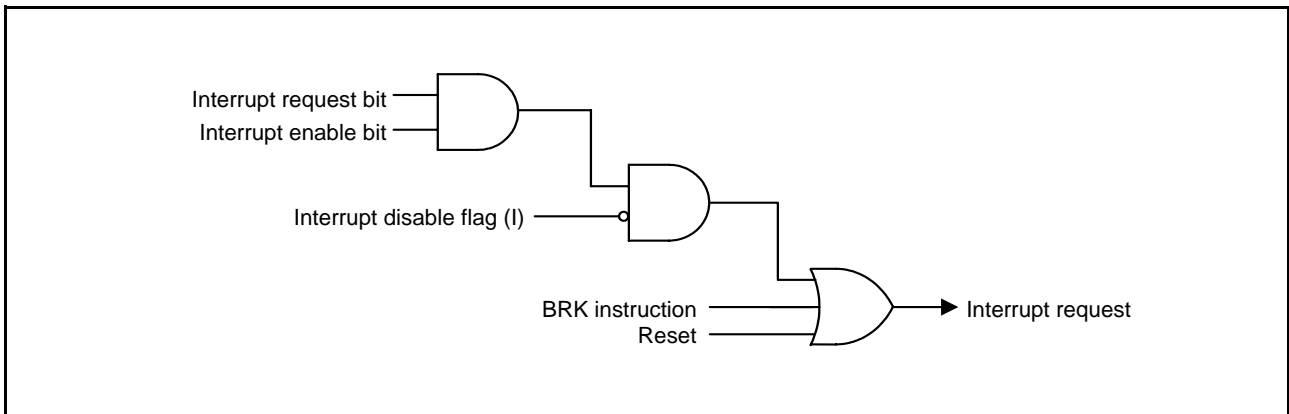


Fig 19. Interrupt control

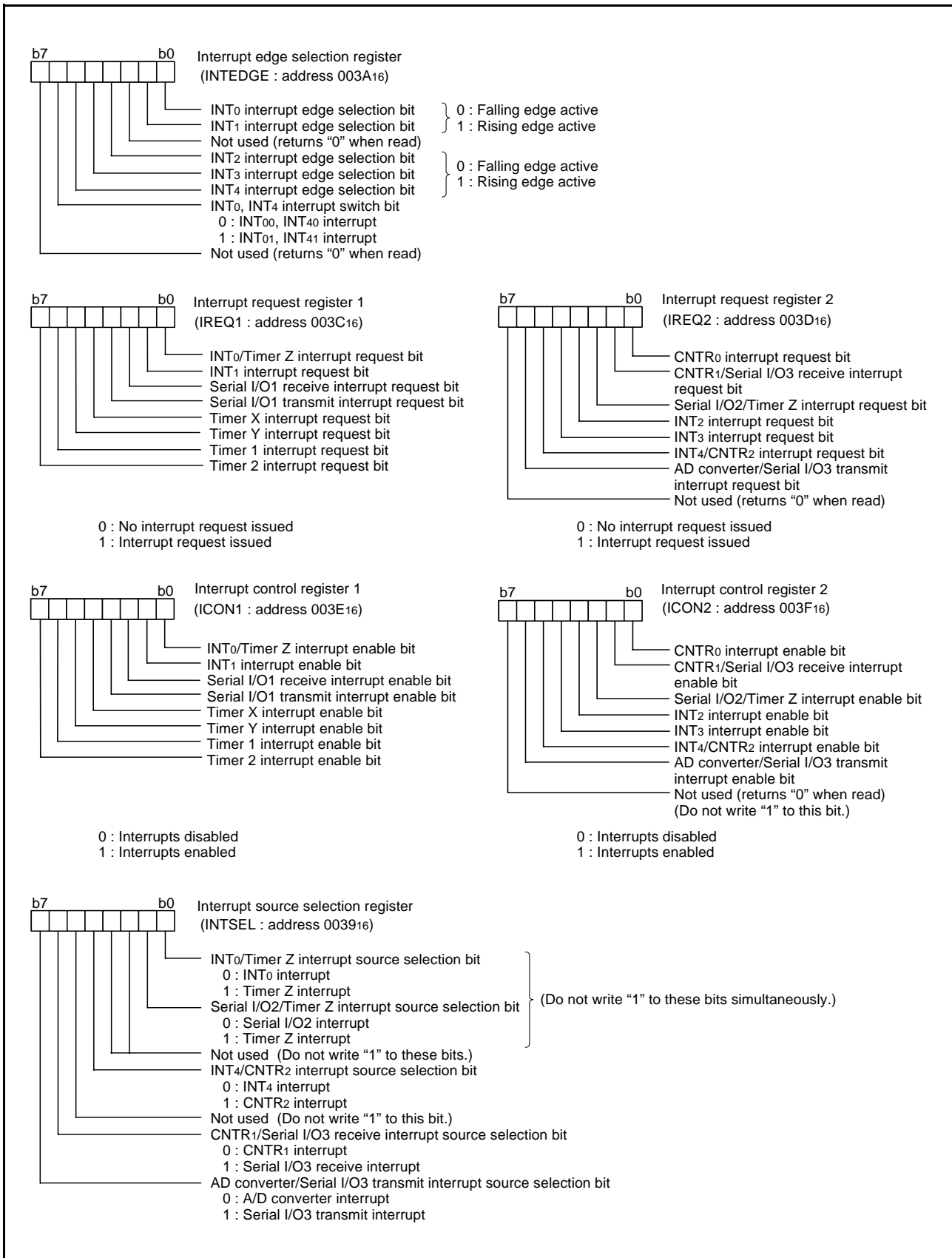


Fig 20. Structure of interrupt-related registers

**TIMERS****• 8-bit Timers**

The 3803 group (Spec.H QzROM version) has four 8-bit timers: timer 1, timer 2, timer X, and timer Y.

The timer 1 and timer 2 use one prescaler in common, and the timer X and timer Y use each prescaler. Those are 8-bit prescalers. Each of the timers and prescalers has a timer latch or a prescaler latch.

The division ratio of each timer or prescaler is given by  $1/(n + 1)$ , where  $n$  is the value in the corresponding timer or prescaler latch. All timers are down-counters. When the timer reaches "00<sub>16</sub>", an underflow occurs at the next count pulse and the contents of the corresponding timer latch are reloaded into the timer and the count is continued. When the timer underflows, the interrupt request bit corresponding to that timer is set to "1".

**• Timer divider**

The divider count source is switched by the main clock division ratio selection bits of CPU mode register (bits 7 and 6 at address 003B<sub>16</sub>). When these bits are "00" (high-speed mode) or "01" (middle-speed mode), XIN is selected. When these bits are "10" (low-speed mode), XCIN is selected.

**• Prescaler 12**

The prescaler 12 counts the output of the timer divider. The count source is selected by the timer 12, X count source selection register among 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512, 1/1024 of  $f(XIN)$  or  $f(XCIN)$ .

**• Timer 1 and Timer 2**

The timer 1 and timer 2 counts the output of prescaler 12 and periodically set the interrupt request bit.

**• Prescaler X and prescaler Y**

The prescaler X and prescaler Y count the output of the timer divider or  $f(XCIN)$ . The count source is selected by the timer 12, X count source selection register (address 000E<sub>16</sub>) and the timer Y, Z count source selection register (address 000F<sub>16</sub>) among 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512, and 1/1024 of  $f(XIN)$  or  $f(XCIN)$ ; and  $f(XCIN)$ .

**• Timer X and Timer Y**

The timer X and timer Y can each select one of four operating modes by setting the timer XY mode register (address 0023<sub>16</sub>).

**(1) Timer mode****• Mode selection**

This mode can be selected by setting "00" to the timer X operating mode bits (bits 1 and 0) and the timer Y operating mode bits (bits 5 and 4) of the timer XY mode register (address 0023<sub>16</sub>).

**• Explanation of operation**

The timer count operation is started by setting "0" to the timer X count stop bit (bit 3) and the timer Y count stop bit (bit 7) of the timer XY mode register (address 0023<sub>16</sub>).

When the timer reaches "00<sub>16</sub>", an underflow occurs at the next count pulse and the contents of timer latch are reloaded into the timer and the count is continued.

**(2) Pulse Output Mode****• Mode selection**

This mode can be selected by setting "01" to the timer X operating mode bits (bits 1 and 0) and the timer Y operating mode bits (bits 5 and 4) of the timer XY mode register (address 0023<sub>16</sub>).

**• Explanation of operation**

The operation is the same as the timer mode's. Moreover the pulse which is inverted each time the timer underflows is output from CNTR0/CNTR1 pin. Regardless of the timer counting or not the output of CNTR0/CNTR1 pin is initialized to the level of specified by their active edge switch bits when writing to the timer. When the CNTR0 active edge switch bit (bit 2) and the CNTR1 active edge switch bit (bit 6) of the timer XY mode register (address 0023<sub>16</sub>) is "0", the output starts with "H" level. When it is "1", the output starts with "L" level.

Switching the CNTR0 or CNTR1 active edge switch bit will reverse the output level of the corresponding CNTR0 or CNTR1 pin.

**• Precautions**

Set the double-function port of CNTR0/CNTR1 pin and port P54/P55 to output in this mode.

**(3) Event Counter Mode****• Mode selection**

This mode can be selected by setting "10" to the timer X operating mode bits (bits 1 and 0) and the timer Y operating mode bits (bits 5 and 4) of the timer XY mode register (address 0023<sub>16</sub>).

**• Explanation of operation**

The operation is the same as the timer mode's except that the timer counts signals input from the CNTR0 or CNTR1 pin. The valid edge for the count operation depends on the CNTR0 active edge switch bit (bit 2) or the CNTR1 active edge switch bit (bit 6) of the timer XY mode register (address 0023<sub>16</sub>). When it is "0", the rising edge is valid. When it is "1", the falling edge is valid.

**• Precautions**

Set the double-function port of CNTR0/CNTR1 pin and port P54/P55 to input in this mode.

#### (4) Pulse Width Measurement Mode

- Mode selection

This mode can be selected by setting “11” to the timer X operating mode bits (bits 1 and 0) and the timer Y operating mode bits (bits 5 and 4) of the timer XY mode register (address 0023<sub>16</sub>).

- Explanation of operation

When the CNTR0 active edge switch bit (bit 2) or the CNTR1 active edge switch bit (bit 6) of the timer XY mode register (address 0023<sub>16</sub>) is “1”, the timer counts during the term of one falling edge of CNTR0/CNTR1 pin input until the next rising edge of input (“L” term). When it is “0”, the timer counts during the term of one rising edge input until the next falling edge input (“H” term).

- Precautions

Set the double-function port of CNTR0/CNTR1 pin and port P54/P55 to input in this mode.

The count operation can be stopped by setting “1” to the timer X count stop bit (bit 3) and the timer Y count stop bit (bit 7) of the timer XY mode register (address 0023<sub>16</sub>). The interrupt request bit is set to “1” each time the timer underflows.

- Precautions when switching count source

When switching the count source by the timer 12, X and Y count source selection bits, the value of timer count is altered in inconsiderable amount owing to generating of thin pulses on the count input signals.

Therefore, select the timer count source before setting the value to the prescaler and the timer.

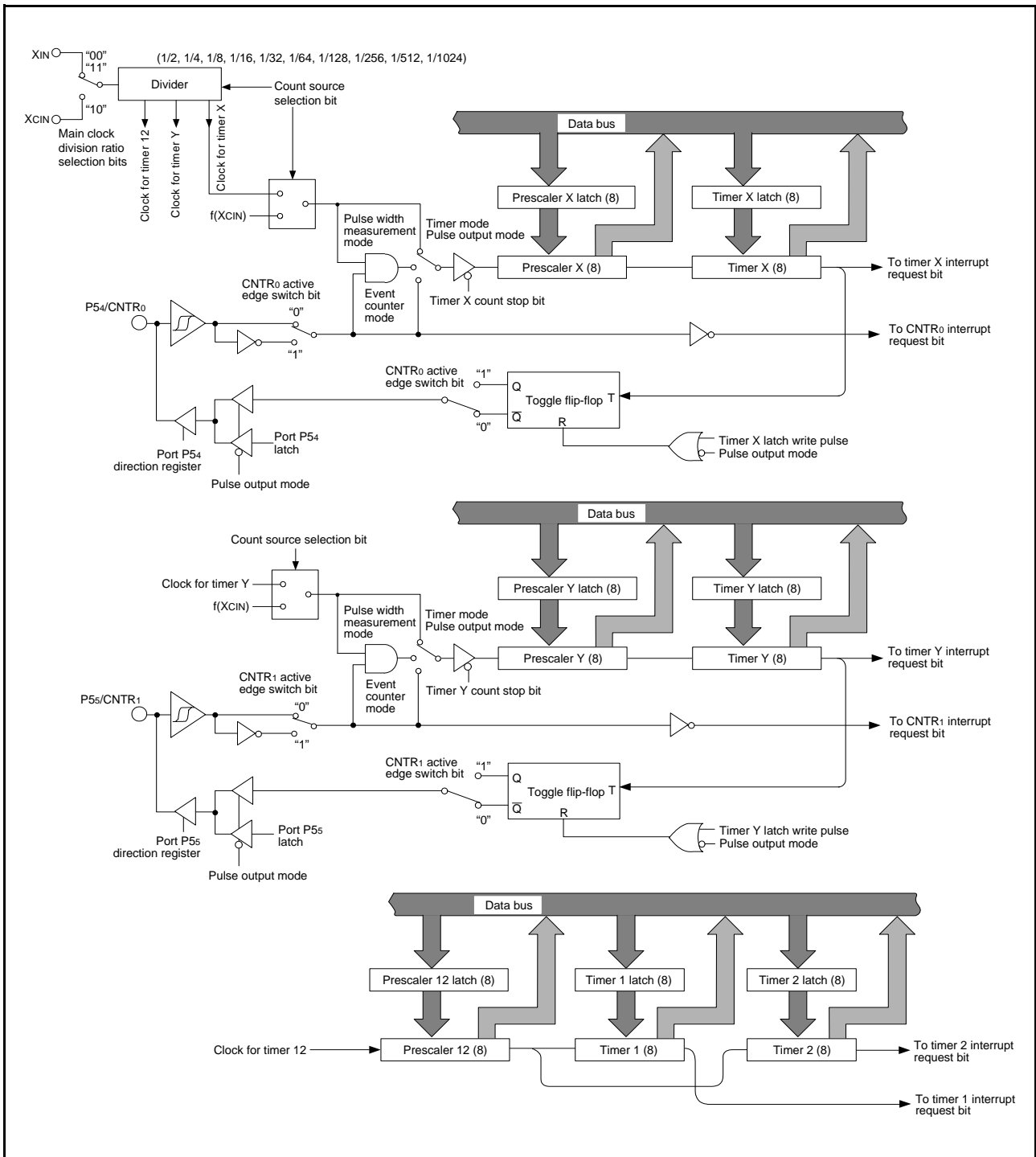


Fig 21. Block diagram of timer X, timer Y, timer 1, and timer 2

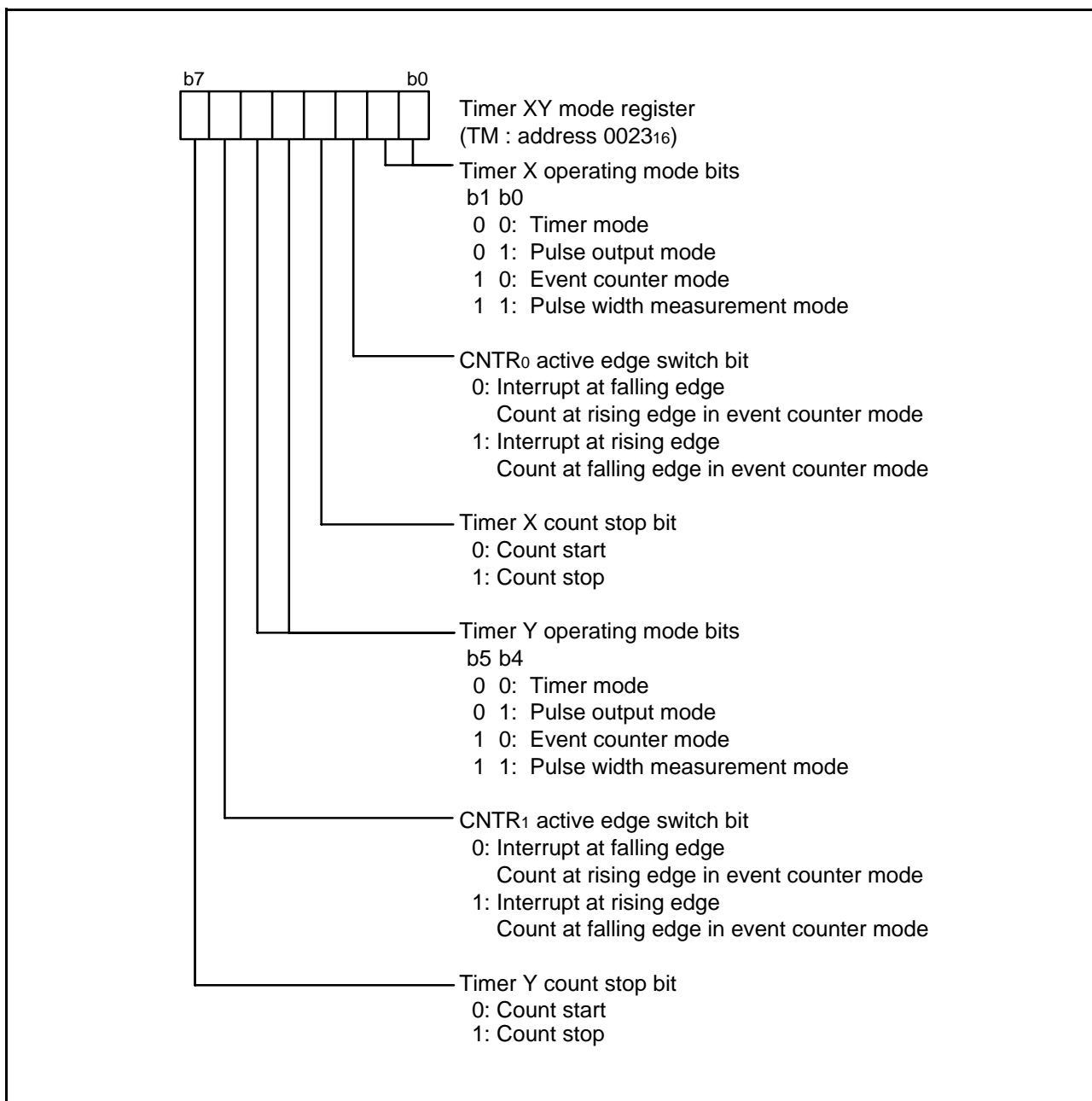


Fig 22. Structure of timer XY mode register



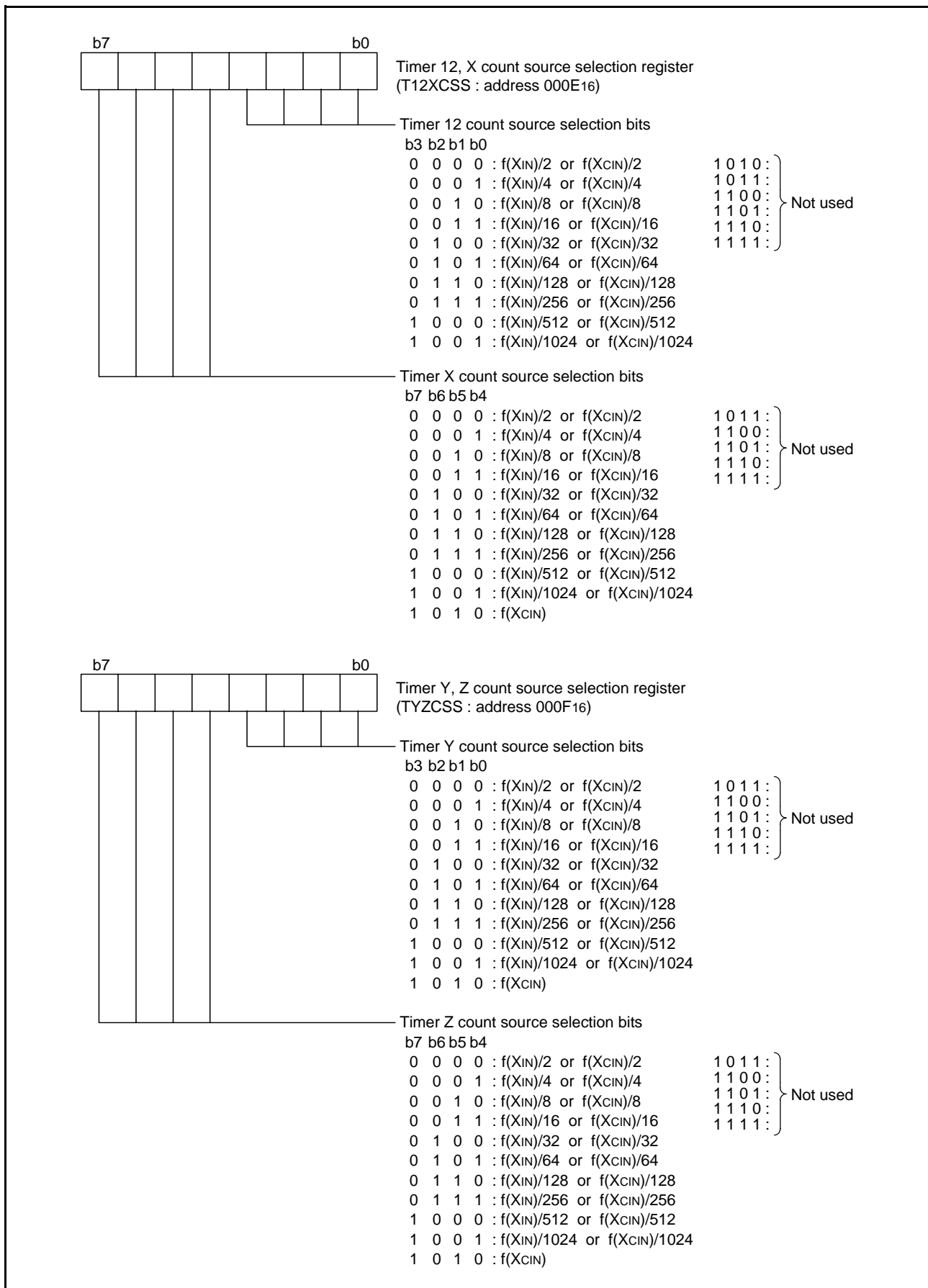


Fig 23. Structure of timer 12, X and timer Y, Z count source selection registers

**• 16-bit Timer**

The timer Z is a 16-bit timer. When the timer reaches “0000<sub>16</sub>”, an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When the timer underflows, the interrupt request bit corresponding to the timer Z is set to “1”.

When reading/writing to the timer Z, perform reading/writing to both the high-order byte and the low-order byte. When reading the timer Z, read from the high-order byte first, followed by the low-order byte. Do not perform the writing to the timer Z between read operation of the high-order byte and read operation of the low-order byte. When writing to the timer Z, write to the low-order byte first, followed by the high-order byte. Do not perform the reading to the timer Z between write operation of the low-order byte and write operation of the high-order byte.

The timer Z can select the count source by the timer Z count source selection bits of timer Y, Z count source selection register (bits 7 to 4 at address 000F<sub>16</sub>).

Timer Z can select one of seven operating modes by setting the timer Z mode register (address 002A<sub>16</sub>).

**(1) Timer mode****• Mode selection**

This mode can be selected by setting “000” to the timer Z operating mode bits (bits 2 to 0) and setting “0” to the timer/event counter mode switch bit (b7) of the timer Z mode register (address 002A<sub>16</sub>).

**• Count source selection**

In high- or middle-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(XIN); or f(XCIN) can be selected as the count source.

In low-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(XCIN); or f(XCIN) can be selected as the count source.

**• Interrupt**

When an underflow occurs, the INT0/timer Z interrupt request bit (bit 0) of the interrupt request register 1 (address 003C<sub>16</sub>) is set to “1”.

**• Explanation of operation**

During timer stop, usually write data to a latch and a timer at the same time to set the timer value.

The timer count operation is started by setting “0” to the timer Z count stop bit (bit 6) of the timer Z mode register (address 002A<sub>16</sub>).

When the timer reaches “0000<sub>16</sub>”, an underflow occurs at the next count pulse and the contents of timer latch are reloaded into the timer and the count is continued.

When writing data to the timer during operation, the data is written only into the latch. Then the new latch value is reloaded into the timer at the next underflow.

**(2) Event counter mode****• Mode selection**

This mode can be selected by setting “000” to the timer Z operating mode bits (bits 2 to 0) and setting “1” to the timer/event counter mode switch bit (bit 7) of the timer Z mode register (address 002A<sub>16</sub>).

The valid edge for the count operation depends on the CNTR2 active edge switch bit (bit 5) of the timer Z mode register (address 002A<sub>16</sub>). When it is “0”, the rising edge is valid. When it is “1”, the falling edge is valid.

**• Interrupt**

The interrupt at an underflow is the same as the timer mode's.

**• Explanation of operation**

The operation is the same as the timer mode's.

Set the double-function port of CNTR2 pin and port P47 to input in this mode.

Figure.26 shows the timing chart of the timer/event counter mode.

**(3) Pulse output mode****• Mode selection**

This mode can be selected by setting “001” to the timer Z operating mode bits (bits 2 to 0) and setting “0” to the timer/event counter mode switch bit (b7) of the timer Z mode register (address 002A<sub>16</sub>).

**• Count source selection**

In high- or middle-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(XIN); or f(XCIN) can be selected as the count source.

In low-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(XCIN); or f(XCIN) can be selected as the count source.

**• Interrupt**

The interrupt at an underflow is the same as the timer mode's.

**• Explanation of operation**

The operation is the same as the timer mode's. Moreover the pulse which is inverted each time the timer underflows is output from CNTR2 pin. When the CNTR2 active edge switch bit (bit 5) of the timer Z mode register (address 002A<sub>16</sub>) is “0”, the output starts with “H” level. When it is “1”, the output starts with “L” level.

**• Precautions**

The double-function port of CNTR2 pin and port P47 is automatically set to the timer pulse output port in this mode.

The output from CNTR2 pin is initialized to the level depending on CNTR2 active edge switch bit by writing to the timer.

When the value of the CNTR2 active edge switch bit is changed, the output level of CNTR2 pin is inverted.

Figure.27 shows the timing chart of the pulse output mode.

**(4) Pulse period measurement mode**

## • Mode selection

This mode can be selected by setting “010” to the timer Z operating mode bits (bits 2 to 0) and setting “0” to the timer/event counter mode switch bit (b7) of the timer Z mode register (address 002A16).

## • Count source selection

In high- or middle-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(XIN); or f(XCIN) can be selected as the count source.

In low-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(XCIN); or f(XCIN) can be selected as the count source.

## • Interrupt

The interrupt at an underflow is the same as the timer mode's. When the pulse period measurement is completed, the INT4/CNTR2 interrupt request bit (bit 5) of the interrupt request register 2 (address 003D16) is set to “1”.

## • Explanation of operation

The cycle of the pulse which is input from the CNTR2 pin is measured. When the CNTR2 active edge switch bit (bit 5) of the timer Z mode register (address 002A16) is “0”, the timer counts during the term from one falling edge of CNTR2 pin input to the next falling edge. When it is “1”, the timer counts during the term from one rising edge input to the next rising edge input.

When the valid edge of measurement completion/start is detected, the 1's complement of the timer value is written to the timer latch and “FFFF16” is set to the timer.

Furthermore when the timer underflows, the timer Z interrupt request occurs and “FFFF16” is set to the timer. When reading the timer Z, the value of the timer latch (measured value) is read. The measured value is retained until the next measurement completion.

## • Precautions

Set the double-function port of CNTR2 pin and port P47 to input in this mode.

A read-out of timer value is impossible in this mode. The timer can be written to only during timer stop (no measurement of pulse period).

Since the timer latch in this mode is specialized for the read-out of measured values, do not perform any write operation during measurement.

“FFFF16” is set to the timer when the timer underflows or when the valid edge of measurement start/completion is detected. Consequently, the timer value at start of pulse period measurement depends on the timer value just before measurement start.

Figure.28 shows the timing chart of the pulse period measurement mode.

**(5) Pulse width measurement mode**

## • Mode selection

This mode can be selected by setting “011” to the timer Z operating mode bits (bits 2 to 0) and setting “0” to the timer/event counter mode switch bit (b7) of the timer Z mode register (address 002A16).

## • Count source selection

In high- or middle-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(XIN); or f(XCIN) can be selected as the count source.

In low-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(XCIN); or f(XCIN) can be selected as the count source.

## • Interrupt

The interrupt at an underflow is the same as the timer mode's. When the pulse widths measurement is completed, the INT4/CNTR2 interrupt request bit (bit 5) of the interrupt request register 2 (address 003D16) is set to “1”.

## • Explanation of operation

The pulse width which is input from the CNTR2 pin is measured. When the CNTR2 active edge switch bit (bit 5) of the timer Z mode register (address 002A16) is “0”, the timer counts during the term from one rising edge input to the next falling edge input (“H” term). When it is “1”, the timer counts during the term from one falling edge of CNTR2 pin input to the next rising edge of input (“L” term).

When the valid edge of measurement completion is detected, the 1's complement of the timer value is written to the timer latch.

When the valid edge of measurement completion/start is detected, “FFFF16” is set to the timer.

When the timer Z underflows, the timer Z interrupt occurs and “FFFF16” is set to the timer Z. When reading the timer Z, the value of the timer latch (measured value) is read. The measured value is retained until the next measurement completion.

## • Precautions

Set the double-function port of CNTR2 pin and port P47 to input in this mode.

A read-out of timer value is impossible in this mode. The timer can be written to only during timer stop (no measurement of pulse widths).

Since the timer latch in this mode is specialized for the read-out of measured values, do not perform any write operation during measurement.

“FFFF16” is set to the timer when the timer underflows or when the valid edge of measurement start/completion is detected. Consequently, the timer value at start of pulse width measurement depends on the timer value just before measurement start.

Figure.29 shows the timing chart of the pulse width measurement mode.

**(6) Programmable waveform generating mode**

## • Mode selection

This mode can be selected by setting “100” to the timer Z operating mode bits (bits 2 to 0) and setting “0” to the timer/event counter mode switch bit (b7) of the timer Z mode register (address 002A16).

## • Count source selection

In high- or middle-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(XIN); or f(XCIN) can be selected as the count source.

In low-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(XCIN); or f(XCIN) can be selected as the count source.

## • Interrupt

The interrupt at an underflow is the same as the timer mode's.

## • Explanation of operation

The operation is the same as the timer mode's. Moreover the timer outputs the data set in the output level latch (bit 4) of the timer Z mode register (address 002A16) from the CNTR2 pin each time the timer underflows.

Changing the value of the output level latch and the timer latch after an underflow makes it possible to output an optional waveform from the CNTR2 pin.

## • Precautions

The double-function port of CNTR2 pin and port P47 is automatically set to the programmable waveform generating port in this mode.

Figure.30 shows the timing chart of the programmable waveform generating mode.

**(7) Programmable one-shot generating mode**

## • Mode selection

This mode can be selected by setting “101” to the timer Z operating mode bits (bits 2 to 0) and setting “0” to the timer/event counter mode switch bit (b7) of the timer Z mode register (address 002A16).

## • Count source selection

In high- or middle-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(XIN); or f(XCIN) can be selected as the count source.

## • Interrupt

The interrupt at an underflow is the same as the timer mode's.

The trigger to generate one-shot pulse can be selected by the INT1 active edge selection bit (bit 1) of the interrupt edge selection register (address 003A16). When it is “0”, the falling edge active is selected; when it is “1”, the rising edge active is selected.

When the valid edge of the INT1 pin is detected, the INT1 interrupt request bit (bit 1) of the interrupt request register 1 (address 003C16) is set to “1”.

## • Explanation of operation

## 1. “H” one-shot pulse; Bit 5 of timer Z mode register = “0”

The output level of the CNTR2 pin is initialized to “L” at mode selection. When trigger generation (input signal to INT1 pin) is detected, “H” is output from the CNTR2 pin. When an underflow occurs, “L” is output. The “H” one-shot pulse width is set by the setting value to the timer Z register low-order and high-order. When trigger generating is detected during timer count stop, although “H” is output from the CNTR2 pin, “H” output state continues because an underflow does not occur.

## 2. “L” one-shot pulse; Bit 5 of timer Z mode register = “1”

The output level of the CNTR2 pin is initialized to “H” at mode selection. When trigger generation (input signal to INT1 pin) is detected, “L” is output from the CNTR2 pin. When an underflow occurs, “H” is output. The “L” one-shot pulse width is set by the setting value to the timer Z low-order and high-order. When trigger generating is detected during timer count stop, although “L” is output from the CNTR2 pin, “L” output state continues because an underflow does not occur.

## • Precautions

Set the double-function port of INT1 pin and port P42 to input in this mode.

The double-function port of CNTR2 pin and port P47 is automatically set to the programmable one-shot generating port in this mode.

This mode cannot be used in low-speed mode.

If the value of the CNTR2 active edge switch bit is changed during one-shot generating enabled or generating one-shot pulse, then the output level from CNTR2 pin changes.

Figure.31 shows the timing chart of the programmable one-shot generating mode.

**<Notes regarding all modes>**

## • Timer Z write control

Which write control can be selected by the timer Z write control bit (bit 3) of the timer Z mode register (address 002A16), writing data to both the latch and the timer at the same time or writing data only to the latch.

When the operation “writing data only to the latch” is selected, the value is set to the timer latch by writing data to the address of timer Z and the timer is updated at next underflow. After reset release, the operation “writing data to both the latch and the timer at the same time” is selected, and the value is set to both the latch and the timer at the same time by writing data to the address of timer Z.

In the case of writing data only to the latch, if writing data to the latch and an underflow are performed almost at the same time, the timer value may become undefined.

## • Timer Z read control

A read-out of timer value is impossible in pulse period measurement mode and pulse width measurement mode. In the other modes, a read-out of timer value is possible regardless of count operating or stopped.

However, a read-out of timer latch value is impossible.

## • Switch of interrupt active edge of CNTR2 and INT1

Each interrupt active edge depends on setting of the CNTR2 active edge switch bit and the INT1 active edge selection bit.

## • Switch of count source

When switching the count source by the timer Z count source selection bits, the value of timer count is altered in inconsiderable amount owing to generating of thin pulses on the count input signals.

Therefore, select the timer count source before setting the value to the prescaler and the timer.

## • Usage of CNTR2 pin as normal I/O port P47

To use the CNTR2 pin as normal I/O port P47, set timer Z operating mode bits (b2, b1, b0) of timer Z mode register (address 002A16) to “000”.

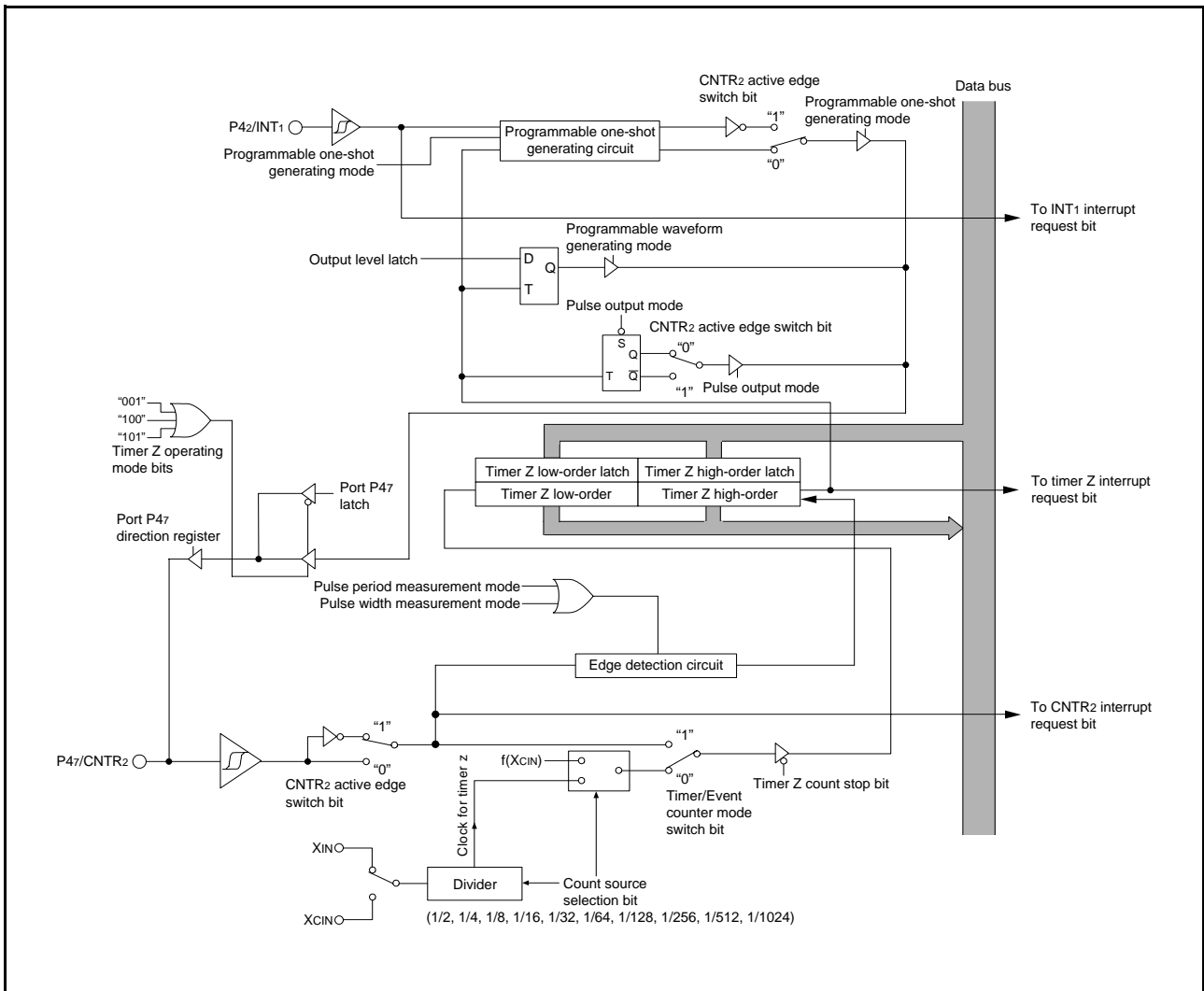


Fig 24. Block diagram of timer Z

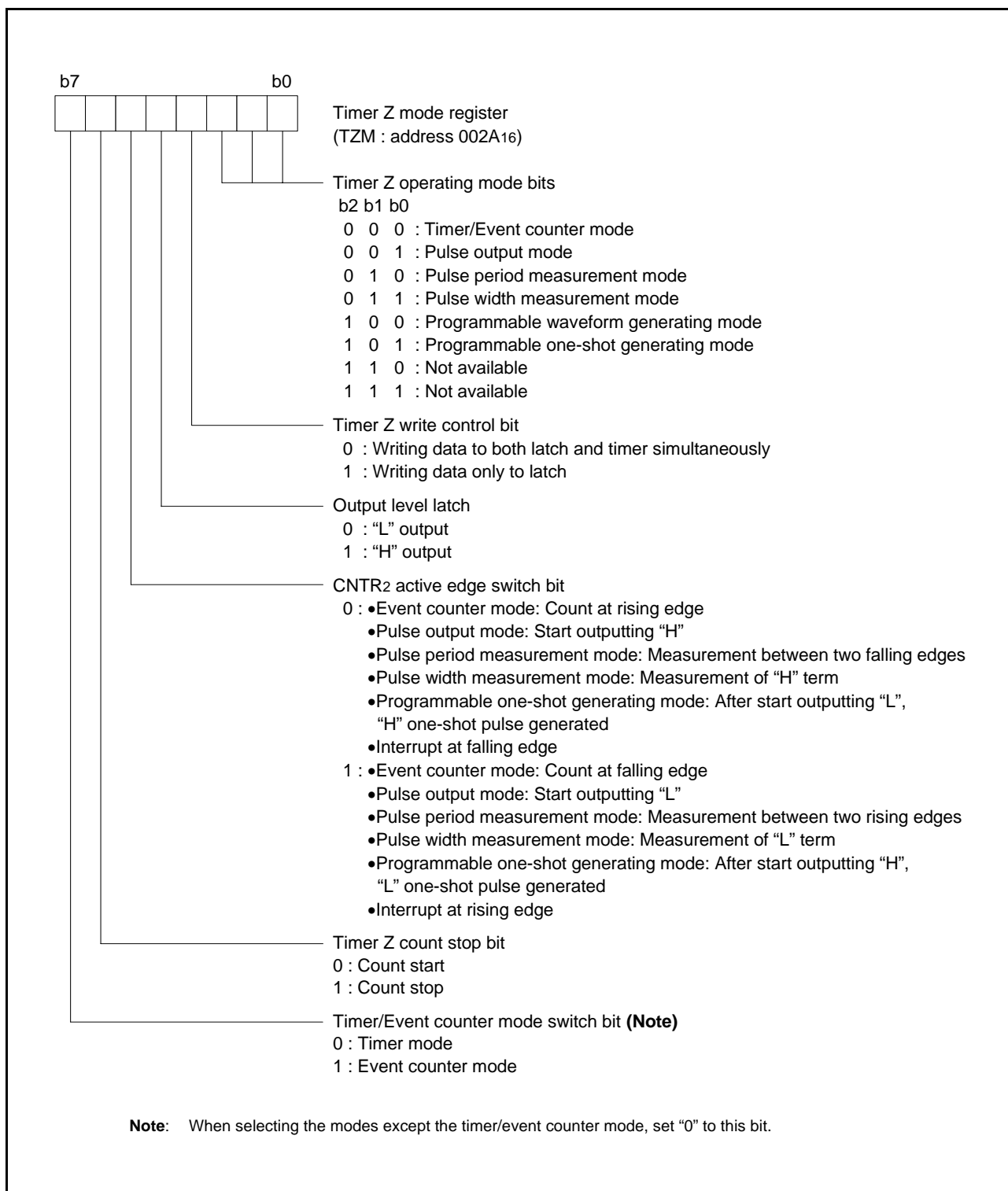


Fig 25. Structure of timer Z mode register

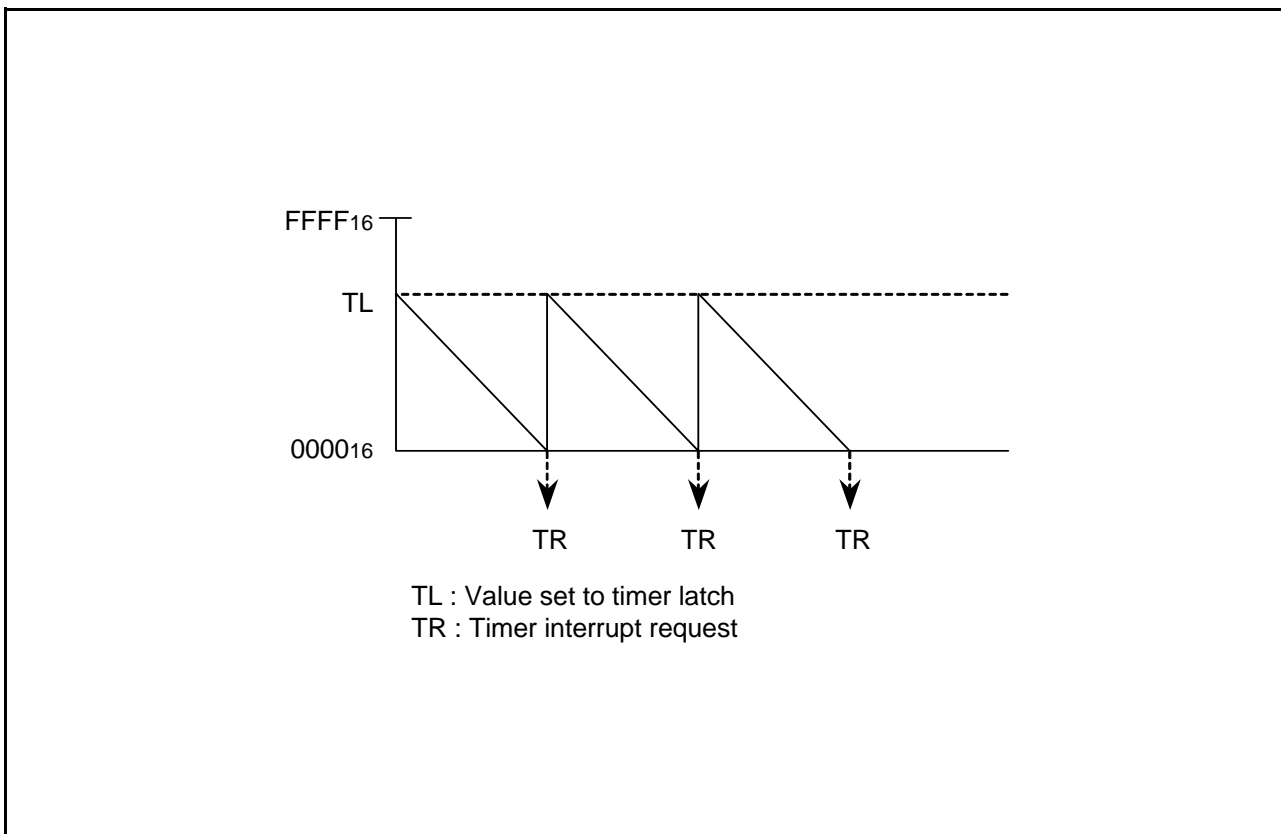


Fig 26. Timing chart of timer/event counter mode

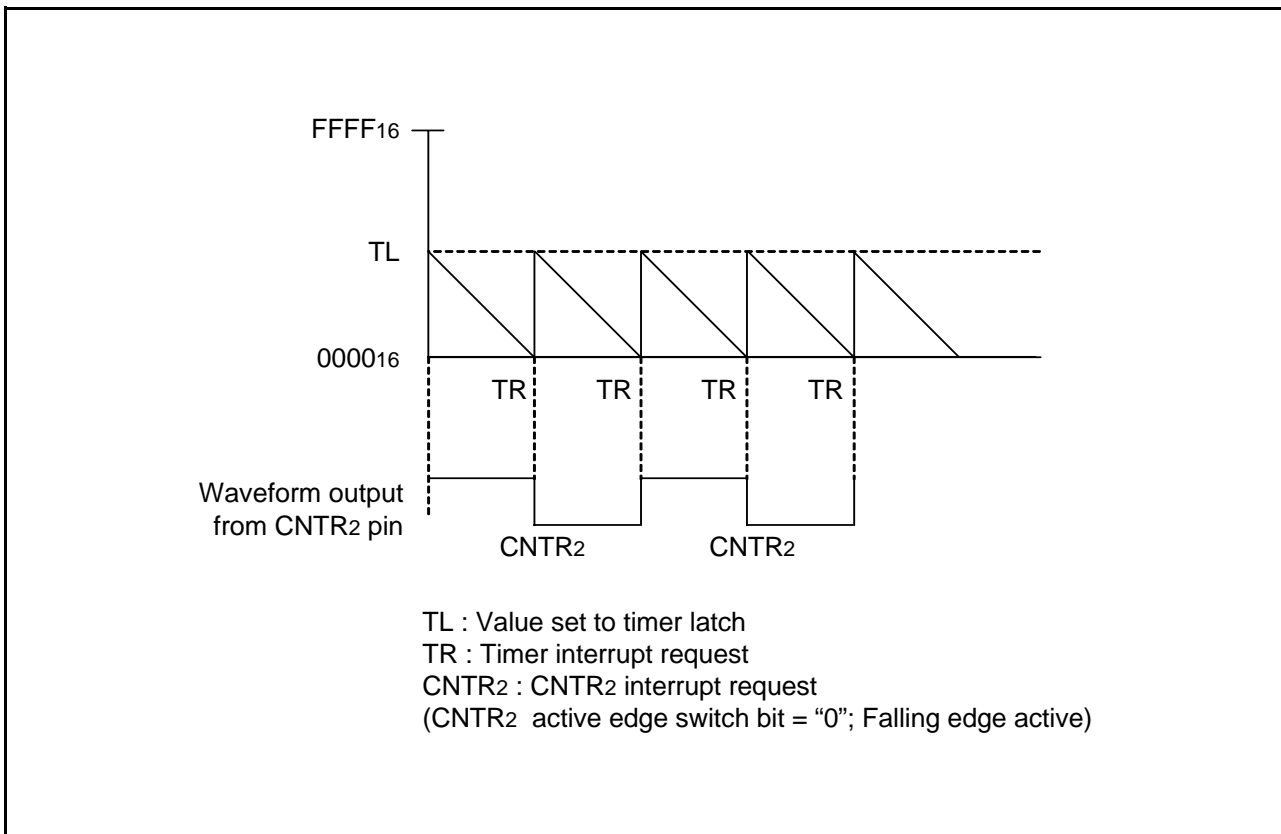


Fig 27. Timing chart of pulse output mode

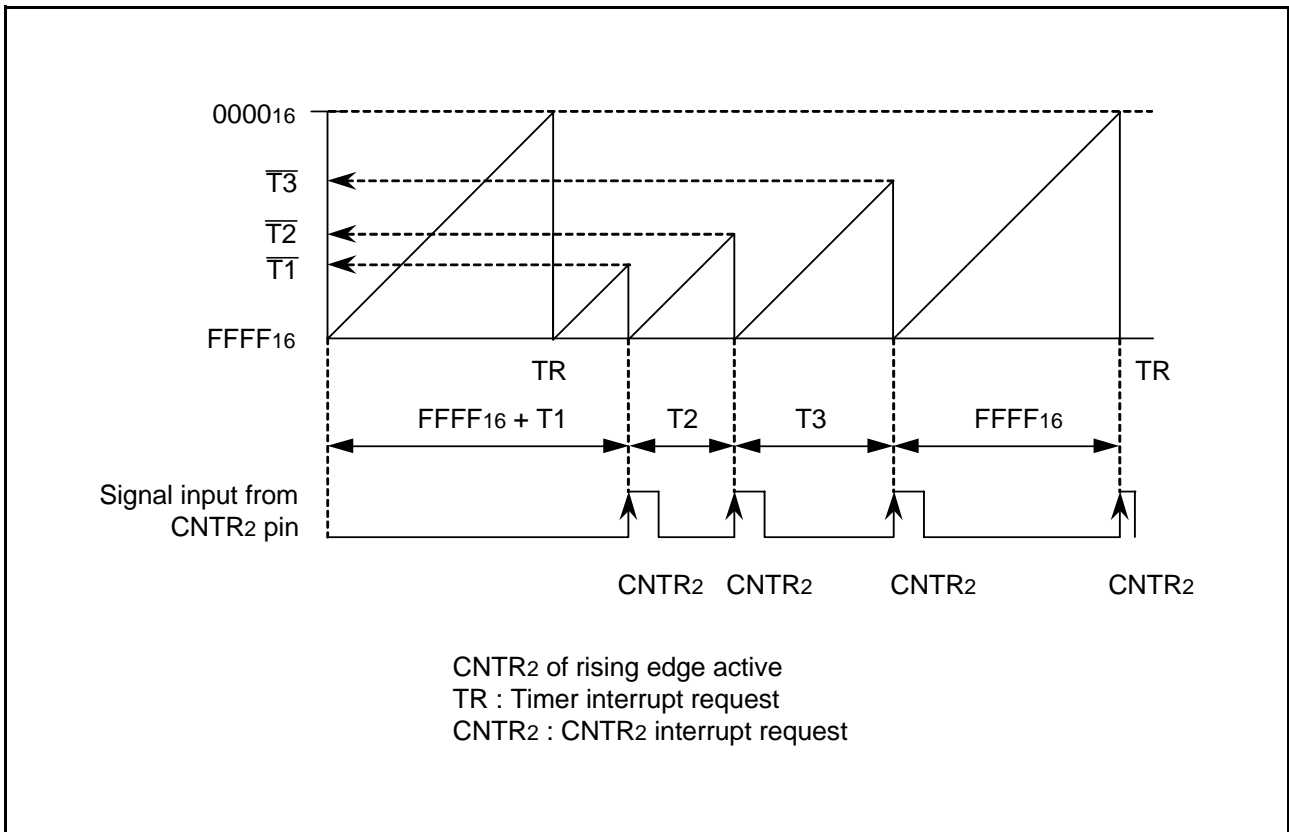


Fig 28. Timing chart of pulse period measurement mode (Measuring term between two rising edges)

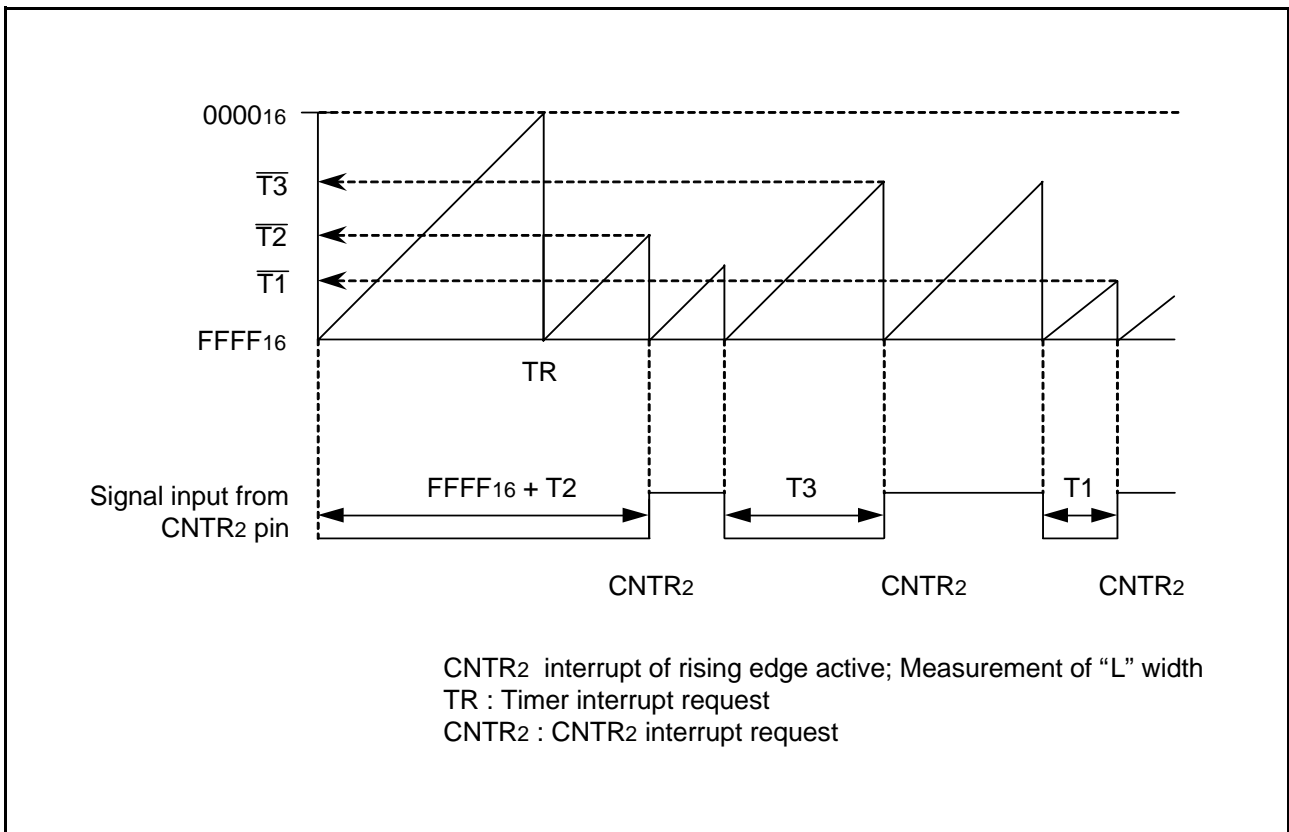


Fig 29. Timing chart of pulse width measurement mode (Measuring "L" term)



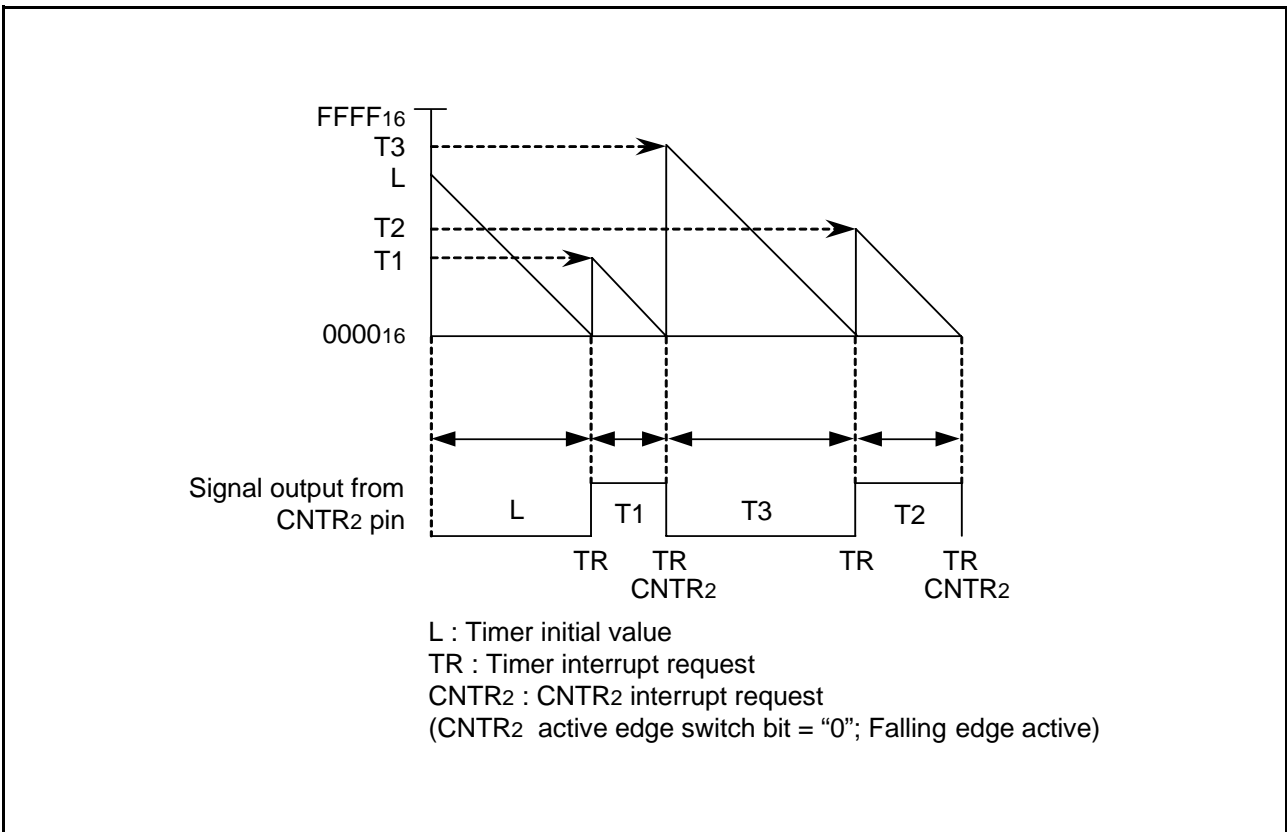


Fig 30. Timing chart of programmable waveform generating mode

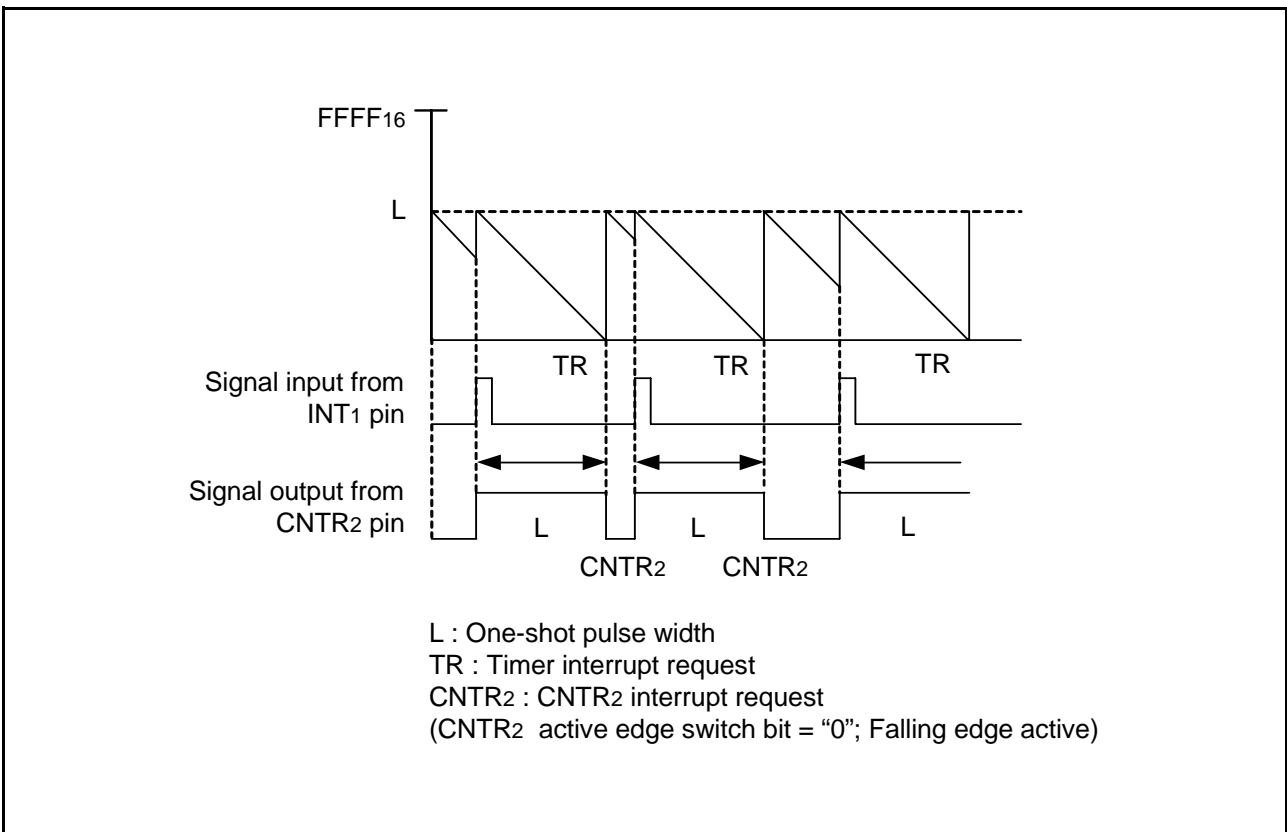


Fig 31. Timing chart of programmable one-shot generating mode ("H" one-shot pulse generating)

**SERIAL INTERFACE**

**Serial I/O1**

Serial I/O1 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

**(1) Clock Synchronous Serial I/O Mode**

Clock synchronous serial I/O1 mode can be selected by setting the serial I/O1 mode selection bit of the serial I/O1 control register (bit 6 of address 001A16) to "1".

For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the transmit/receive buffer register.

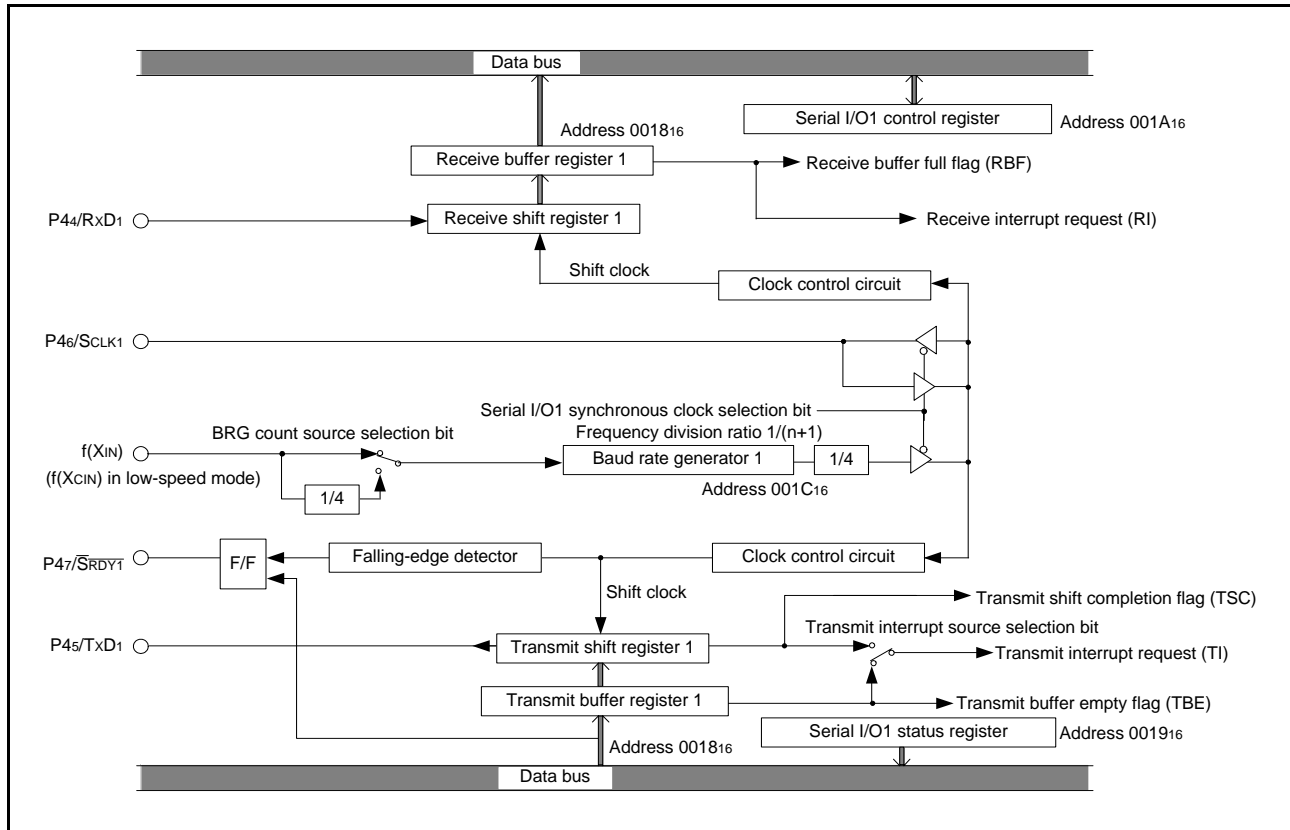


Fig 32. Block diagram of clock synchronous serial I/O1

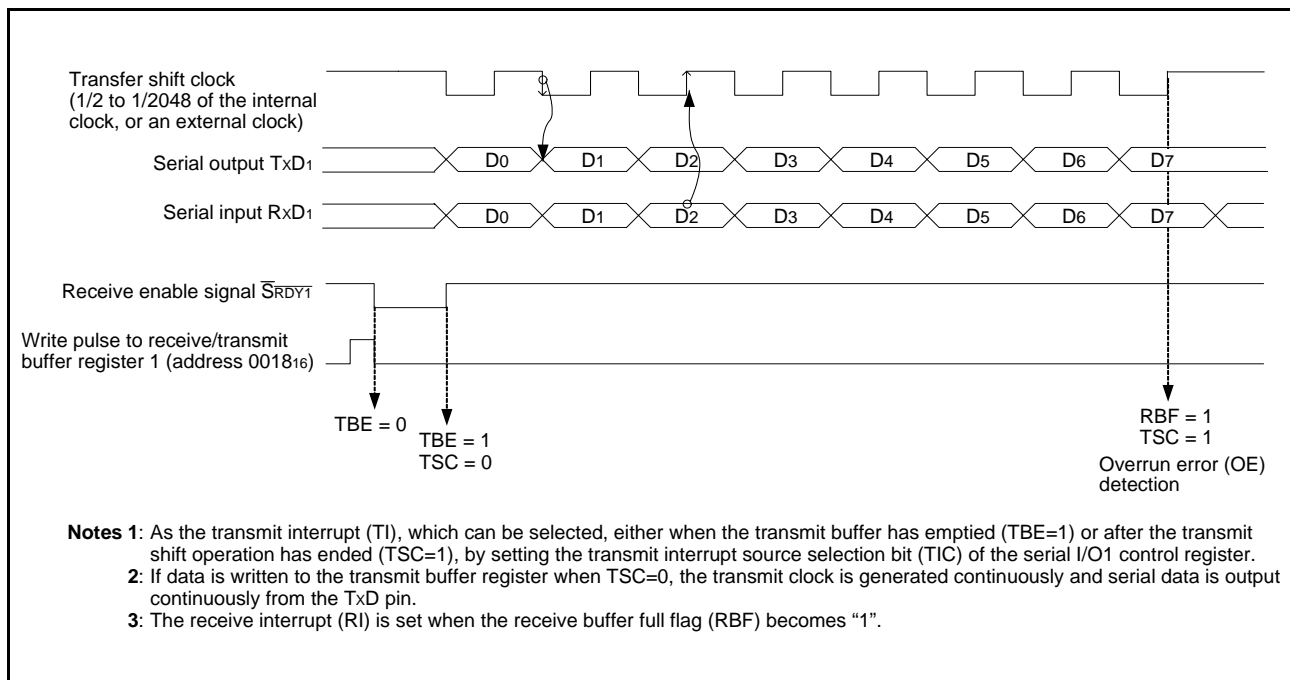


Fig 33. Operation of clock synchronous serial I/O1

**(2) Asynchronous Serial I/O (UART) Mode**

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O1 mode selection bit (b6) of the serial I/O1 control register to "0".

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the two buffers have the same address in a memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register.

The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

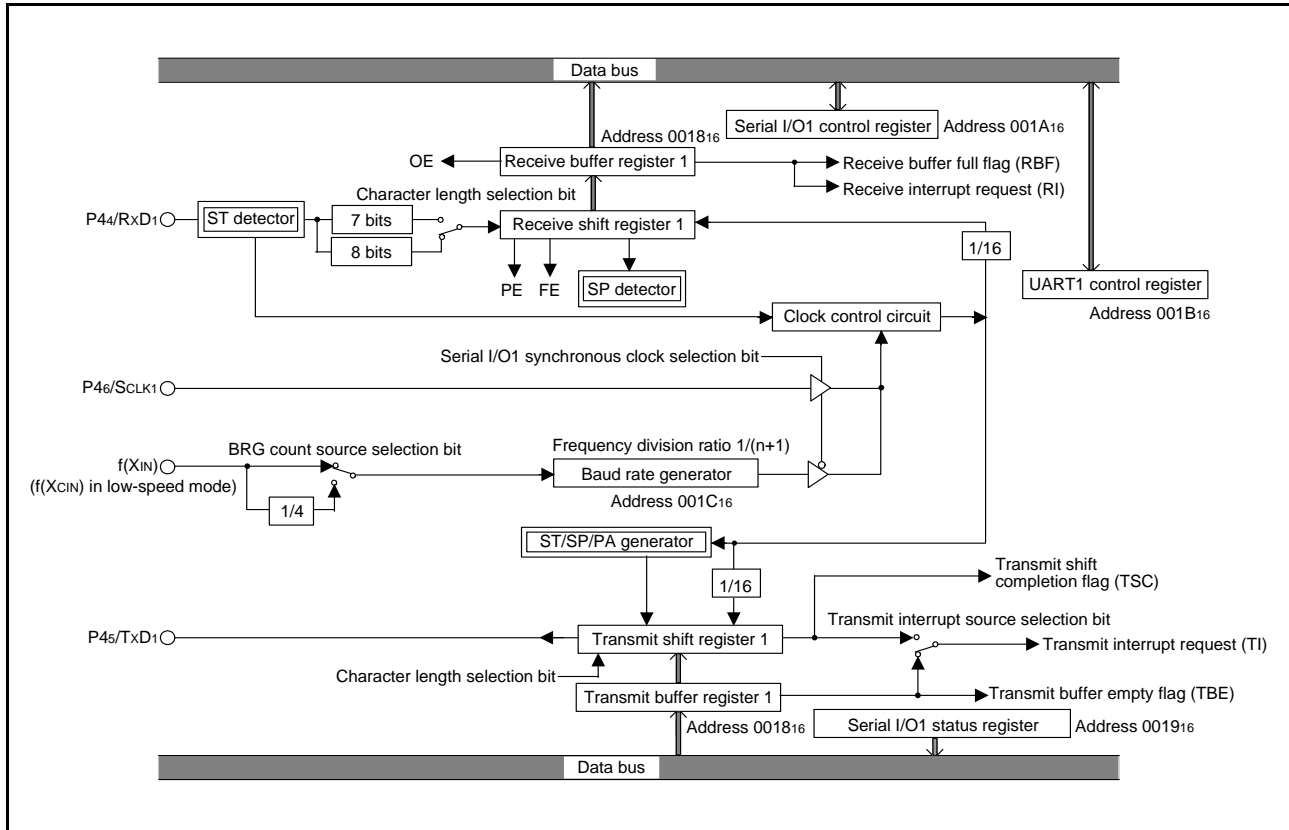


Fig 34. Block diagram of UART serial I/O1

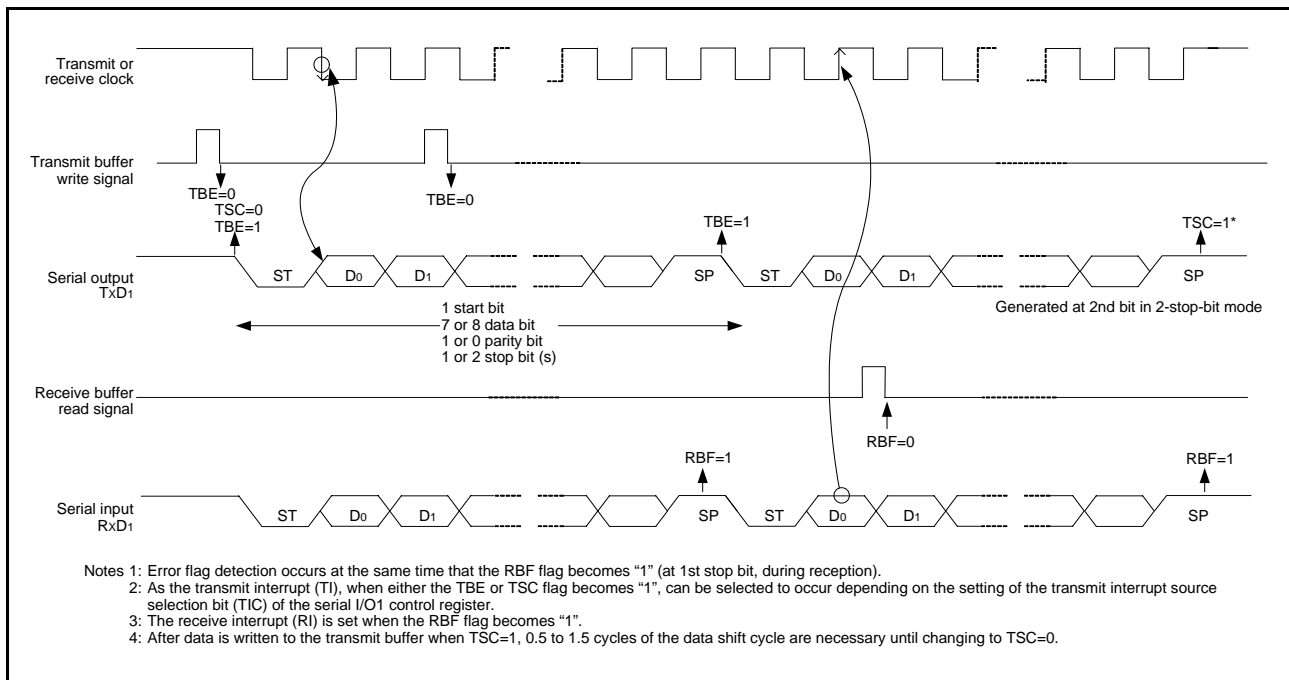


Fig 35. Operation of UART serial I/O1

**[Transmit Buffer Register 1/Receive Buffer Register 1 (TB1/RB1)] 0018<sub>16</sub>**

The transmit buffer register 1 and the receive buffer register 1 are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

**[Serial I/O1 Status Register (SIO1STS)] 0019<sub>16</sub>**

The read-only serial I/O1 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O1 function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer register is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O1 status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O1 enable bit SIOE (bit 7 of the serial I/O1 control register) also clears all the status flags, including the error flags.

Bits 0 to 6 of the serial I/O1 status register are initialized to "0" at reset, but if the transmit enable bit (bit 4) of the serial I/O1 control register has been set to "1", the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

**[Serial I/O1 Control Register (SIO1CON)] 001A<sub>16</sub>**

The serial I/O1 control register consists of eight control bits for the serial I/O1 function.

**[UART1 Control Register (UART1CON)] 001B<sub>16</sub>**

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer, and one bit (bit 4) which is always valid and sets the output structure of the P45/TxD1 pin.

**[Baud Rate Generator 1 (BRG1)] 001C<sub>16</sub>**

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by  $1/(n + 1)$ , where  $n$  is the value written to the baud rate generator.

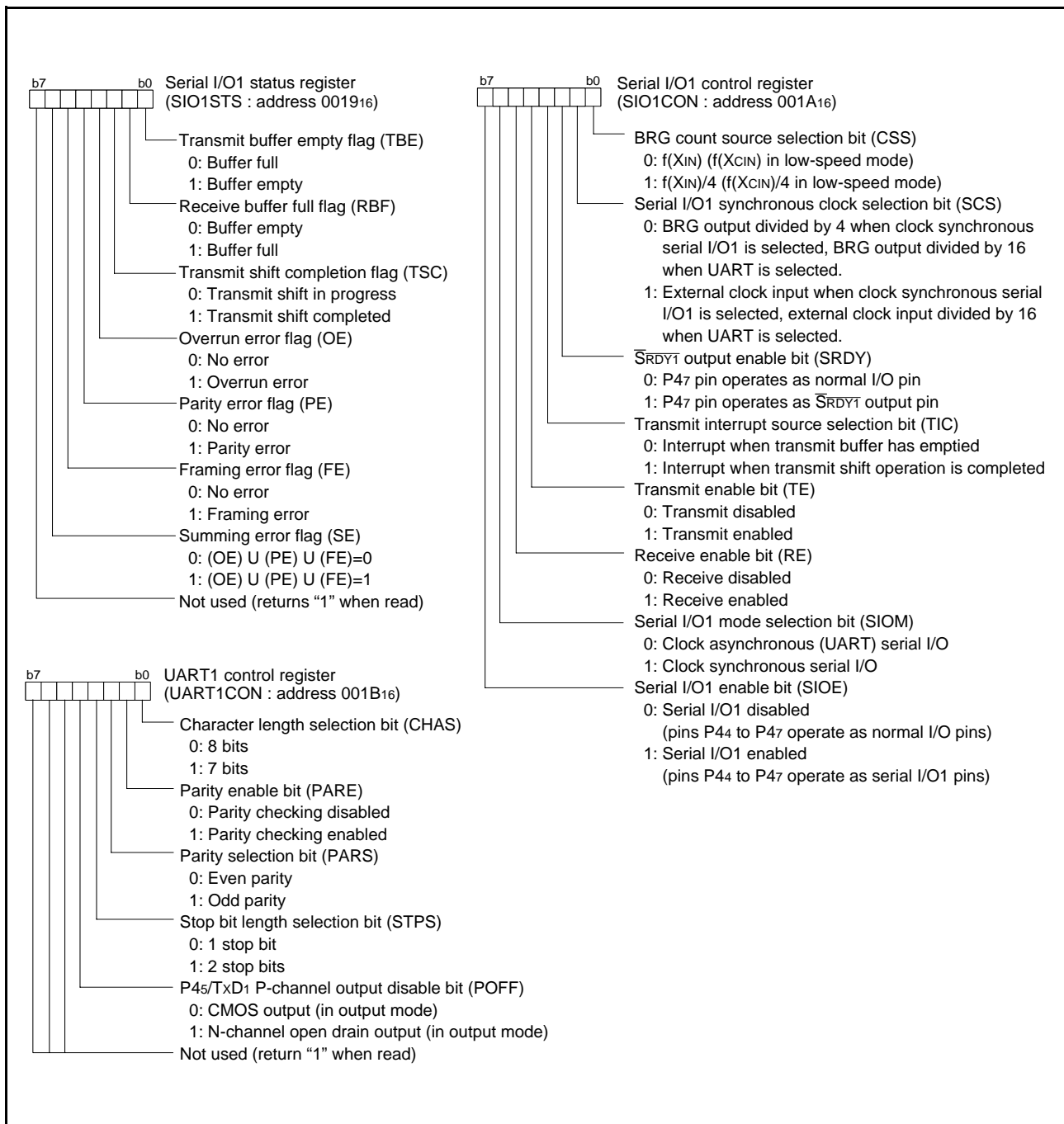


Fig 36. Structure of serial I/O1 control registers

**<Notes concerning serial I/O1>**

## 1. Notes when selecting clock synchronous serial I/O

## 1.1 Stop of transmission operation

## • Note

Clear the serial I/O1 enable bit and the transmit enable bit to “0” (serial I/O and transmit disabled).

## • Reason

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O1 enable bit is cleared to “0” (serial I/O disabled), the internal transmission is running (in this case, since pins TXD1, RXD1, SCLK1, and  $\overline{\text{SRDY1}}$  function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O1 enable bit is set to “1” at this time, the data during internally shifting is output to the TXD1 pin and an operation failure occurs.

## 1.2 Stop of receive operation

## • Note

Clear the receive enable bit to “0” (receive disabled), or clear the serial I/O1 enable bit to “0” (serial I/O disabled).

## 1.3 Stop of transmit/receive operation

## • Note

Clear both the transmit enable bit and receive enable bit to “0” (transmit and receive disabled).

(when data is transmitted and received in the clock synchronous serial I/O mode, any one of data transmission and reception cannot be stopped.)

## • Reason

In the clock synchronous serial I/O mode, the same clock is used for transmission and reception. If any one of transmission and reception is disabled, a bit error occurs because transmission and reception cannot be synchronized.

In this mode, the clock circuit of the transmission circuit also operates for data reception. Accordingly, the transmission circuit does not stop by clearing only the transmit enable bit to “0” (transmit disabled). Also, the transmission circuit is not initialized by clearing the serial I/O1 enable bit to “0” (serial I/O disabled) (refer to 1.1).

## 2. Notes when selecting clock asynchronous serial I/O

## 2.1 Stop of transmission operation

## • Note

Clear the transmit enable bit to “0” (transmit disabled). The transmission operation does not stop by clearing the serial I/O1 enable bit to “0”.

## • Reason

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O1 enable bit is cleared to “0” (serial I/O disabled), the internal transmission is running (in this case, since pins TXD1, RXD1, SCLK1, and  $\overline{\text{SRDY1}}$  function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O1 enable bit is set to “1” at this time, the data during internally shifting is output to the TXD1 pin and an operation failure occurs.

## 2.2 Stop of receive operation

## • Note

Clear the receive enable bit to “0” (receive disabled).

## 2.3 Stop of transmit/receive operation

## • Note 1 (only transmission operation is stopped)

Clear the transmit enable bit to “0” (transmit disabled). The transmission operation does not stop by clearing the serial I/O1 enable bit to “0”.

## • Reason

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O1 enable bit is cleared to “0” (serial I/O disabled), the internal transmission is running (in this case, since pins TXD1, RXD1, SCLK1, and  $\overline{\text{SRDY1}}$  function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O1 enable bit is set to “1” at this time, the data during internally shifting is output to the TXD1 pin and an operation failure occurs.

## • Note 2 (only receive operation is stopped)

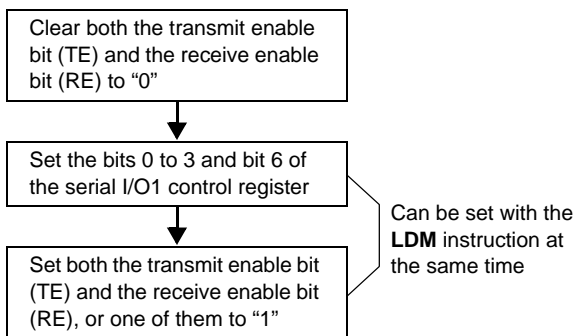
Clear the receive enable bit to “0” (receive disabled).

3.  $\overline{\text{SRDYI}}$  output of reception side

- Note  
When signals are output from the  $\overline{\text{SRDYI}}$  pin on the reception side by using an external clock in the clock synchronous serial I/O mode, set all of the receive enable bit, the  $\overline{\text{SRDYI}}$  output enable bit, and the transmit enable bit to “1” (transmit enabled).

4. Setting serial I/O1 control register again

- Note  
Set the serial I/O1 control register again after the transmission and the reception circuits are reset by clearing both the transmit enable bit and the receive enable bit to “0”.



5. Data transmission control with referring to transmit shift register completion flag

- Note  
After the transmit data is written to the transmit buffer register, the transmit shift register completion flag changes from “1” to “0” with a delay of 0.5 to 1.5 shift clocks. When data transmission is controlled with referring to the flag after writing the data to the transmit buffer register, note the delay.

6. Transmission control when external clock is selected

- Note  
When an external clock is used as the synchronous clock for data transmission, set the transmit enable bit to “1” at “H” of the SCLK1 input level. Also, write data to the transmit buffer register at “H” of the SCLK1 input level.

7. Transmit interrupt request when transmit enable bit is set

- Note  
When using the transmit interrupt, take the following sequence.
  1. Set the serial I/O1 transmit interrupt enable bit to “0” (disabled).
  2. Set the transmit enable bit to “1”.
  3. Set the serial I/O1 transmit interrupt request bit to “0” after 1 or more instruction has executed.
  4. Set the serial I/O1 transmit interrupt enable bit to “1” (enabled).

• Reason

When the transmit enable bit is set to “1”, the transmit buffer empty flag and the transmit shift register shift completion flag are also set to “1”. Therefore, regardless of selecting which timing for the generating of transmit interrupts, the interrupt request is generated and the transmit interrupt request bit is set at this point.

• Serial I/O2

The serial I/O2 function can be used only for clock synchronous serial I/O.

For clock synchronous serial I/O2, the transmitter and the receiver must use the same clock. If the internal clock is used, transfer is started by a write signal to the serial I/O2 register (address 001F16).

[Serial I/O2 Control Register (SIO2CON)] 001D16

The serial I/O2 control register contains eight bits which control various serial I/O2 functions.

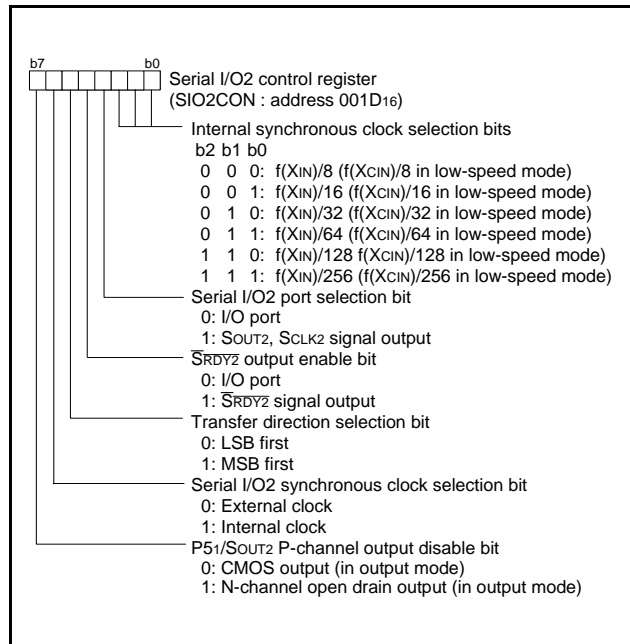


Fig 37. Structure of Serial I/O2 control register

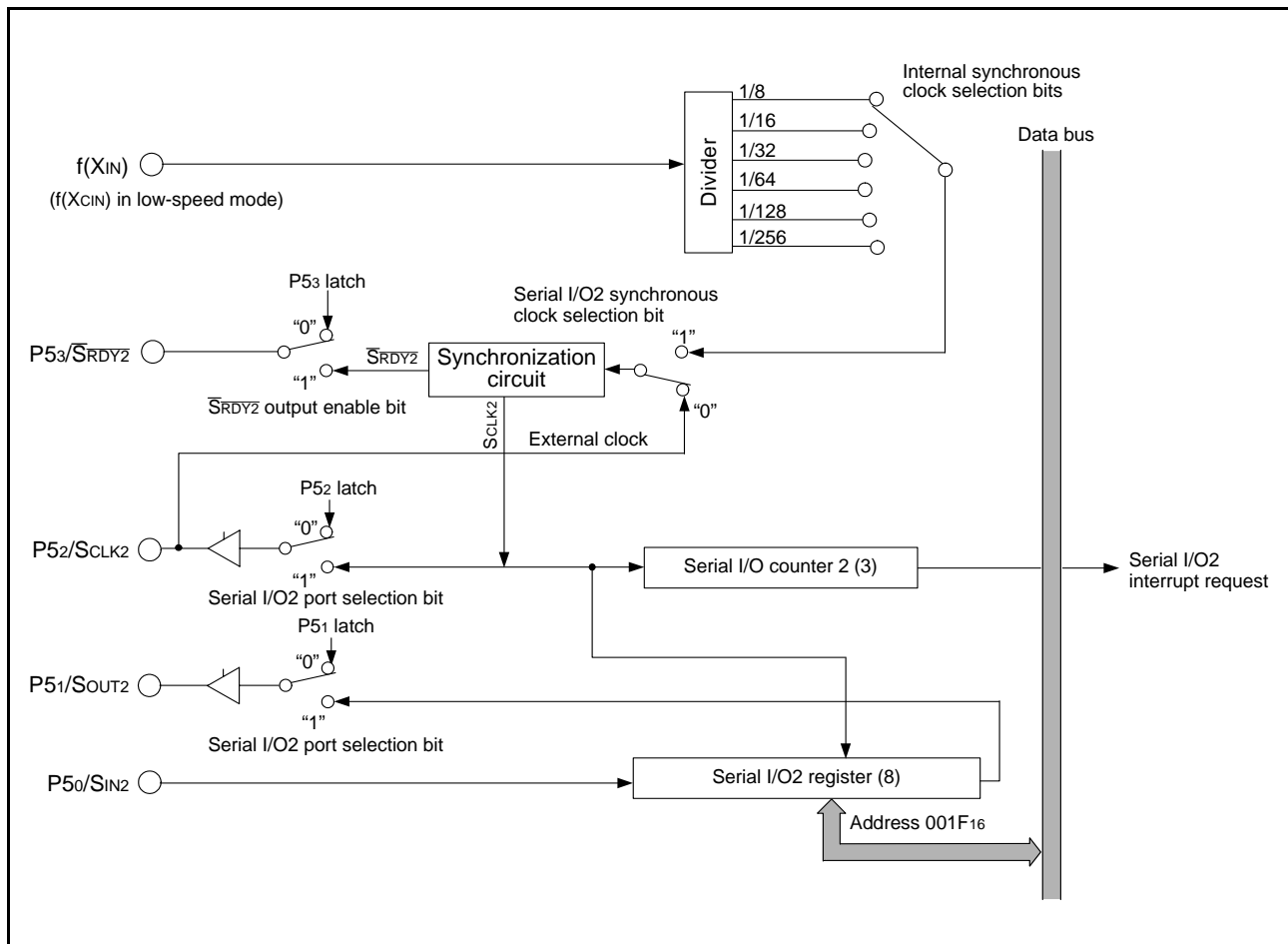


Fig 38. Block diagram of serial I/O2



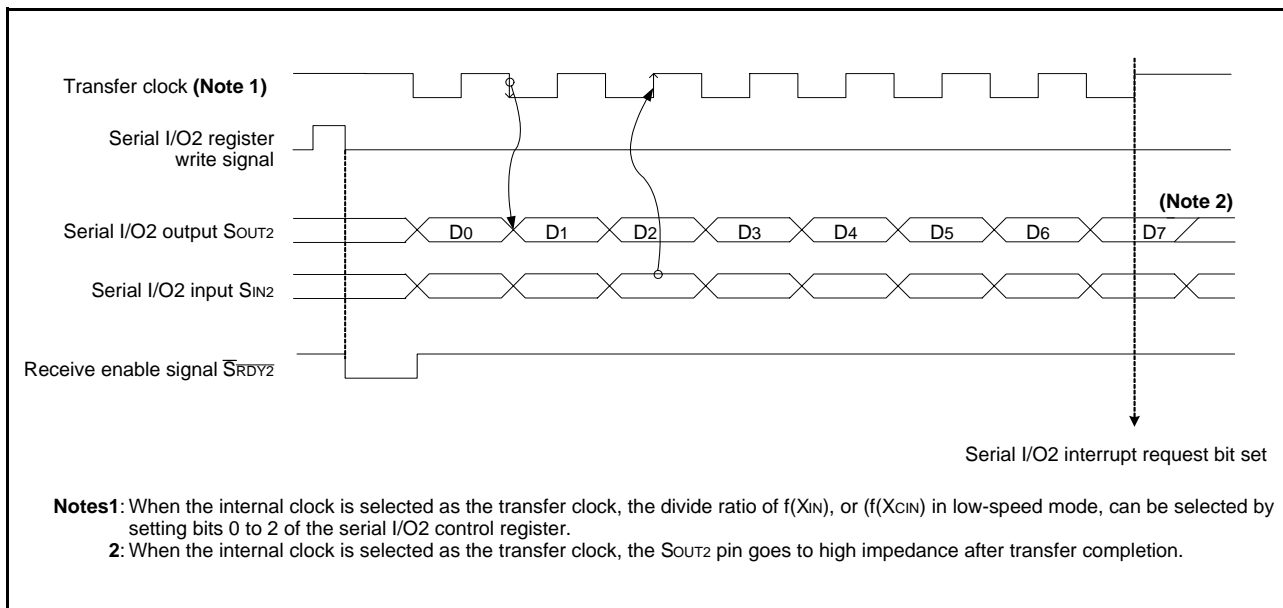


Fig 39. Timing of serial I/O2

• Serial I/O3

Serial I/O3 can be used as either clock synchronous or asynchronous (UART) serial I/O3. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O3 mode can be selected by setting the serial I/O3 mode selection bit of the serial I/O3 control register (bit 6 of address 003216) to "1".

For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the transmit/receive buffer register.

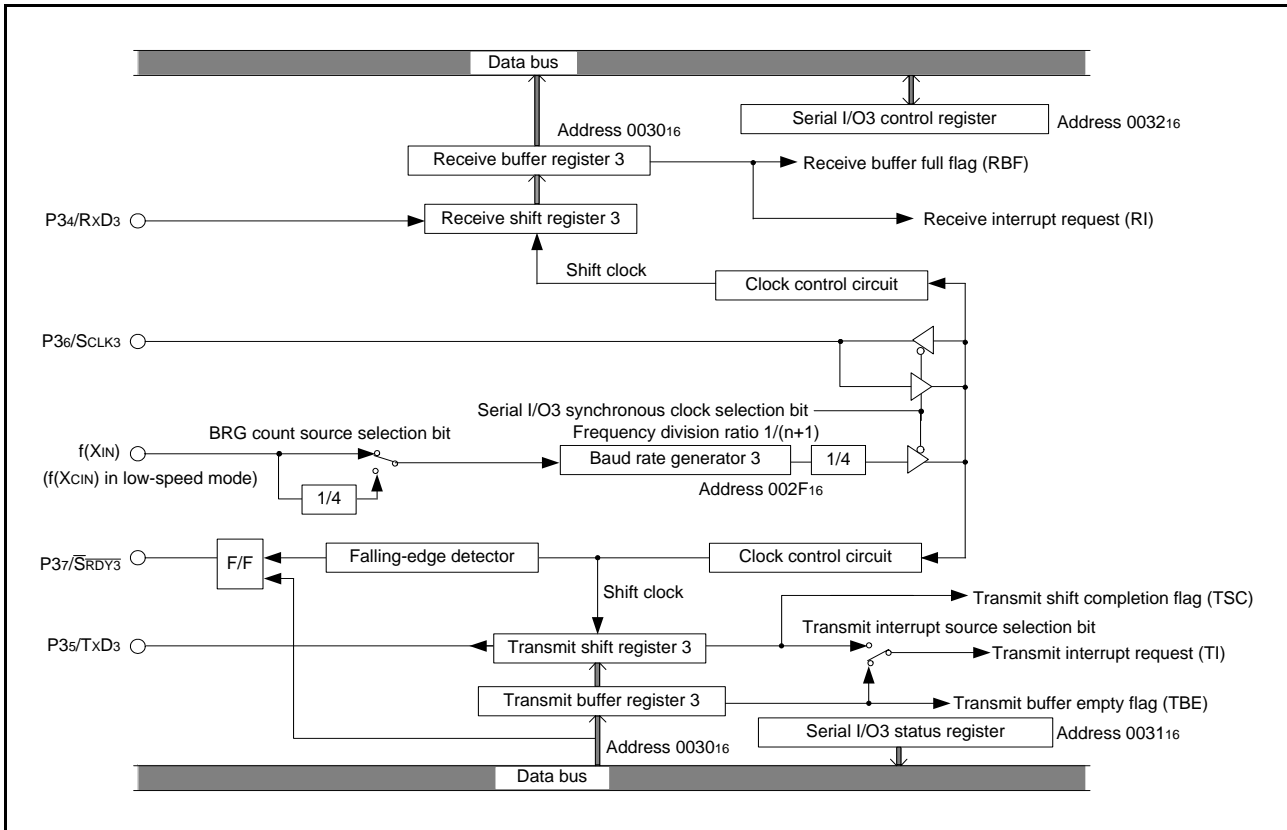


Fig 40. Block diagram of clock synchronous serial I/O3

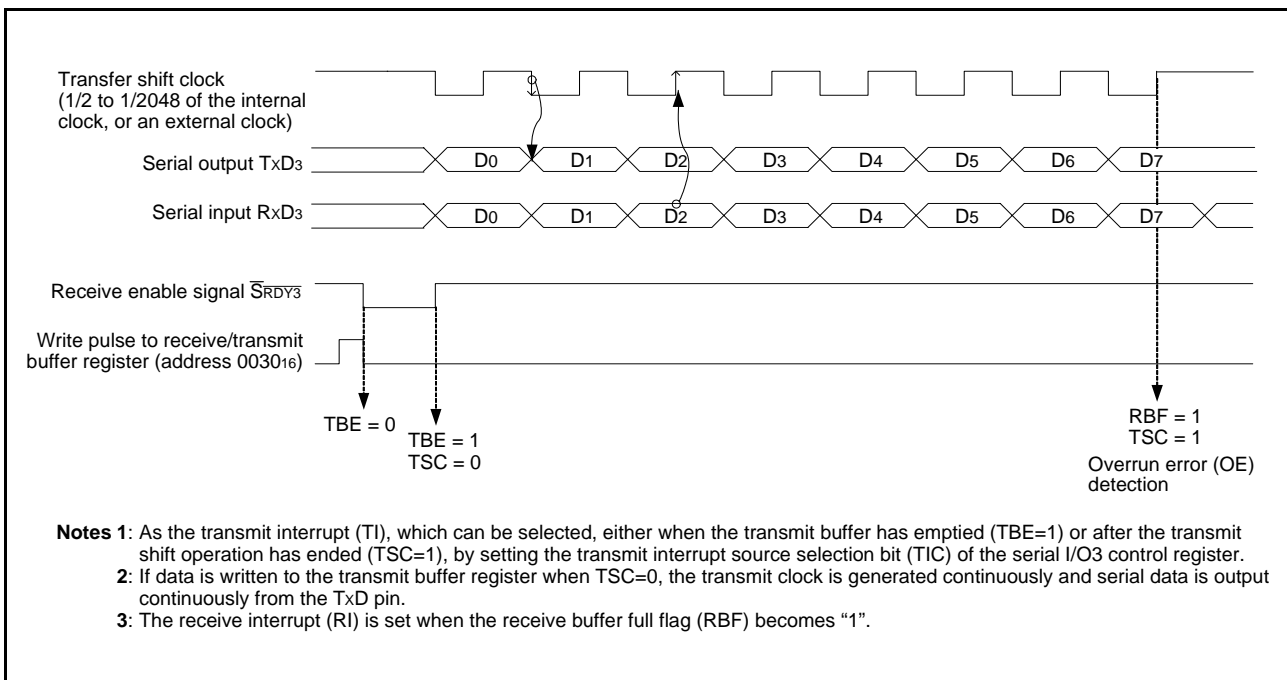


Fig 41. Operation of clock synchronous serial I/O3

**(2) Asynchronous Serial I/O (UART) Mode**

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O3 mode selection bit (b6) of the serial I/O3 control register to "0".

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the two buffers have the same address in a memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register.

The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

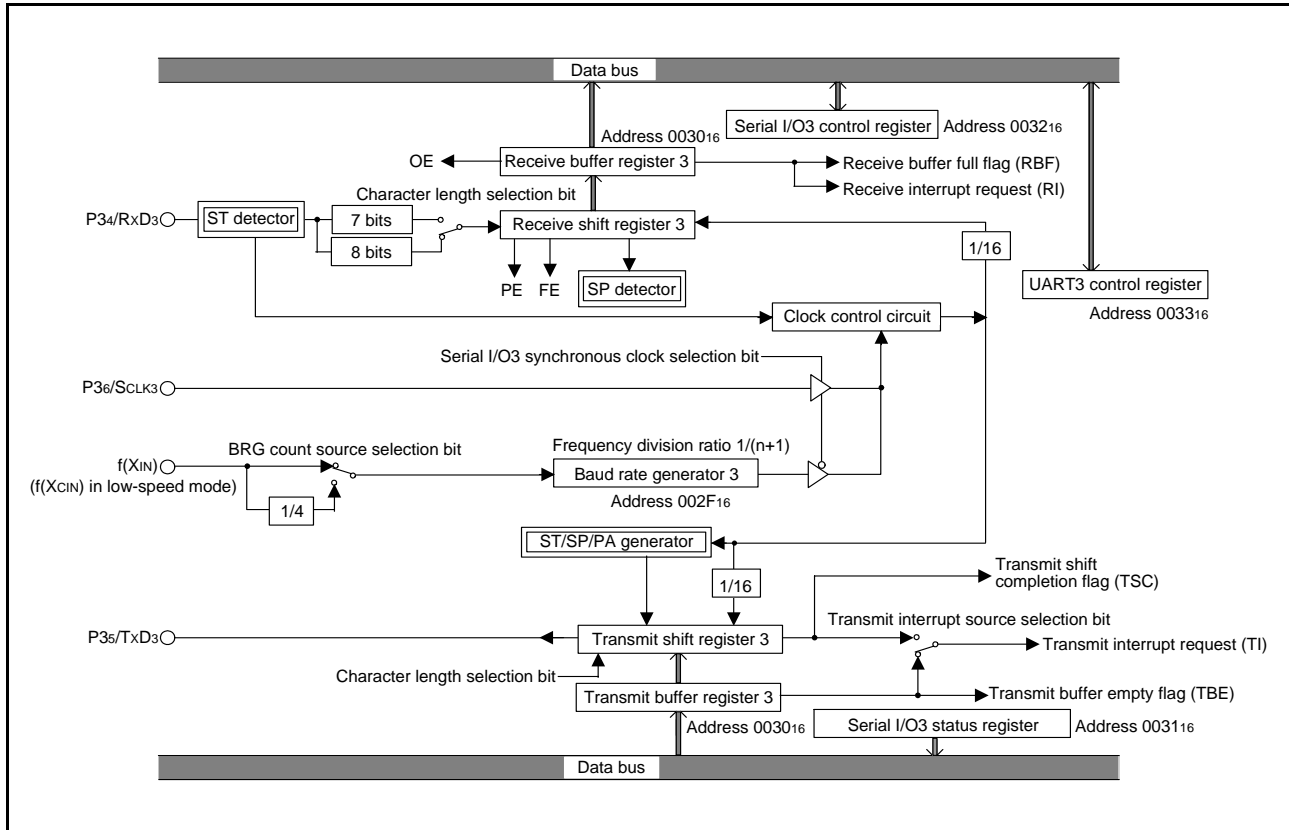


Fig 42. Block diagram of UART serial I/O3

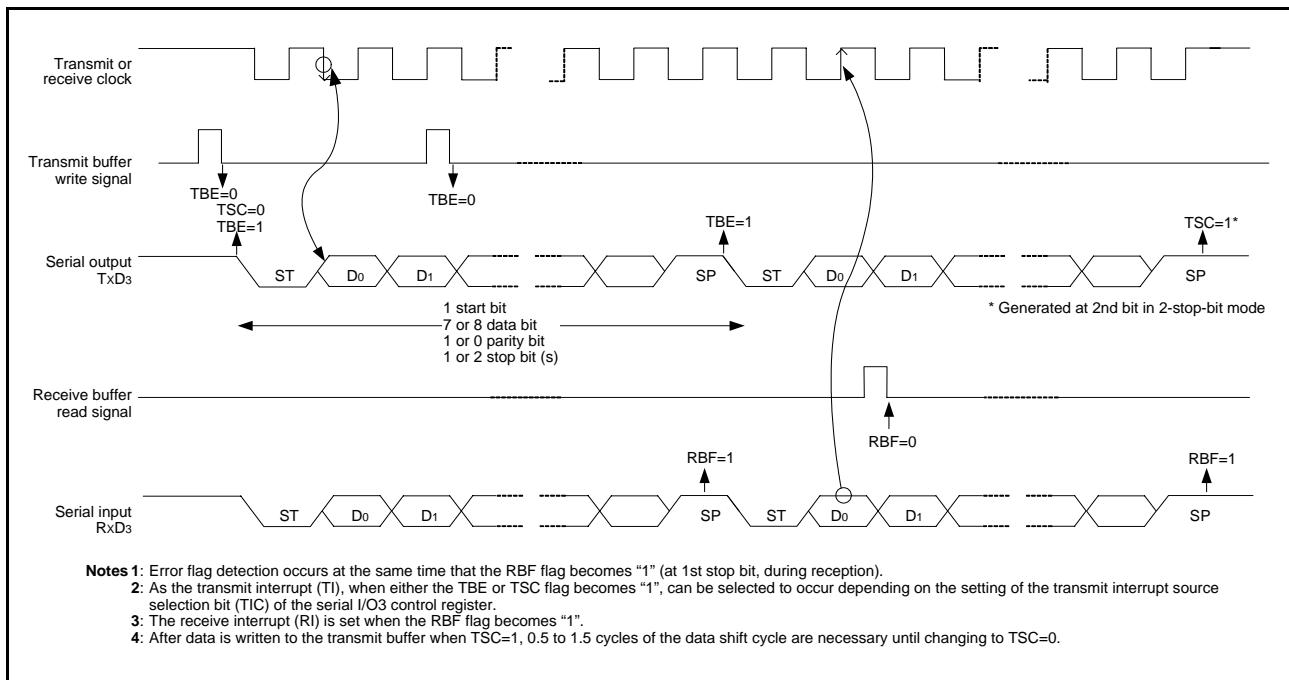


Fig 43. Operation of UART serial I/O3

**[Transmit Buffer Register 3/Receive Buffer Register 3 (TB3/RB3)] 0030<sub>16</sub>**

The transmit buffer register 3 and the receive buffer register 3 are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

**[Serial I/O3 Status Register (SIO3STS)] 0031<sub>16</sub>**

The read-only serial I/O3 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O3 function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer register is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O3 status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O3 enable bit SIOE (bit 7 of the serial I/O3 control register) also clears all the status flags, including the error flags.

Bits 0 to 6 of the serial I/O3 status register are initialized to "0" at reset, but if the transmit enable bit (bit 4) of the serial I/O3 control register has been set to "1", the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

**[Serial I/O3 Control Register (SIO3CON)] 0032<sub>16</sub>**

The serial I/O3 control register consists of eight control bits for the serial I/O3 function.

**[UART3 Control Register (UART3CON)] 0033<sub>16</sub>**

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer, and one bit (bit 4) which is always valid and sets the output structure of the P3<sub>5</sub>/TXD<sub>3</sub> pin.

**[Baud Rate Generator 3 (BRG3)] 002F<sub>16</sub>**

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by  $1/(n + 1)$ , where  $n$  is the value written to the baud rate generator.

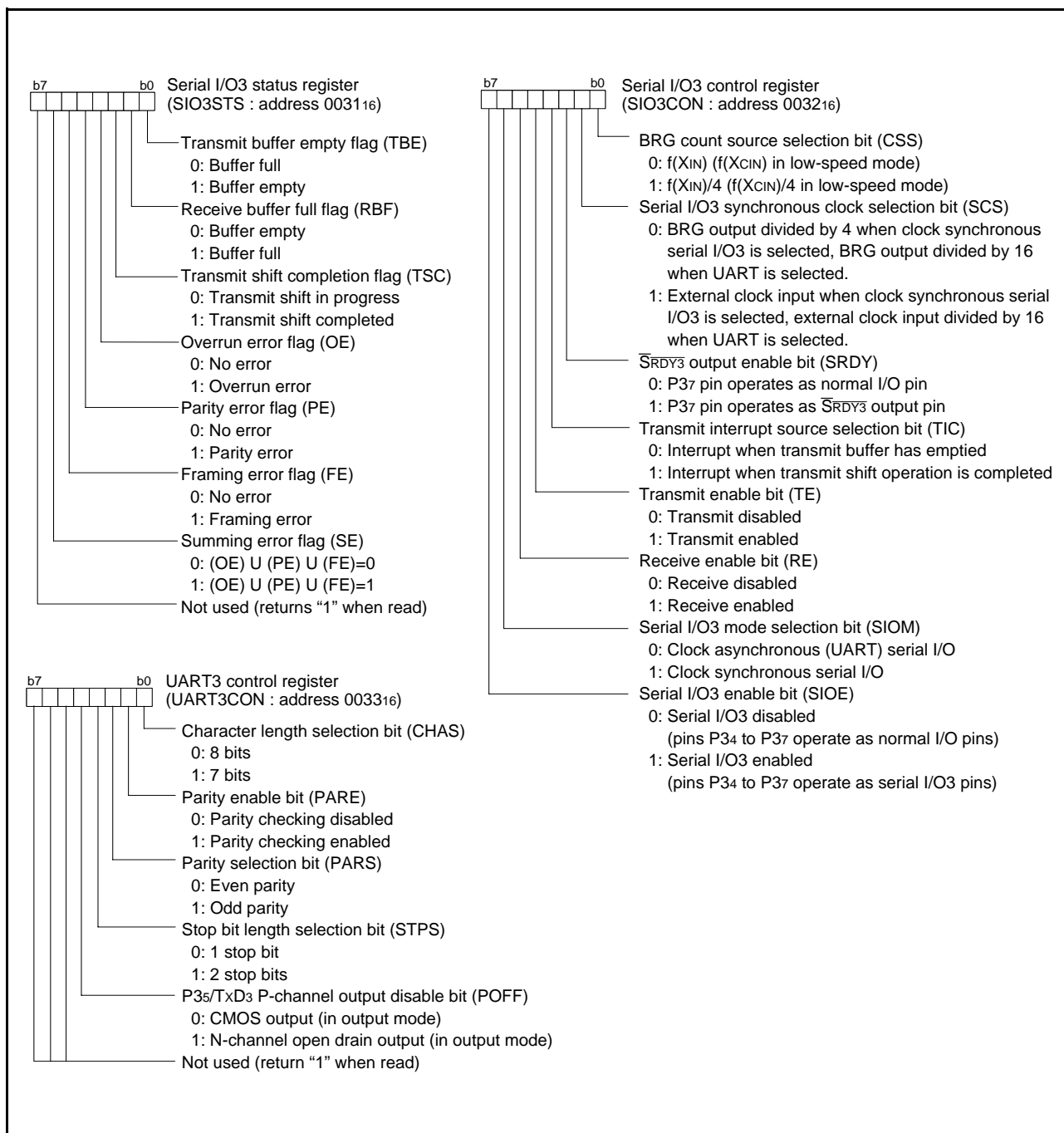


Fig 44. Structure of serial I/O3 control registers

**<Notes concerning serial I/O3>**

## 1. Notes when selecting clock synchronous serial I/O

## 1.1 Stop of transmission operation

## • Note

Clear the serial I/O3 enable bit and the transmit enable bit to “0” (serial I/O and transmit disabled).

## • Reason

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O3 enable bit is cleared to “0” (serial I/O disabled), the internal transmission is running (in this case, since pins TXD3, RXD3, SCLK3, and  $\overline{\text{SRDY}}3$  function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O3 enable bit is set to “1” at this time, the data during internally shifting is output to the TXD3 pin and an operation failure occurs.

## 1.2 Stop of receive operation

## • Note

Clear the receive enable bit to “0” (receive disabled), or clear the serial I/O3 enable bit to “0” (serial I/O disabled).

## 1.3 Stop of transmit/receive operation

## • Note

Clear both the transmit enable bit and receive enable bit to “0” (transmit and receive disabled).

(when data is transmitted and received in the clock synchronous serial I/O mode, any one of data transmission and reception cannot be stopped.)

## • Reason

In the clock synchronous serial I/O mode, the same clock is used for transmission and reception. If any one of transmission and reception is disabled, a bit error occurs because transmission and reception cannot be synchronized.

In this mode, the clock circuit of the transmission circuit also operates for data reception. Accordingly, the transmission circuit does not stop by clearing only the transmit enable bit to “0” (transmit disabled). Also, the transmission circuit is not initialized by clearing the serial I/O3 enable bit to “0” (serial I/O disabled) (refer to 1.1).

## 2. Notes when selecting clock asynchronous serial I/O

## 2.1 Stop of transmission operation

## • Note

Clear the transmit enable bit to “0” (transmit disabled). The transmission operation does not stop by clearing the serial I/O3 enable bit to “0”.

## • Reason

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O3 enable bit is cleared to “0” (serial I/O disabled), the internal transmission is running (in this case, since pins TXD3, RXD3, SCLK3, and  $\overline{\text{SRDY}}3$  function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O3 enable bit is set to “1” at this time, the data during internally shifting is output to the TXD3 pin and an operation failure occurs.

## 2.2 Stop of receive operation

## • Note

Clear the receive enable bit to “0” (receive disabled).

## 2.3 Stop of transmit/receive operation

## • Note 1 (only transmission operation is stopped)

Clear the transmit enable bit to “0” (transmit disabled). The transmission operation does not stop by clearing the serial I/O3 enable bit to “0”.

## • Reason

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O3 enable bit is cleared to “0” (serial I/O disabled), the internal transmission is running (in this case, since pins TXD3, RXD3, SCLK3, and  $\overline{\text{SRDY}}3$  function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O3 enable bit is set to “1” at this time, the data during internally shifting is output to the TXD3 pin and an operation failure occurs.

## • Note 2 (only receive operation is stopped)

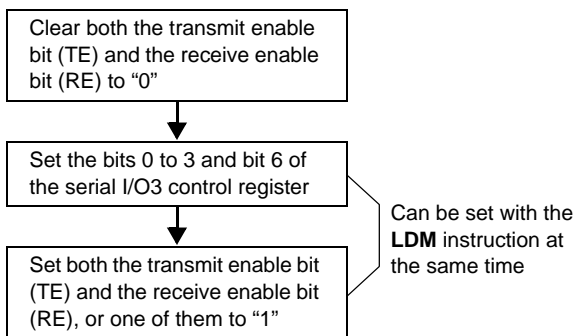
Clear the receive enable bit to “0” (receive disabled).

3.  $\overline{SRDY3}$  output of reception side

- Note  
When signals are output from the  $\overline{SRDY3}$  pin on the reception side by using an external clock in the clock synchronous serial I/O mode, set all of the receive enable bit, the  $\overline{SRDY3}$  output enable bit, and the transmit enable bit to "1" (transmit enabled).

4. Setting serial I/O3 control register again

- Note  
Set the serial I/O3 control register again after the transmission and the reception circuits are reset by clearing both the transmit enable bit and the receive enable bit to "0".



5. Data transmission control with referring to transmit shift register completion flag

- Note  
After the transmit data is written to the transmit buffer register, the transmit shift register completion flag changes from "1" to "0" with a delay of 0.5 to 1.5 shift clocks. When data transmission is controlled with referring to the flag after writing the data to the transmit buffer register, note the delay.

6. Transmission control when external clock is selected

- Note  
When an external clock is used as the synchronous clock for data transmission, set the transmit enable bit to "1" at "H" of the SCLK3 input level. Also, write data to the transmit buffer register at "H" of the SCLK input level.

7. Transmit interrupt request when transmit enable bit is set

- Note  
When using the transmit interrupt, take the following sequence.

1. Set the serial I/O3 transmit interrupt enable bit to "0" (disabled).
2. Set the transmit enable bit to "1".
3. Set the serial I/O3 transmit interrupt request bit to "0" after 1 or more instruction has executed.
4. Set the serial I/O3 transmit interrupt enable bit to "1" (enabled).

- Reason

When the transmit enable bit is set to "1", the transmit buffer empty flag and the transmit shift register shift completion flag are also set to "1". Therefore, regardless of selecting which timing for the generating of transmit interrupts, the interrupt request is generated and the transmit interrupt request bit is set at this point.

**PULSE WIDTH MODULATION (PWM)**

The 3803 group (Spec.H QzROM version) has PWM functions with an 8-bit resolution, based on a signal that is the clock input X<sub>IN</sub> or that clock input divided by 2 or the clock input X<sub>CIN</sub> or that clock input divided by 2 in low-speed mode.

**• Data Setting**

The PWM output pin also functions as port P56. Set the PWM period by the PWM prescaler, and set the “H” term of output pulse by the PWM register.

If the value in the PWM prescaler is n and the value in the PWM register is m (where n = 0 to 255 and m = 0 to 255):

$$\begin{aligned} \text{PWM period} &= 255 \times (n+1) / f(\text{X}_{\text{IN}}) \\ &= 31.875 \times (n+1) \mu\text{s} \\ &\text{(when } f(\text{X}_{\text{IN}}) = 8 \text{ MHz, count source selection bit = "0"}) \end{aligned}$$

$$\begin{aligned} \text{Output pulse "H" term} &= \text{PWM period} \times m / 255 \\ &= 0.125 \times (n+1) \times m \mu\text{s} \\ &\text{(when } f(\text{X}_{\text{IN}}) = 8 \text{ MHz, count source selection bit = "0"}) \end{aligned}$$

**• PWM Operation**

When bit 0 (PWM enable bit) of the PWM control register is set to “1”, operation starts by initializing the PWM output circuit, and pulses are output starting at an “H”.

If the PWM register or PWM prescaler is updated during PWM output, the pulses will change in the cycle after the one in which the change was made.

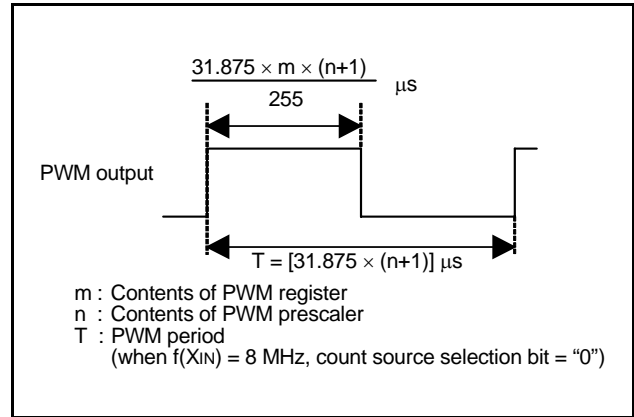


Fig 45. Timing of PWM period

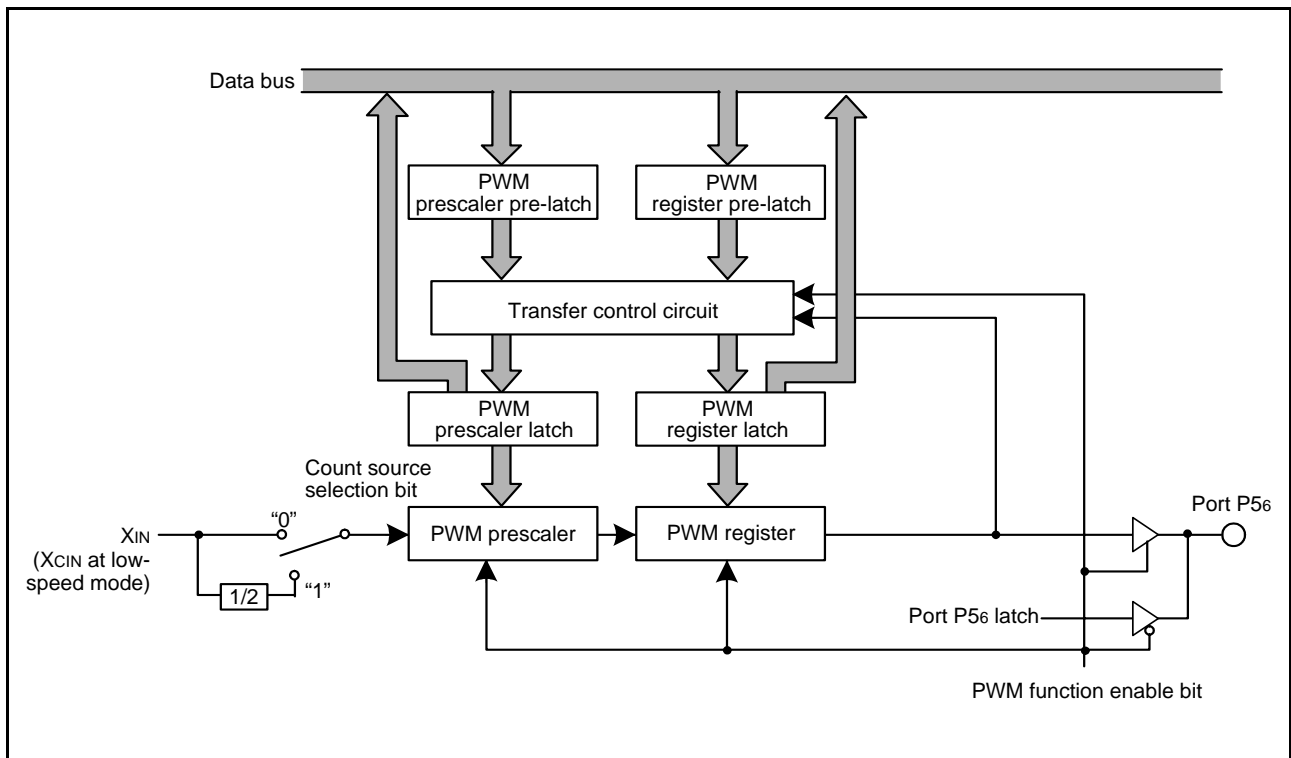


Fig 46. Block diagram of PWM function



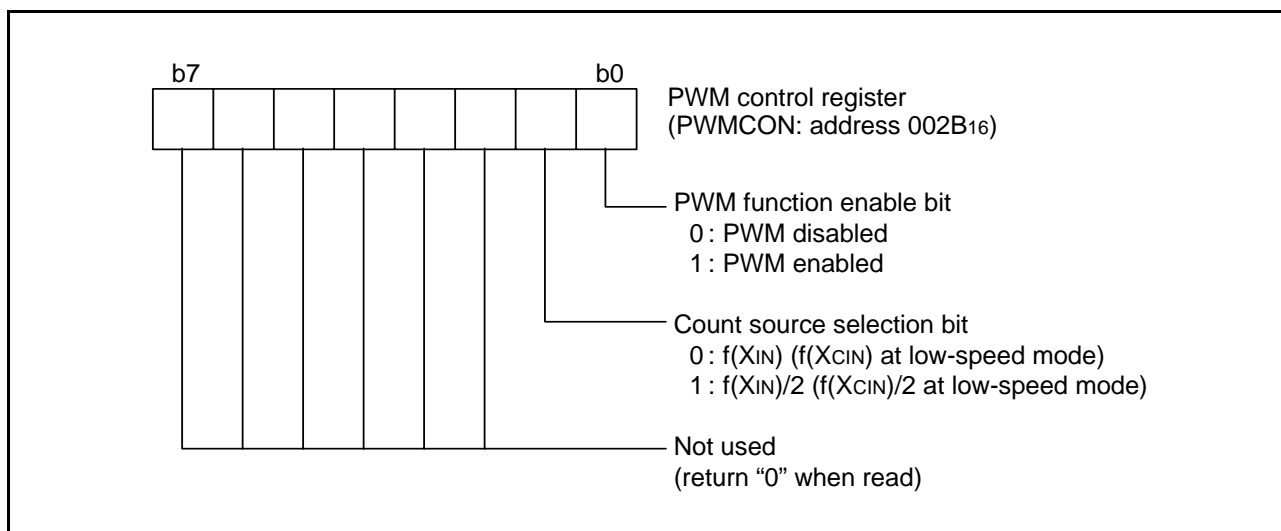


Fig 47. Structure of PWM control register

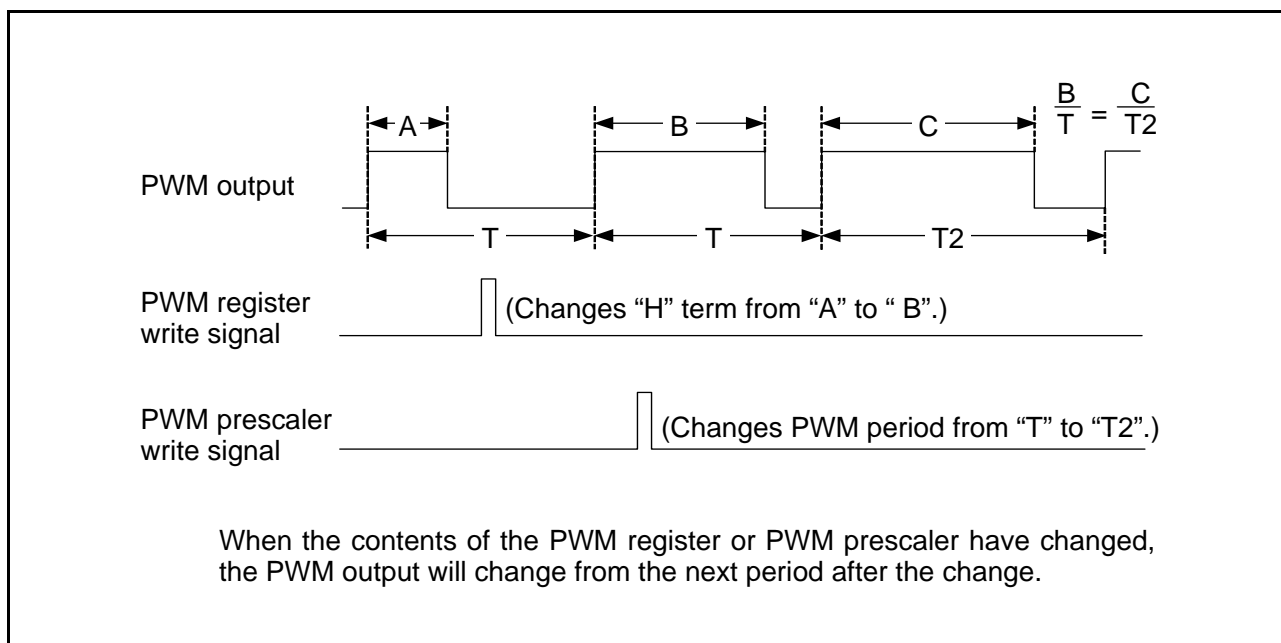


Fig 48. PWM output timing when PWM register or PWM prescaler is changed

<Notes>

The PWM starts after the PWM function enable bit is set to enable and "L" level is output from the PWM pin. The length of this "L" level output is as follows:

$$\frac{n+1}{2 \times f(X_{IN})} \text{ sec} \quad (\text{Count source selection bit} = 0, \text{ where } n \text{ is the value set in the prescaler})$$

$$\frac{n+1}{f(X_{IN})} \text{ sec} \quad (\text{Count source selection bit} = 1, \text{ where } n \text{ is the value set in the prescaler})$$

**A/D CONVERTER**

**[AD Conversion Register 1, 2 (AD1, AD2)] 0035<sub>16</sub>, 0038<sub>16</sub>**

The AD conversion register is a read-only register that stores the result of an A/D conversion. When reading this register during an A/D conversion, the previous conversion result is read.

Bit 7 of the AD conversion register 2 is the conversion mode selection bit. When this bit is set to “0”, the A/D converter becomes the 10-bit A/D mode. When this bit is set to “1”, that becomes the 8-bit A/D mode. The conversion result of the 8-bit A/D mode is stored in the AD conversion register 1. As for 10-bit A/D mode, not only 10-bit reading but also only high-order 8-bit reading of conversion result can be performed by selecting the reading procedure of the AD conversion registers 1, 2 after A/D conversion is completed (in Figure.50).

As for 10-bit A/D mode, the 8-bit reading inclined to MSB is performed when reading the AD converter register 1 after A/D conversion is started; and when the AD converter register 1 is read after reading the AD converter register 2, the 8-bit reading inclined to LSB is performed.

**[AD/DA Control Register (ADCON)] 0034<sub>16</sub>**

The AD/DA control register controls the A/D conversion process. Bits 0 to 2 and bit 4 select a specific analog input pin. Bit 3 signals the completion of an A/D conversion. The value of this bit remains at “0” during an A/D conversion, and changes to “1” when an A/D conversion ends. Writing “0” to this bit starts the A/D conversion.

**• Comparison Voltage Generator**

The comparison voltage generator divides the voltage between AVSS and VREF into 1024, and that outputs the comparison voltage in the 10-bit A/D mode (256 division in 8-bit A/D mode). The A/D converter successively compares the comparison voltage Vref in each mode, dividing the VREF voltage (see below), with the input voltage.

- 10-bit A/D mode (10-bit reading)

$$V_{ref} = \frac{V_{REF}}{1024} \times n \quad (n = 0 - 1023)$$

- 10-bit A/D mode (8-bit reading)

$$V_{ref} = \frac{V_{REF}}{256} \times n \quad (n = 0 - 255)$$

- 8-bit A/D mode

$$V_{ref} = \frac{V_{REF}}{256} \times n \quad (n = 1 - 255)$$

$$= 0 \quad (n = 0)$$

**• Channel Selector**

The channel selector selects one of ports P67/AN7 to P60/AN0 or P07/AN15 to P00/AN8, and inputs the voltage to the comparator.

**• Comparator and Control Circuit**

The comparator and control circuit compares an analog input voltage with the comparison voltage, and then stores the result in the AD conversion registers 1, 2. When an A/D conversion is completed, the control circuit sets the AD conversion completion bit and the AD interrupt request bit to “1”.

Note that because the comparator consists of a capacitor coupling, set f(XIN) to 500 kHz or more during an A/D conversion.

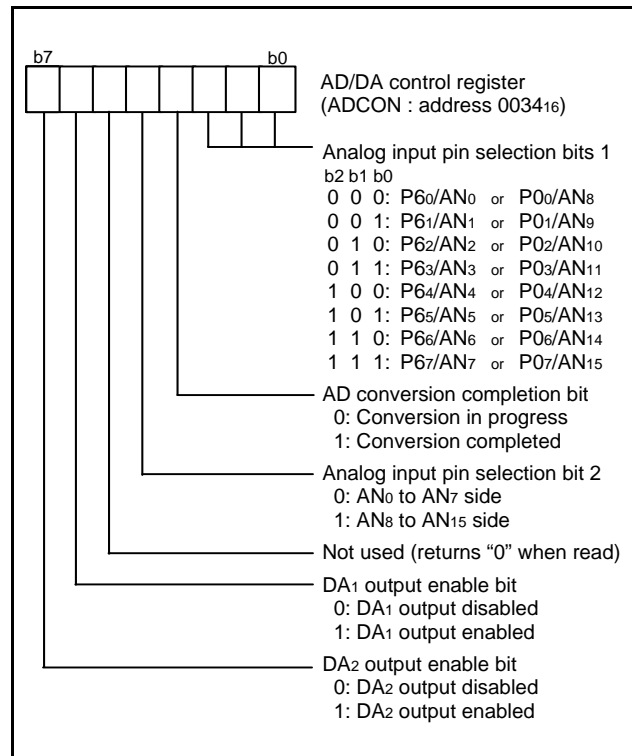


Fig 49. Structure of AD/DA control register

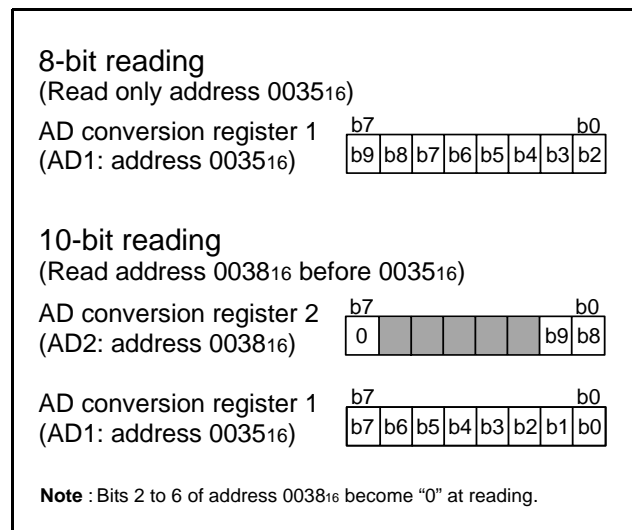


Fig 50. Structure of 10-bit A/D mode reading

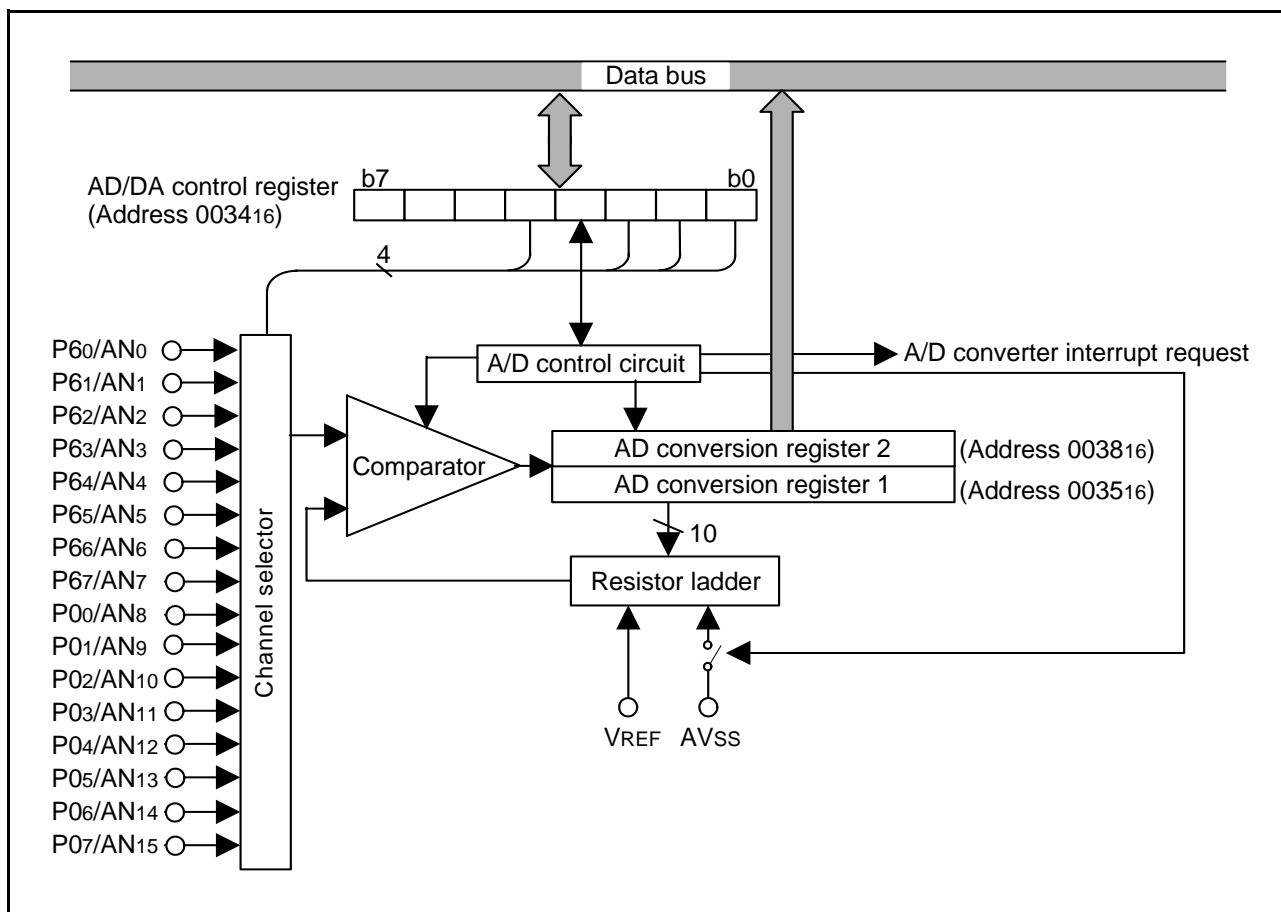


Fig 51. Block diagram of A/D converter

**D/A CONVERTER**

The 3803 group (Spec.H QzROM version) has two internal D/A converters (DA1 and DA2) with 8-bit resolution.

The D/A conversion is performed by setting the value in each DA conversion register. The result of D/A conversion is output from the DA1 or DA2 pin by setting the DA output enable bit to "1".

When using the D/A converter, the corresponding port direction register bit (P30/DA1 or P31/DA2) must be set to "0" (input status).

The output analog voltage V is determined by the value n (decimal notation) in the DA conversion register as follows:

$$V = V_{REF} \times n / 256 \quad (n = 0 \text{ to } 255)$$

Where VREF is the reference voltage.

At reset, the DA conversion registers are cleared to "0016", and the DA output enable bits are cleared to "0", and the P30/DA1 and P31/DA2 pins become high impedance.

The DA output does not have buffers. Accordingly, connect an external buffer when driving a low-impedance load.

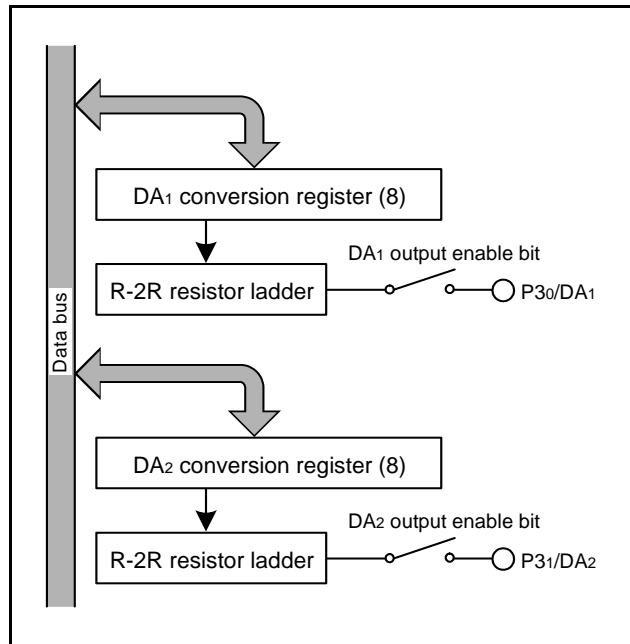


Fig 52. Block diagram of D/A converter

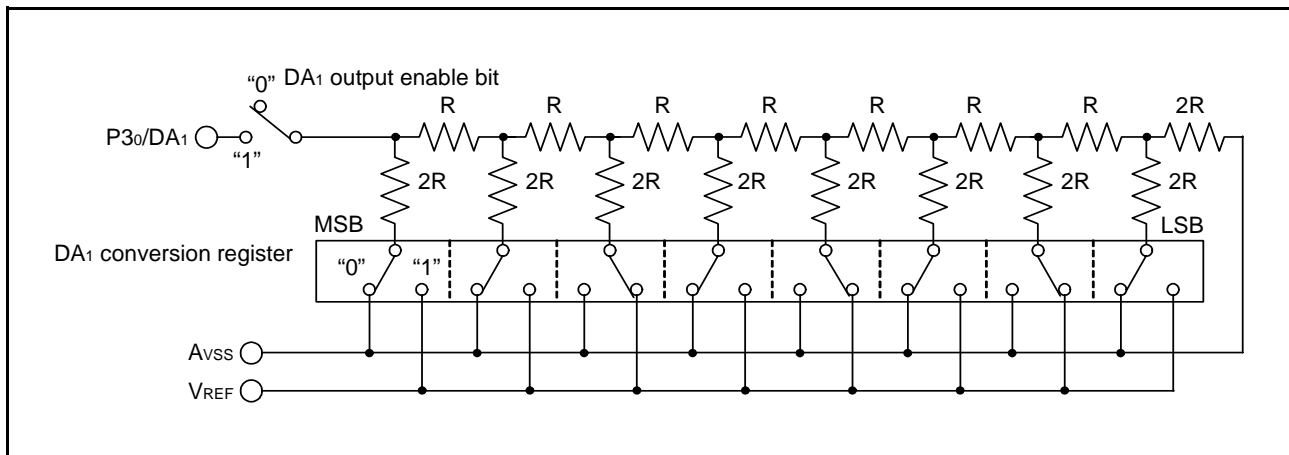


Fig 53. Equivalent connection circuit of D/A converter (DA1)

**WATCHDOG TIMER**

The watchdog timer gives a mean of returning to the reset status when a program cannot run on a normal loop (for example, because of a software run-away). The watchdog timer consists of an 8-bit watchdog timer L and an 8-bit watchdog timer H.

**• Watchdog Timer Initial Value**

Watchdog timer L is set to “FF16” and watchdog timer H is set to “FF16” by writing to the watchdog timer control register (address 001E16) or at a reset. Any write instruction that causes a write signal can be used, such as the STA, LDM, CLB, etc. Data can only be written to bits 6 and 7 of the watchdog timer control register. Regardless of the value written to bits 0 to 5, the above-mentioned value will be set to each timer.

**• Watchdog Timer Operations**

The watchdog timer stops at reset and starts to count down by writing to the watchdog timer control register (address 001E16). An internal reset occurs at an underflow of the watchdog timer H. The reset is released after waiting for a reset release time and the program is processed from the reset vector address. Accordingly, programming is usually performed so that writing to the watchdog timer control register may be started before an underflow. If writing to the watchdog timer control register is not performed once, the watchdog timer does not function.

**• Bit 6 of Watchdog Timer Control Register**

- When bit 6 of the watchdog timer control register is “0”, the MCU enters the stop mode by execution of STP instruction. Just after releasing the stop mode, the watchdog timer restarts counting(Note.). When executing the WIT instruction, the watchdog timer does not stop.
- When bit 6 is “1”, execution of STP instruction causes an internal reset. When this bit is set to “1” once, it cannot be rewritten to “0” by program. Bit 6 is “0” at reset.

The following shows the period between the write execution to the watchdog timer control register and the underflow of watchdog timer H.

Bit 7 of the watchdog timer control register is “0”:

- when  $X_{CIN} = 32.768 \text{ kHz}$ ; 32 s
- when  $X_{IN} = 16 \text{ MHz}$ ; 65.536 ms

Bit 7 of the watchdog timer control register is “1”:

- when  $X_{CIN} = 32.768 \text{ kHz}$ ; 125 ms
- when  $X_{IN} = 16 \text{ MHz}$ ; 256  $\mu\text{s}$

Note. The watchdog timer continues to count even while waiting for a stop release. Therefore, make sure that watchdog timer H does not underflow during this period.

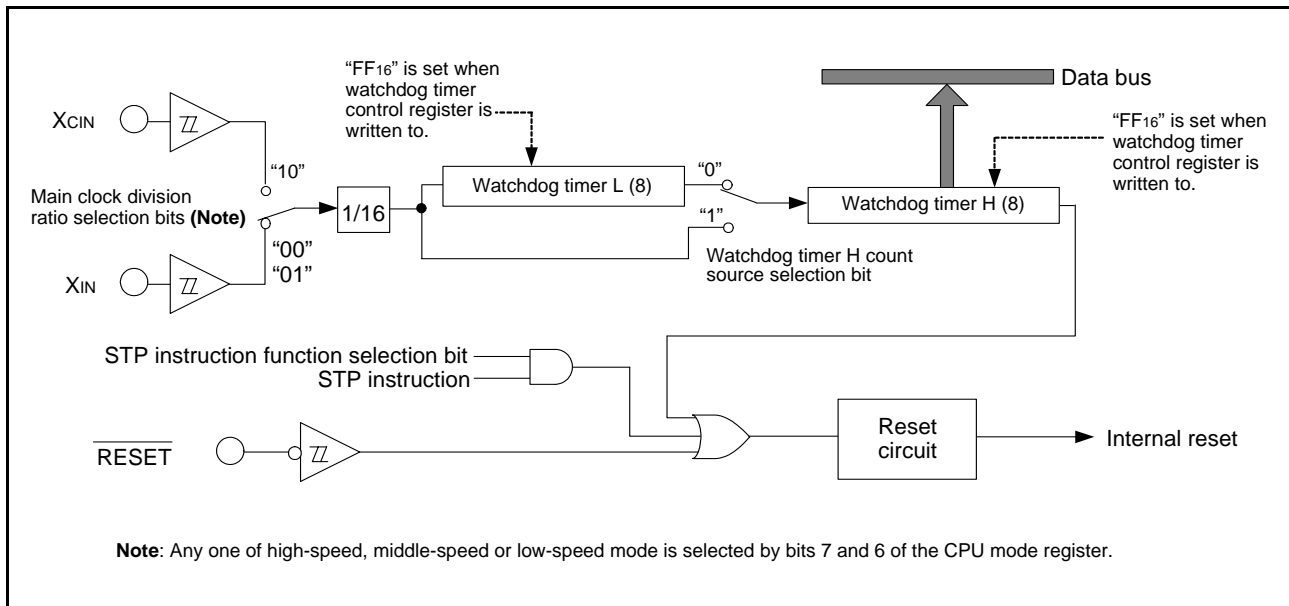


Fig 54. Block diagram of Watchdog timer

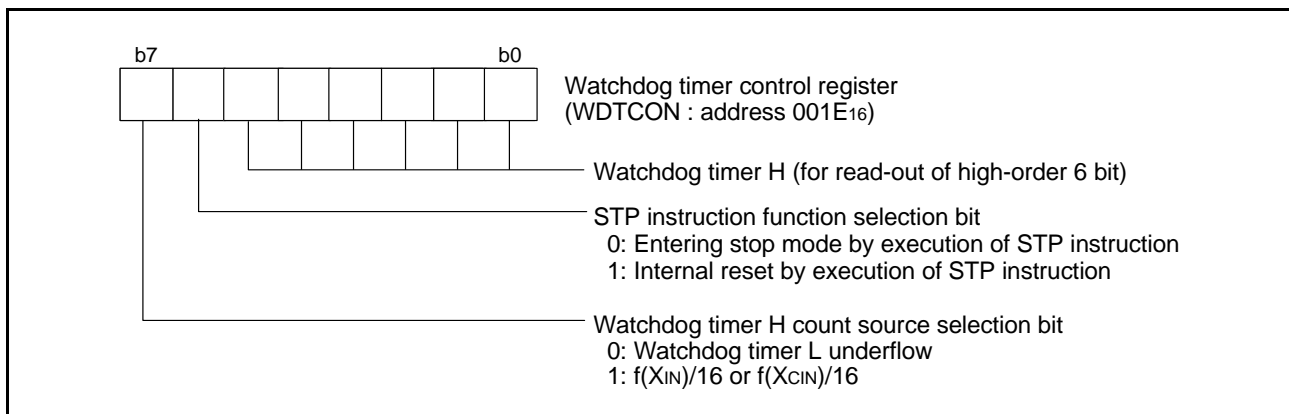


Fig 55. Structure of Watchdog timer control register

**RESET CIRCUIT**

To reset the microcomputer,  $\overline{\text{RESET}}$  pin should be held at an “L” level for 16 cycles or more of  $X_{\text{IN}}$ . Then the  $\overline{\text{RESET}}$  pin is returned to an “H” level (the power source voltage should be between 1.8 V and 5.5 V, and the oscillation should be stable), reset is released. After the reset is completed, the program starts from the address contained in address  $\text{FFFD}_{16}$  (high-order byte) and address  $\text{FFFC}_{16}$  (low-order byte). Make sure that the reset input voltage is less than 0.29 V for  $V_{\text{CC}}$  of 1.8 V.

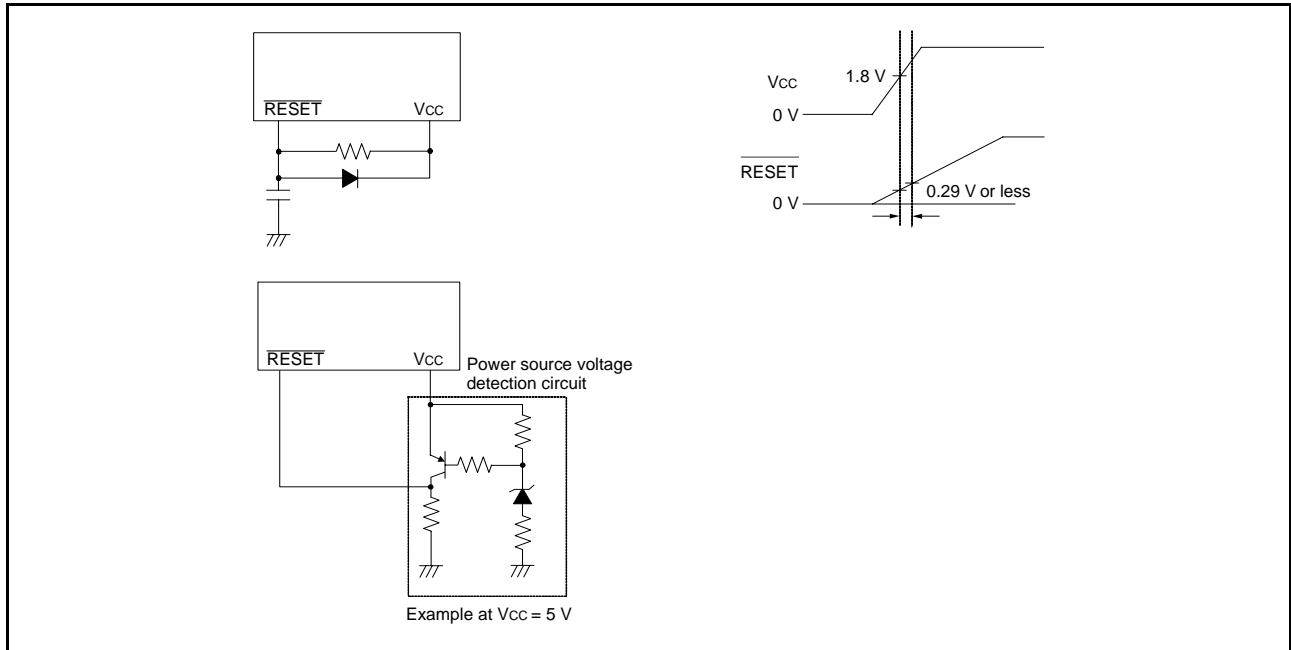


Fig 56. Reset circuit example

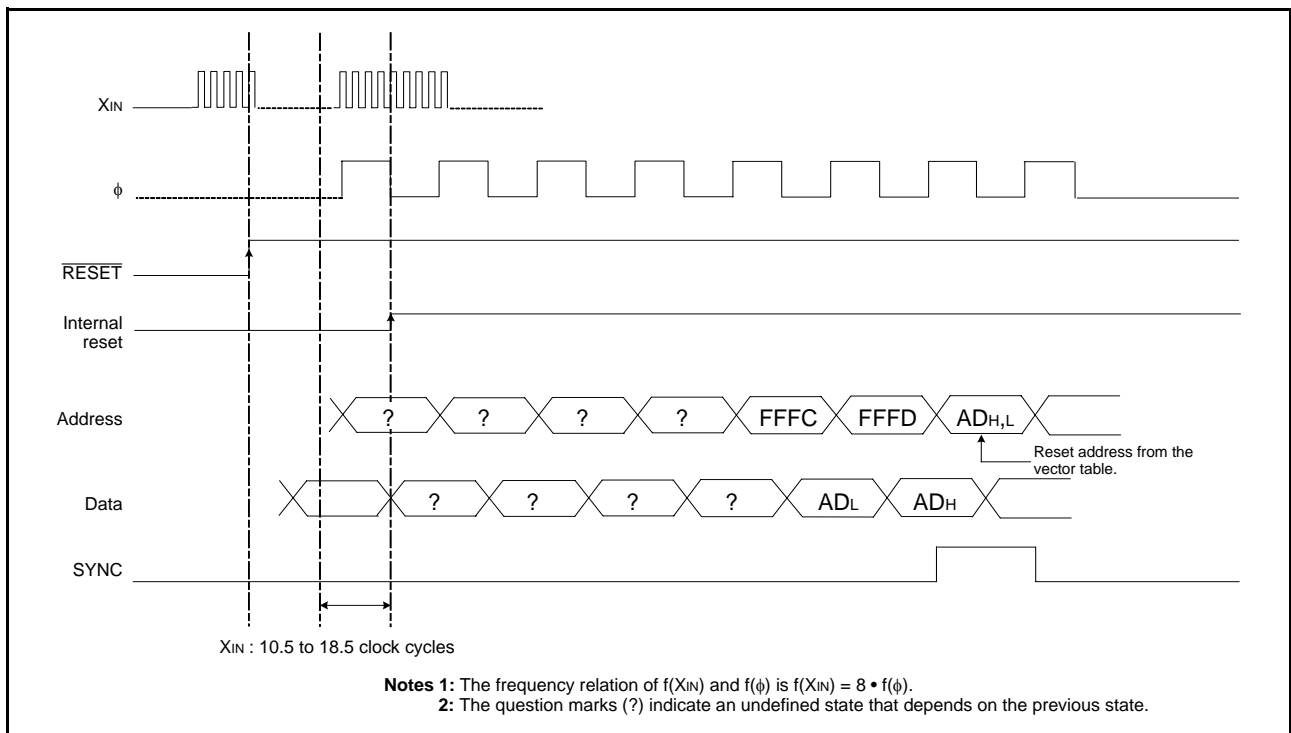


Fig 57. Reset sequence

	Address	Register contents		Address	Register contents
(1) Port P0 (P0)	0000 <sub>16</sub>	00 <sub>16</sub>	(34) Timer Z (low-order) (TZL)	0028 <sub>16</sub>	FF <sub>16</sub>
(2) Port P0 direction register (P0D)	0001 <sub>16</sub>	00 <sub>16</sub>	(35) Timer Z (high-order) (TZH)	0029 <sub>16</sub>	FF <sub>16</sub>
(3) Port P1 (P1)	0002 <sub>16</sub>	00 <sub>16</sub>	(36) Timer Z mode register (TZM)	002A <sub>16</sub>	00 <sub>16</sub>
(4) Port P1 direction register (P1D)	0003 <sub>16</sub>	00 <sub>16</sub>	(37) PWM control register (PWMCN)	002B <sub>16</sub>	00 <sub>16</sub>
(5) Port P2 (P2)	0004 <sub>16</sub>	00 <sub>16</sub>	(38) PWM prescaler (PREPWM)	002C <sub>16</sub>	X X X X X X X X
(6) Port P2 direction register (P2D)	0005 <sub>16</sub>	00 <sub>16</sub>	(39) PWM register (PWM)	002D <sub>16</sub>	X X X X X X X X
(7) Port P3 (P3)	0006 <sub>16</sub>	00 <sub>16</sub>	(40) Baud rate generator 3 (BRG3)	002F <sub>16</sub>	X X X X X X X X
(8) Port P3 direction register (P3D)	0007 <sub>16</sub>	00 <sub>16</sub>	(41) Transmit/Receive buffer register 3 (TB3/RB3)	0030 <sub>16</sub>	X X X X X X X X
(9) Port P4 (P4)	0008 <sub>16</sub>	00 <sub>16</sub>	(42) Serial I/O3 status register (SIO3STS)	0031 <sub>16</sub>	1 0 0 0 0 0 0 0
(10) Port P4 direction register (P4D)	0009 <sub>16</sub>	00 <sub>16</sub>	(43) Serial I/O3 control register (SIO3CN)	0032 <sub>16</sub>	00 <sub>16</sub>
(11) Port P5 (P5)	000A <sub>16</sub>	00 <sub>16</sub>	(44) UART3 control register (UART3CN)	0033 <sub>16</sub>	1 1 1 0 0 0 0 0
(12) Port P5 direction register (P5D)	000B <sub>16</sub>	00 <sub>16</sub>	(45) AD/DA control register (ADCN)	0034 <sub>16</sub>	0 0 0 0 1 0 0 0
(13) Port P6 (P6)	000C <sub>16</sub>	00 <sub>16</sub>	(46) AD conversion register 1 (AD1)	0035 <sub>16</sub>	X X X X X X X X
(14) Port P6 direction register (P6D)	000D <sub>16</sub>	00 <sub>16</sub>	(47) DA1 conversion register (DA1)	0036 <sub>16</sub>	00 <sub>16</sub>
(15) Timer 12, X count source selection register (T12XCSS)	000E <sub>16</sub>	0 0 1 1 0 0 1 1	(48) DA2 conversion register (DA2)	0037 <sub>16</sub>	00 <sub>16</sub>
(16) Timer Y, Z count source selection register (TYZCSS)	000F <sub>16</sub>	0 0 1 1 0 0 1 1	(49) AD conversion register 2 (AD2)	0038 <sub>16</sub>	0 0 0 0 0 0 X X
(17) MISRG	0010 <sub>16</sub>	00 <sub>16</sub>	(50) Interrupt source selection register (INTSEL)	0039 <sub>16</sub>	00 <sub>16</sub>
(18) Transmit/Receive buffer register 1 (TB1/RB1)	0018 <sub>16</sub>	X X X X X X X X	(51) Interrupt edge selection register (INTEDGE)	003A <sub>16</sub>	00 <sub>16</sub>
(19) Serial I/O1 status register (SIO1STS)	0019 <sub>16</sub>	1 0 0 0 0 0 0 0	(52) CPU mode register (CPUM)	003B <sub>16</sub>	0 1 0 0 1 0 0 0
(20) Serial I/O1 control register (SIO1CN)	001A <sub>16</sub>	00 <sub>16</sub>	(53) Interrupt request register 1 (IREQ1)	003C <sub>16</sub>	00 <sub>16</sub>
(21) UART1 control register (UART1CN)	001B <sub>16</sub>	1 1 1 0 0 0 0 0	(54) Interrupt request register 2 (IREQ2)	003D <sub>16</sub>	00 <sub>16</sub>
(22) Baud rate generator 1 (BRG1)	001C <sub>16</sub>	X X X X X X X X	(55) Interrupt control register 1 (ICON1)	003E <sub>16</sub>	00 <sub>16</sub>
(23) Serial I/O2 control register (SIO2CN)	001D <sub>16</sub>	00 <sub>16</sub>	(56) Interrupt control register 2 (ICON2)	003F <sub>16</sub>	00 <sub>16</sub>
(24) Watchdog timer control register (WDTCON)	001E <sub>16</sub>	0 0 1 1 1 1 1 1	(57) Port P0 pull-up control register (PULL0)	0FF0 <sub>16</sub>	00 <sub>16</sub>
(25) Serial I/O2 register (SIO2)	001F <sub>16</sub>	X X X X X X X X	(58) Port P1 pull-up control register (PULL1)	0FF1 <sub>16</sub>	00 <sub>16</sub>
(26) Prescaler 12 (PRE12)	0020 <sub>16</sub>	FF <sub>16</sub>	(59) Port P2 pull-up control register (PULL2)	0FF2 <sub>16</sub>	00 <sub>16</sub>
(27) Timer 1 (T1)	0021 <sub>16</sub>	01 <sub>16</sub>	(60) Port P3 pull-up control register (PULL3)	0FF3 <sub>16</sub>	00 <sub>16</sub>
(28) Timer 2 (T2)	0022 <sub>16</sub>	FF <sub>16</sub>	(61) Port P4 pull-up control register (PULL4)	0FF4 <sub>16</sub>	00 <sub>16</sub>
(29) Timer XY mode register (TM)	0023 <sub>16</sub>	00 <sub>16</sub>	(62) Port P5 pull-up control register (PULL5)	0FF5 <sub>16</sub>	00 <sub>16</sub>
(30) Prescaler X (PREX)	0024 <sub>16</sub>	FF <sub>16</sub>	(63) Port P6 pull-up control register (PULL6)	0FF6 <sub>16</sub>	00 <sub>16</sub>
(31) Timer X (TX)	0025 <sub>16</sub>	FF <sub>16</sub>	(64) Processor status register (PS)	X X X X X 1 X X	
(32) Prescaler Y (PREY)	0026 <sub>16</sub>	FF <sub>16</sub>	(65) Program counter (PC <sub>H</sub> )	FFFD <sub>16</sub> contents	
(33) Timer Y (TY)	0027 <sub>16</sub>	FF <sub>16</sub>	(PC <sub>L</sub> )	FFFC <sub>16</sub> contents	

**Note** : X: Not fixed.  
Since the initial values for other than above mentioned registers and RAM contents are indefinite at reset, they must be set.

Fig 58. Internal status at reset

## CLOCK GENERATING CIRCUIT

The 3803 group (Spec.H QzROM version) has two built-in oscillation circuits: main clock XIN-XOUT oscillation circuit and sub clock XCIN-XCOUT oscillation circuit. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT (XCIN and XCOUT). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. (An external feed-back resistor may be needed depending on conditions.) However, an external feed-back resistor is needed between XCIN and XCOUT. Immediately after power on, only the XIN oscillation circuit starts oscillating, and XCIN and XCOUT pins function as I/O ports.

### • Frequency Control

#### (1) Middle-speed mode

The internal clock  $\phi$  is the frequency of XIN divided by 8. After reset is released, this mode is selected.

#### (2) High-speed mode

The internal clock  $\phi$  is half the frequency of XIN.

#### (3) Low-speed mode

The internal clock  $\phi$  is half the frequency of XCIN.

#### (4) Low power dissipation mode

The low power consumption operation can be realized by stopping the main clock XIN in low-speed mode. To stop the main clock, set bit 5 of the CPU mode register to "1". When the main clock XIN is restarted (by setting the main clock stop bit to "0"), set sufficient time for oscillation to stabilize.

The sub-clock XCIN-XCOUT oscillating circuit can not directly input clocks that are generated externally. Accordingly, make sure to cause an external resonator to oscillate.

## Oscillation Control

### (1) Stop mode

If the STP instruction is executed, the internal clock  $\phi$  stops at an "H" level, and XIN and XCIN oscillators stop. When the oscillation stabilizing time set after STP instruction released bit (bit 0 of address 001016) is "0", the prescaler 12 is set to "FF16" and timer 1 is set to "0116". When the oscillation stabilizing time set after STP instruction released bit is "1", set the sufficient time for oscillation of used oscillator to stabilize since nothing is set to the prescaler 12 and timer 1.

After STP instruction is released, the input of the prescaler 12 is connected to count source which had set at executing the STP instruction, and the output of the prescaler 12 is connected to timer 1. Oscillator restarts when an external interrupt is received, but the internal clock  $\phi$  is not supplied to the CPU (remains at "H") until timer 1 underflows. The internal clock  $\phi$  is supplied for the first time, when timer 1 underflows. This ensures time for the clock oscillation using the ceramic resonators to be stabilized. When the oscillator is restarted by reset, apply "L" level to the RESET pin until the oscillation is stable since a wait time will not be generated.

### (2) Wait mode

If the WIT instruction is executed, the internal clock  $\phi$  stops at an "H" level, but the oscillator does not stop. The internal clock  $\phi$  restarts at reset or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

To ensure that the interrupts will be received to release the STP or WIT state, their interrupt enable bits must be set to "1" before executing of the STP or WIT instruction.

When releasing the STP state, the prescaler 12 and timer 1 will start counting the clock XIN divided by 16. Accordingly, set the timer 1 interrupt enable bit to "0" before executing the STP instruction.

### <Notes>

- If you switch the mode between middle/high-speed and low-speed, stabilize both XIN and XCIN oscillations. The sufficient time is required for the sub clock to stabilize, especially immediately after power on and at returning from stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency on condition that  $f(XIN) > 3 \times f(XCIN)$ .
- When using the quartz-crystal oscillator of high frequency, such as 16 MHz etc., it may be necessary to select a specific oscillator with the specification demanded.
- When using the oscillation stabilizing time set after STP instruction released bit set to "1", evaluate time to stabilize oscillation of the used oscillator and set the value to the timer 1 and prescaler 12.



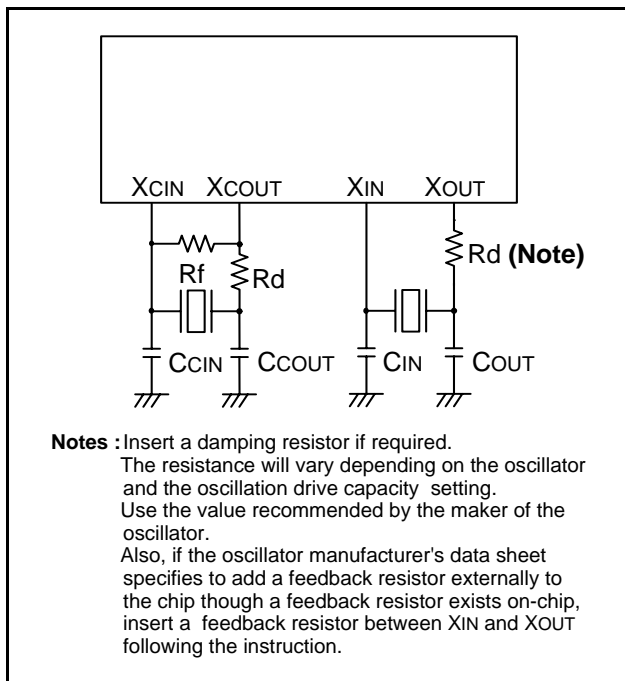


Fig 59. Ceramic resonator circuit

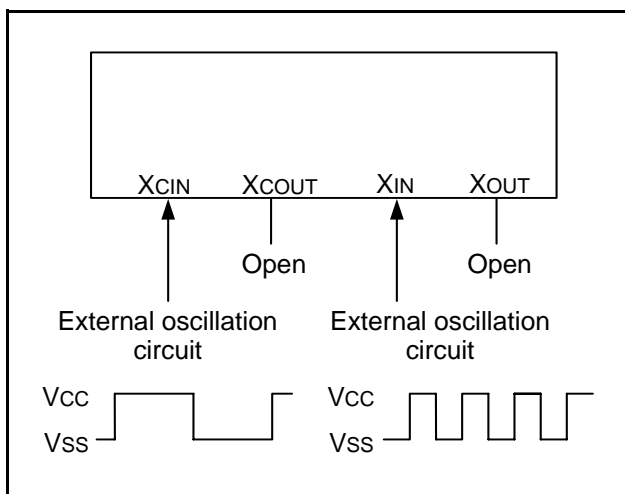


Fig 60. External clock input circuit

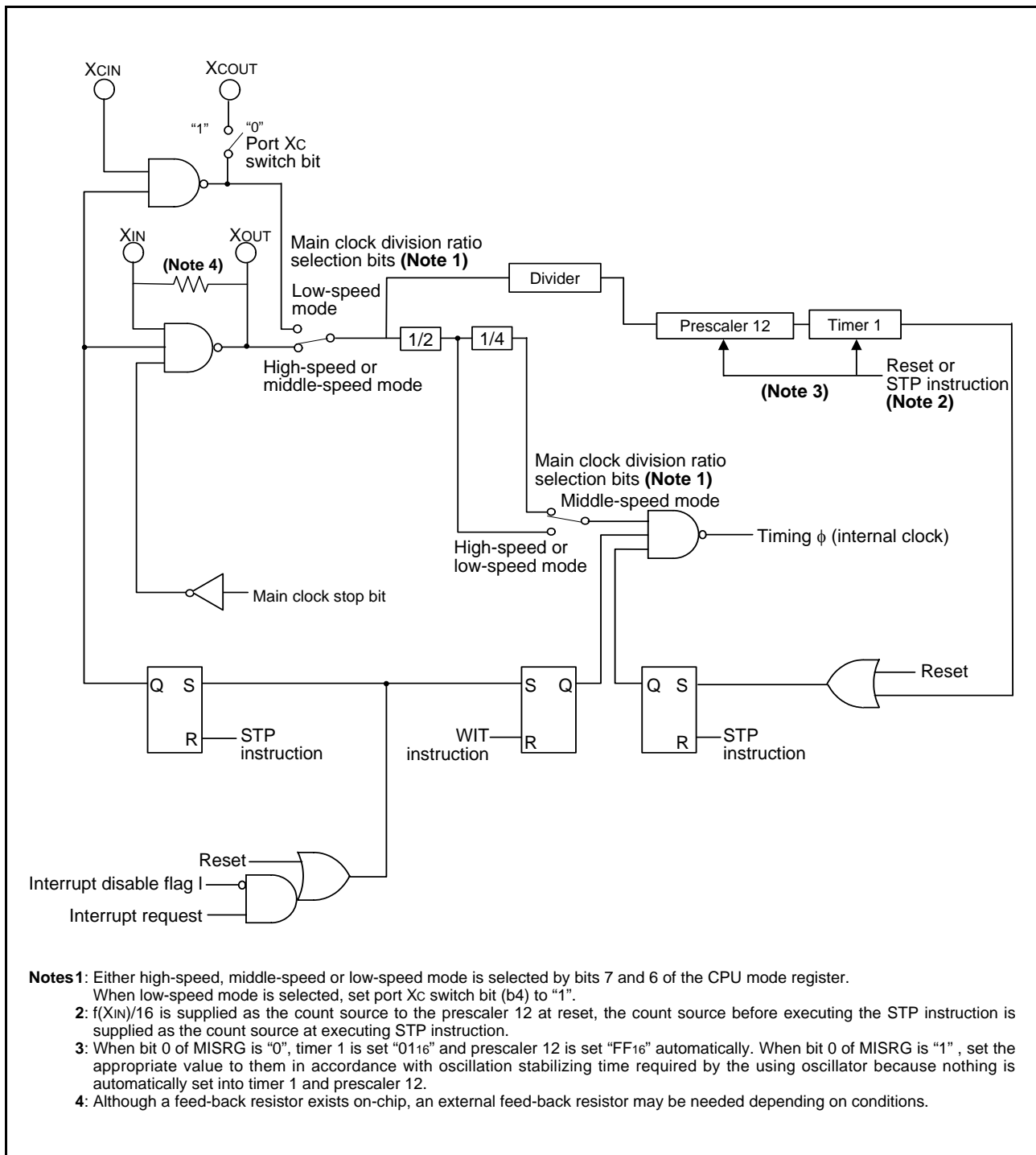


Fig 61. System clock generating circuit block diagram (Single-chip mode)

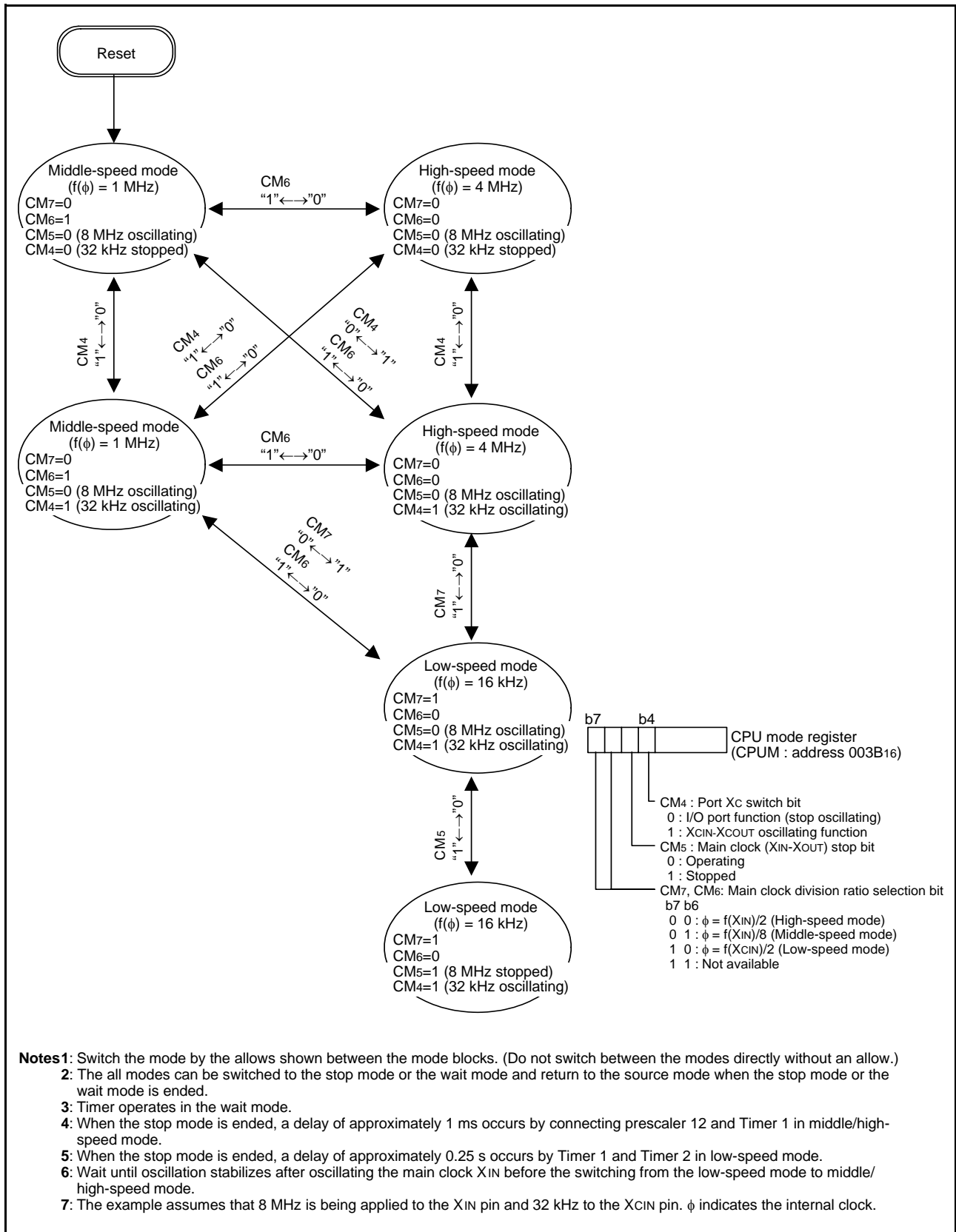


Fig 62. State transitions of system clock

## NOTES ON PROGRAMMING

### Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1". After a reset, initialize flags which affect program execution. In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

### Interrupts

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

### Decimal Calculations

- To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute an ADC or SBC instruction. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.
- In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

### Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is  $1/(n+1)$ .

### Multiplication and Division Instructions

- The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
- The execution of these instructions does not change the contents of the processor status register.

### Ports

The contents of the port direction registers cannot be read. The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is "1"
- The instruction with the addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instructions (ROR, CLB, or SEB, etc.) to a direction register.

Use instructions such as LDM and STA, etc., to set the port direction registers.

### Serial Interface

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the  $\overline{\text{SRDY}}$  signal, set the transmit enable bit, the receive enable bit, and the  $\overline{\text{SRDY}}$  output enable bit to "1".

Serial I/O1 continues to output the final bit from the TxD pin after transmission is completed. SOUT2 pin for serial I/O2 goes to high impedance after transfer is completed.

When in serial I/Os 1 and 3 (clock-synchronous mode) or in serial I/O2, an external clock is used as synchronous clock, write transmission data to the transmit buffer register or serial I/O2 register, during transfer clock is "H".

### A/D Converter

The comparator uses capacitive coupling amplifier whose charge will be lost if the clock frequency is too low.

Therefore, make sure that  $f(\text{XIN})$  in the middle/high-speed mode is at least on 500 kHz during an A/D conversion.

Do not execute the STP instruction during an A/D conversion.

### D/A Converter

The accuracy of the D/A converter becomes rapidly poor under the  $V_{CC} = 4.0$  V or less condition; a supply voltage of  $V_{CC} \geq 4.0$  V is recommended. When a D/A converter is not used, set all values of DAi conversion registers ( $i=1, 2$ ) to "0016".

### Instruction Execution Time

The instruction execution time is obtained by multiplying the period of the internal clock  $\phi$  by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction is shown in the list of machine instructions.

The period of the internal clock  $\phi$  is double of the XIN period in high-speed mode.

### Reserved Area, Reserved Bit

Do not write any data to the reserved area in the SFR area and the special page. (Do not change the contents after reset.)

### CPU Mode Register

Be sure to fix bit 3 of the CPU mode register (address 003B16) to "1".

## NOTES ON USAGE

### Termination of Unused Pins.

Be sure to perform the termination of unused pins.

### Handling of Power Source Pins

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (VCC pin) and GND pin (VSS pin), and between power source pin (VCC pin) and analog power source input pin (AVSS pin). Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of 0.01  $\mu\text{F}$ –0.1  $\mu\text{F}$  is recommended.

### Power Source Voltage

When the power source voltage value of a microcomputer is less than the value which is indicated as the recommended operating conditions, the microcomputer does not operate normally and may perform unstable operation.

In a system where the power source voltage drops slowly when the power source voltage drops or the power supply is turned off, reset a microcomputer when the power source voltage is less than the recommended operating conditions and design a system not to cause errors to the system by this unstable operation.

### Electric Characteristic Differences Between Flash Memory, Mask ROM and QzROM Version MCUs

There are differences in the manufacturing processes and the mask pattern among flash memory, mask ROM, and QzROM version MCUs due to the differences of the ROM type. Even when the ROM type is the same, when the memory size is different, the manufacturing processes and the mask pattern differ. For these reasons, the oscillation circuit constants and the characteristics such as a characteristic value, operation margin, noise immunity, and noise radiation within the limits of electrical characteristics may differ.

When manufacturing an application system, please perform sufficient evaluations in each product. Especially, when switching a product (example: change from the mask ROM version to QzROM version), please perform sufficient evaluations by the switching product in the stage before mass-producing an application system.

### Product Shipped in Blank

As for the product shipped in blank, Renesas does not perform the writing test to user ROM area after the assembly process though the QzROM writing test is performed enough before the assembly process. Therefore, a writing error of approx.0.1 % may occur. Moreover, please note the contact of cables and foreign bodies on a socket, etc. because a writing environment may cause some writing errors.

### QzROM Version

Connect the CNVSS/VPP pin the shortest possible to the GND pattern which is supplied to the VSS pin of the microcomputer. In addition connecting an approximately 5 k $\Omega$  resistor in series to the GND could improve noise immunity. In this case as well as the above mention, connect the pin the shortest possible to the GND pattern which is supplied to the VSS pin of the microcomputer.

#### • Reason

The CNVSS/VPP pin is the power source input pin for the built-in QzROM. When programming in the QzROM, the impedance of the VPP pin is low to allow the electric current for writing to flow into the built-in QzROM. Because of this, noise can enter easily. If noise enters the VPP pin, abnormal instruction codes or data are read from the QzROM, which may cause a program runaway.

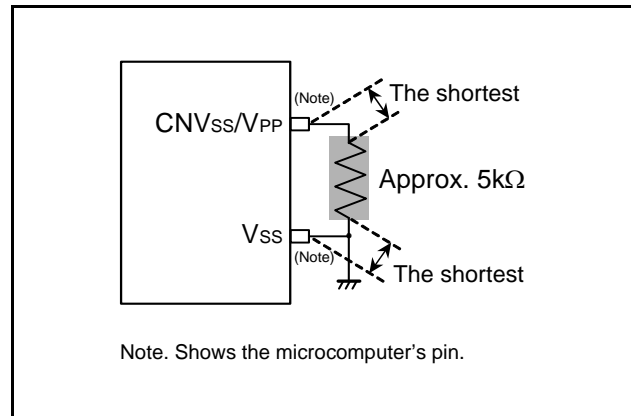


Fig 63. Wiring for the CNVSS/VPP

### Notes On QzROM Writing Orders

When ordering the QzROM product shipped after writing, submit the mask file (extension: .msk) which is made by the mask file converter MM.

Be sure to set the ROM option (“MASK option” written in the mask file converter) setup when making the mask file by using the mask file converter MM.

### Notes On ROM Code Protect

#### (QzROM product shipped after writing)

As for the QzROM product shipped after writing, the ROM code protect is specified according to the ROM option setup data in the mask file which is submitted at ordering.

Renesas Technology corp. uses the ROM option setup data at the ROM code protect address (address FFDB16) when writing to the QzROM. Consequently, the actual written value might differ from the ordered value as the contents of the ROM code protect address.

The ROM option setup data in the mask file is “0016” for protect enabled, “FE16” (protect enabled to the protect area 1 only) or “FF16” for protect disabled. Therefore, the contents of the ROM code protect address of the QzROM product shipped after writing are “0016”, “FE16” or “FF16”.

Note that the mask file which has nothing at the ROM option data or has the data other than “0016”, “FE16” and “FF16” can not be accepted.

### DATA REQUIRED FOR QzROM WRITING ORDERS

The following are necessary when ordering a QzROM product shipped after writing:

1. QzROM Writing Confirmation Form\*
2. Mark Specification Form\*
3. ROM data.....Mask file

\* For the QzROM writing confirmation form and the mark specification form, refer to the “Renesas Technology Corp.” Homepage (<http://www.renesas.com/homepage.jsp>).

Note that we cannot deal with special font marking (customer's trademark etc.) in QzROM microcomputer.

**ELECTRICAL CHARACTERISTICS**

**Absolute maximum ratings**

Table 10 Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>cc</sub>	Power source voltages	All voltages are based on V <sub>ss</sub> .	-0.3 to 6.5	V
V <sub>i</sub>	Input voltage P00-P07, P10-P17, P20-P27, P30, P31, P34-P37, P40-P47, P50-P57, P60-P67, V <sub>REF</sub>	When an input voltage is measured, output transistors are cut off.	-0.3 to V <sub>cc</sub> + 0.3	V
V <sub>i</sub>	Input voltage P32, P33		-0.3 to 5.8	V
V <sub>i</sub>	Input voltage $\overline{\text{RESET}}$ , X <sub>IN</sub>		-0.3 to V <sub>cc</sub> + 0.3	V
V <sub>i</sub>	Input voltage CNV <sub>ss</sub>		-0.3 to V <sub>cc</sub> + 0.3	V
V <sub>o</sub>	Output voltage P00-P07, P10-P17, P20-P27, P30, P31, P34-P37, P40-P47, P50-P57, P60-P67, X <sub>OUT</sub>		-0.3 to V <sub>cc</sub> + 0.3	V
V <sub>o</sub>	Output voltage P32, P33		-0.3 to 5.8	V
P <sub>d</sub>	Power dissipation	T <sub>a</sub> =25 °C	1000 <sup>(1)</sup>	mW
T <sub>opr</sub>	Operating temperature		-20 to 85	°C
T <sub>stg</sub>	Storage temperature		-65 to 125	°C

NOTES:

1. This value is 300 mW except SP package.

Recommended operating conditions

Table 11 Recommended operating conditions (1)  
(Vcc = 1.8 to 5.5 V, Vss = 0 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit	
			Min.	Typ.	Max.		
Vcc	Power source voltage <sup>(1)</sup>	When start oscillating <sup>(2)</sup>	2.2	5.0	5.5	V	
		High-speed mode f(φ) = f(XIN)/2	f(XIN) ≤ 2.1 MHz	2.0	5.0	5.5	V
			f(XIN) ≤ 4.2 MHz	2.2	5.0	5.5	
			f(XIN) ≤ 8.4 MHz	2.7	5.0	5.5	
			f(XIN) ≤ 12.5 MHz	4.0	5.0	5.5	
			f(XIN) ≤ 16.8 MHz	4.5	5.0	5.5	
		Middle-speed mode f(φ) = f(XIN)/8	f(XIN) ≤ 6.3 MHz	1.8	5.0	5.5	V
			f(XIN) ≤ 8.4 MHz	2.2	5.0	5.5	
			f(XIN) ≤ 12.5 MHz	2.7	5.0	5.5	
			f(XIN) ≤ 16.8 MHz	4.5	5.0	5.5	
Vss	Power source voltage		0		V		
VIH	"H" input voltage P00-P07, P10-P17, P20-P27, P30, P31, P34-P37, P40-P47, P50-P57, P60-P67	1.8 ≤ Vcc < 2.7 V	0.85 Vcc		Vcc	V	
		2.7 ≤ Vcc ≤ 5.5 V	0.8 Vcc		Vcc		
VIH	"H" input voltage P32, P33	1.8 ≤ Vcc < 2.7 V	0.85 Vcc		5.5	V	
		2.7 ≤ Vcc ≤ 5.5 V	0.8 Vcc		5.5		
VIH	"H" input voltage RESET, XIN, XCIN, CNVss	1.8 ≤ Vcc < 2.7 V	0.85 Vcc		Vcc	V	
		2.7 ≤ Vcc ≤ 5.5 V	0.8 Vcc		Vcc		
VIL	"L" input voltage P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67	1.8 ≤ Vcc < 2.7 V	0		0.16 Vcc	V	
		2.7 ≤ Vcc ≤ 5.5 V	0		0.2 Vcc		
VIL	"L" input voltage RESET, CNVss	1.8 ≤ Vcc < 2.7 V	0		0.16 Vcc	V	
		2.7 ≤ Vcc ≤ 5.5 V	0		0.2 Vcc		
VIL	"L" input voltage XIN, XCIN	1.8 ≤ Vcc ≤ 5.5 V	0		0.16 Vcc	V	
f(XIN)	Main clock input oscillation frequency <sup>(3)</sup>	High-speed mode f(φ) = f(XIN)/2	2.0 ≤ Vcc < 2.2 V		$\frac{(20 \times Vcc - 36) \times 1.05}{2}$	MHz	
			2.2 ≤ Vcc < 2.7 V		$\frac{(24 \times Vcc - 40.8) \times 1.05}{3}$	MHz	
			2.7 ≤ Vcc < 4.0 V		$\frac{(9 \times Vcc - 0.3) \times 1.05}{3}$	MHz	
			4.0 ≤ Vcc < 4.5 V		$\frac{(24 \times Vcc - 60) \times 1.05}{3}$	MHz	
			4.5 ≤ Vcc ≤ 5.5 V		16.8	MHz	
		Middle-speed mode f(φ) = f(XIN)/8	1.8 ≤ Vcc < 2.2 V		$\frac{(15 \times Vcc - 9) \times 1.05}{3}$	MHz	
			2.2 ≤ Vcc < 2.7 V		$\frac{(24 \times Vcc - 28.8) \times 1.05}{3}$	MHz	
			2.7 ≤ Vcc < 4.5 V		$\frac{(15 \times Vcc + 39) \times 1.1}{7}$	MHz	
			4.5 ≤ Vcc ≤ 5.5 V		16.8	MHz	
f(XCIN)	Sub-clock input oscillation frequency <sup>(3, 4)</sup>		32.768	50	kHz		

NOTES:

1. When using A/D converter, see A/D converter recommended operating conditions.
2. The start voltage and the start time for oscillation depend on the using oscillator, oscillation circuit constant value and operating temperature range, etc.. Particularly a high-frequency oscillator might require some notes in the low voltage operation.
3. When the oscillation frequency has a duty cycle of 50%.
4. When using the microcomputer in low-speed mode, set the sub-clock input oscillation frequency on condition that f(XCIN) < f(XIN)/3.

Table 12 Recommended operating conditions (2)  
(V<sub>CC</sub> = 1.8 to 5.5 V, V<sub>SS</sub> = 0V, T<sub>a</sub> = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit	
		Min.	Typ.	Max.		
ΣIOH(peak)	"H" total peak output current <sup>(1)</sup>	P00-P07, P10-P17, P20-P27, P30, P31, P34-P37			-80	mA
ΣIOH(peak)	"H" total peak output current <sup>(1)</sup>	P40-P47, P50-P57, P60-P67			-80	mA
ΣIOL(peak)	"L" total peak output current <sup>(1)</sup>	P00-P07, P10-P17, P30-P37			80	mA
ΣIOL(peak)	"L" total peak output current <sup>(1)</sup>	P20-P27			80	mA
ΣIOL(peak)	"L" total peak output current <sup>(1)</sup>	P40-P47, P50-P57, P60-P67			80	mA
ΣIOH(avg)	"H" total average output current <sup>(1)</sup>	P00-P07, P10-P17, P20-P27, P30, P31, P34-P37			-40	mA
ΣIOH(avg)	"H" total average output current <sup>(1)</sup>	P40-P47, P50-P57, P60-P67			-40	mA
ΣIOL(avg)	"L" total average output current <sup>(1)</sup>	P00-P07, P10-P17, P30-P37			40	mA
ΣIOL(avg)	"L" total average output current <sup>(1)</sup>	P20-P27			40	mA
ΣIOL(avg)	"L" total average output current <sup>(1)</sup>	P40-P47, P50-P57, P60-P67			40	mA
IOH(peak)	"H" peak output current <sup>(2)</sup>	P00-P07, P10-P17, P20-P27, P30, P31, P34-P37, P40-P47, P50-P57, P60-P67			-10	mA
IOL(peak)	"L" peak output current <sup>(2)</sup>	P00-P07, P10-P17, P30-P37, P40-P47, P50-P57, P60-P67			10	mA
IOL(peak)	"L" peak output current <sup>(2)</sup>	P20-P27			20	mA
IOH(avg)	"H" average output current <sup>(3)</sup>	P00-P07, P10-P17, P20-P27, P30, P31, P34-P37, P40-P47, P50-P57, P60-P67			-5	mA
IOL(avg)	"L" average output current <sup>(3)</sup>	P00-P07, P10-P17, P30-P37, P40-P47, P50-P57, P60-P67			5	mA
IOL(avg)	"L" average output current <sup>(3)</sup>	P20-P27			10	mA

## NOTES:

1. The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.
2. The peak output current is the peak current flowing in each port.
3. The average output current IOL(avg), IOH(avg) are average value measured over 100 ms.



**Electrical characteristics**

Table 13 Electrical characteristics (1)  
(V<sub>CC</sub> = 1.8 to 5.5 V, V<sub>SS</sub> = 0V, T<sub>a</sub> = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V <sub>OH</sub>	"H" output voltage <sup>(1)</sup> P00-P07, P10-P17, P20-P27, P30, P31, P34-P37, P40-P47, P50-P57, P60-P67	I <sub>OH</sub> = -10 mA V <sub>CC</sub> = 4.0 to 5.5 V	V <sub>CC</sub> - 2.0			V
		I <sub>OH</sub> = -1.0 mA V <sub>CC</sub> = 1.8 to 5.5 V	V <sub>CC</sub> - 1.0			
V <sub>OL</sub>	"L" output voltage P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67	I <sub>OL</sub> = 10 mA V <sub>CC</sub> = 4.0 to 5.5 V			2.0	V
		I <sub>OL</sub> = 1.6 mA V <sub>CC</sub> = 1.8 to 5.5 V			1.0	
V <sub>OL</sub>	"L" output voltage P20-P27	I <sub>OL</sub> = 20 mA V <sub>CC</sub> = 4.0 to 5.5 V			2.0	V
		I <sub>OL</sub> = 1.6 mA V <sub>CC</sub> = 1.8 to 5.5 V			0.4	
V <sub>T+</sub> - V <sub>T-</sub>	Hysteresis CNTR <sub>0</sub> , CNTR <sub>1</sub> , CNTR <sub>2</sub> , INT <sub>0</sub> -INT <sub>4</sub>			0.4		V
V <sub>T+</sub> - V <sub>T-</sub>	Hysteresis RxD <sub>1</sub> , SCLK <sub>1</sub> , SIN <sub>2</sub> , SCLK <sub>2</sub> , RxD <sub>3</sub> , SCLK <sub>3</sub>			0.5		V
V <sub>T+</sub> - V <sub>T-</sub>	Hysteresis RESET			0.5		V
I <sub>IH</sub>	"H" input current P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67	V <sub>I</sub> = V <sub>CC</sub> (Pin floating, Pull-up transistor "off")			5.0	μA
I <sub>IH</sub>	"H" input current RESET, CNV <sub>SS</sub>	V <sub>I</sub> = V <sub>CC</sub>			5.0	μA
I <sub>IH</sub>	"H" input current X <sub>IN</sub>	V <sub>I</sub> = V <sub>CC</sub>		4.0		μA
I <sub>IL</sub>	"L" input current P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67	V <sub>I</sub> = V <sub>CC</sub> (Pin floating, Pull-up transistor "off")			-5.0	μA
I <sub>IL</sub>	"L" input current RESET, CNV <sub>SS</sub>	V <sub>I</sub> = V <sub>SS</sub>			-5.0	μA
I <sub>IL</sub>	"L" input current X <sub>IN</sub>	V <sub>I</sub> = V <sub>SS</sub>		-4.0		μA
I <sub>IL</sub>	"L" input current (at Pull-up) P00-P07, P10-P17, P20-P27, P30, P31, P34-P37, P40-P47, P50-P57, P60-P67	V <sub>I</sub> = V <sub>SS</sub> V <sub>CC</sub> = 5.0 V	-80	-210	-420	μA
		V <sub>I</sub> = V <sub>SS</sub> V <sub>CC</sub> = 3.0 V	-30	-70	-140	
V <sub>RAM</sub>	RAM hold voltage	When clock stopped	1.8		V <sub>CC</sub>	V

NOTES:

1. P<sub>35</sub> is measured when the P<sub>35</sub>/TxD<sub>3</sub> P-channel output disable bit of the UART3 control register (bit 4 of address 00331<sub>6</sub>) is "0".  
P<sub>45</sub> is measured when the P<sub>45</sub>/TxD<sub>1</sub> P-channel output disable bit of the UART1 control register (bit 4 of address 001B1<sub>6</sub>) is "0".

Table 14 Electrical characteristics (2)  
 ( $V_{CC} = 1.8$  to  $5.5$  V,  $T_a = -20$  to  $85$  °C,  $f(X_{IN})=32.768$ kHz (Stopped in middle-speed mode),  
 Output transistors "off", AD converter not operated)

Symbol	Parameter	Test conditions			Limits			Unit	
					Min.	Typ.	Max.		
I <sub>CC</sub>	Power source current	High-speed mode	V <sub>CC</sub> = 5.0 V	f(X <sub>IN</sub> ) = 16.8 MHz		8.0	15.0	mA	
				f(X <sub>IN</sub> ) = 12.5 MHz		6.5	12.0		
				f(X <sub>IN</sub> ) = 8.4 MHz		5.0	9.0		
				f(X <sub>IN</sub> ) = 4.2 MHz		2.5	5.0		
				f(X <sub>IN</sub> ) = 16.8 MHz (in WIT state)		2.0	3.6		
			V <sub>CC</sub> = 3.0 V	f(X <sub>IN</sub> ) = 8.4 MHz		1.9	3.8	mA	
				f(X <sub>IN</sub> ) = 4.2 MHz		1.0	2.0		
				f(X <sub>IN</sub> ) = 2.1 MHz		0.6	1.2		
			Middle-speed mode	V <sub>CC</sub> = 5.0 V	f(X <sub>IN</sub> ) = 16.8 MHz		4.0	7.0	mA
					f(X <sub>IN</sub> ) = 12.5 MHz		3.0	6.0	
		f(X <sub>IN</sub> ) = 8.4 MHz				2.5	5.0		
		f(X <sub>IN</sub> ) = 16.8 MHz (in WIT state)				1.8	3.3		
		V <sub>CC</sub> = 3.0 V		f(X <sub>IN</sub> ) = 12.5 MHz		1.5	3.0	mA	
				f(X <sub>IN</sub> ) = 8.4 MHz		1.2	2.4		
		Low-speed mode	V <sub>CC</sub> = 5.0 V	f(X <sub>IN</sub> ) = stopped		55	200	μA	
				In WIT state		40	70		
			V <sub>CC</sub> = 3.0 V	f(X <sub>IN</sub> ) = stopped		15	40	μA	
				In WIT state		8	15		
			V <sub>CC</sub> = 2.0 V	f(X <sub>IN</sub> ) = stopped		6	15	μA	
				In WIT state		3	6		
In STP state (All oscillation stopped)		T <sub>a</sub> = 25 °C		0.1	1.0	μA			
		T <sub>a</sub> = 85 °C			10				
Increment when A/D conversion is executed		f(X <sub>IN</sub> ) = 16.8 MHz, V <sub>CC</sub> = 5.0 V In Middle-, high-speed mode		500		μA			

**A/D converter characteristics**

Table 15 A/D converter recommended operating conditions  
(VCC = 2.0 to 5.5 V, VSS = AVSS = 0 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
VCC	Power source voltage (When A/D converter is used)	8-bit A/D mode <sup>(1)</sup>	2.0	5.0	5.5	V
		10-bit A/D mode <sup>(2)</sup>	2.2	5.0	5.5	
VREF	Analog convert reference voltage		2.0		VCC	V
AVSS	Analog power source voltage			0		V
VIA	Analog input voltage AN0-AN15		0		VCC	V
f(XIN)	Main clock input oscillation frequency (When A/D converter is used)	2.0 ≤ VCC < 2.2 V	0.5		$\frac{(20 \times V_{CC} - 36) \times 1.05}{2}$	MHz
		2.2 ≤ VCC < 2.7 V	0.5		$\frac{(24 \times V_{CC} - 40.8) \times 1.05}{3}$	
		2.7 ≤ VCC < 4.0 V	0.5		$\frac{(9 \times V_{CC} - 0.3) \times 1.05}{3}$	
		4.0 ≤ VCC < 4.5 V	0.5		$\frac{(24.6 \times V_{CC} - 62.7) \times 1.05}{3}$	
		4.5 ≤ VCC ≤ 5.5 V	0.5		16.8	

NOTES:

1. 8-bit A/D mode: When the conversion mode selection bit (bit 7 of address 003816) is "1".
2. 10-bit A/D mode: When the conversion mode selection bit (bit 7 of address 003816) is "0".

Table 16 A/D converter characteristics  
(VCC = 2.0 to 5.5 V, VSS = AVSS = 0 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
-	Resolution		8-bit A/D mode <sup>(1)</sup>			8	bit
			10-bit A/D mode <sup>(2)</sup>			10	
-	Absolute accuracy (excluding quantization error)		8-bit A/D mode <sup>(1)</sup>	2.0 ≤ VREF < 2.2 V		±3	LSB
				2.2 ≤ VREF ≤ 5.5 V		±2	
			10-bit A/D mode <sup>(2)</sup>	2.2 ≤ VREF < 2.7 V		±5	LSB
				2.7 ≤ VREF ≤ 5.5 V		±4	
tCONV	Conversion time		8-bit A/D mode <sup>(1)</sup>			50	2tc(XIN)
			10-bit A/D mode <sup>(2)</sup>			61	
RLADDER	Ladder resistor			12	35	100	kΩ
IVREF	Reference power source input current	at A/D converter operated	VREF = 5.0 V	50	150	200	μA
		at A/D converter stopped	VREF = 5.0 V			5.0	μA
II(AD)	A/D port input current					5.0	μA

NOTES:

1. 8-bit A/D mode: When the conversion mode selection bit (bit 7 of address 003816) is "1".
2. 10-bit A/D mode: When the conversion mode selection bit (bit 7 of address 003816) is "0".

**D/A converter characteristics**

Table 17 D/A converter characteristics  
(VCC = 2.7 to 5.5 V, VREF = 2.7 V to VCC, VSS = AVSS = 0 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
-	Resolution				8	bit
-	Absolute accuracy		4.0 ≤ VREF ≤ 5.5 V		1.0	%
			2.7 ≤ VREF < 4.0 V		2.5	
tsu	Setting time				3	μs
RO	Output resistor		2	3.5	5	kΩ
IVREF	Reference power source input current <sup>(1)</sup>				3.2	mA

NOTES:

1. Using one D/A converter, with the value in the DA conversion register of the other D/A converter being "0016".

Timing requirements and switching characteristics

Table 18 Timing requirements (1)  
(Vcc = 2.0 to 5.5 V, Vss = 0V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
tw(RESET)	Reset input "L" pulse width		16			XIN cycle
tc(XIN)	Main clock XIN input cycle time	4.5 ≤ Vcc ≤ 5.5 V	59.5			ns
		4.0 ≤ Vcc < 4.5 V	10000/(86 Vcc - 219)			
		2.7 ≤ Vcc < 4.0 V	26 × 10 <sup>3</sup> /(82 Vcc - 3)			
		2.2 ≤ Vcc < 2.7 V	10000/(84 Vcc - 143)			
		2.0 ≤ Vcc < 2.2 V	10000/(105 Vcc - 189)			
twh(XIN)	Main clock XIN input "H" pulse width	4.5 ≤ Vcc ≤ 5.5 V	25			ns
		4.0 ≤ Vcc < 4.5 V	4000/(86 Vcc - 219)			
		2.7 ≤ Vcc < 4.0 V	10000/(82 Vcc - 3)			
		2.2 ≤ Vcc < 2.7 V	4000/(84 Vcc - 143)			
		2.0 ≤ Vcc < 2.2 V	4000/(105 Vcc - 189)			
twl(XIN)	Main clock XIN input "L" pulse width	4.5 ≤ Vcc ≤ 5.5 V	25			ns
		4.0 ≤ Vcc < 4.5 V	4000/(86 Vcc - 219)			
		2.7 ≤ Vcc < 4.0 V	10000/(82 Vcc - 3)			
		2.2 ≤ Vcc < 2.7 V	4000/(84 Vcc - 143)			
		2.0 ≤ Vcc < 2.2 V	4000/(105 Vcc - 189)			
tc(XCIN)	Sub-clock XCIN input cycle time		20			μs
twh(XCIN)	Sub-clock XCIN input "H" pulse width		5			μs
twl(XCIN)	Sub-clock XCIN input "L" pulse width		5			μs
tc(CNTR)	CNTR0–CNTR2 input cycle time	4.5 ≤ Vcc ≤ 5.5 V	120			ns
		4.0 ≤ Vcc < 4.5 V	160			
		2.7 ≤ Vcc < 4.0 V	250			
		2.2 ≤ Vcc < 2.7 V	500			
		2.0 ≤ Vcc < 2.2 V	1000			
twh(CNTR)	CNTR0–CNTR2 input "H" pulse width	4.5 ≤ Vcc ≤ 5.5 V	48			ns
		4.0 ≤ Vcc < 4.5 V	64			
		2.7 ≤ Vcc < 4.0 V	115			
		2.2 ≤ Vcc < 2.7 V	230			
		2.0 ≤ Vcc < 2.2 V	460			
twl(CNTR)	CNTR0–CNTR2 input "L" pulse width	4.5 ≤ Vcc ≤ 5.5 V	48			ns
		4.0 ≤ Vcc < 4.5 V	64			
		2.7 ≤ Vcc < 4.0 V	115			
		2.2 ≤ Vcc < 2.7 V	230			
		2.0 ≤ Vcc < 2.2 V	460			
twh(INT)	INT00, INT01, INT1, INT2, INT3, INT40, INT41 input "H" pulse width	4.5 ≤ Vcc ≤ 5.5 V	48			ns
		4.0 ≤ Vcc < 4.5 V	64			
		2.7 ≤ Vcc < 4.0 V	115			
		2.2 ≤ Vcc < 2.7 V	230			
		2.0 ≤ Vcc < 2.2 V	460			
twl(INT)	INT00, INT01, INT1, INT2, INT3, INT40, INT41 input "L" pulse width	4.5 ≤ Vcc ≤ 5.5 V	48			ns
		4.0 ≤ Vcc < 4.5 V	64			
		2.7 ≤ Vcc < 4.0 V	115			
		2.2 ≤ Vcc < 2.7 V	230			
		2.0 ≤ Vcc < 2.2 V	460			

Table 19 Timing requirements (2)  
(VCC = 2.0 to 5.5 V, VSS = 0V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tc(SCLK1) tc(SCLK3)	Serial I/O1, serial I/O3 clock input cycle time <sup>(1)</sup>	4.5 ≤ Vcc ≤ 5.5 V	250		ns
		4.0 ≤ Vcc < 4.5 V	320		
		2.7 ≤ Vcc < 4.0 V	500		
		2.2 ≤ Vcc < 2.7 V	1000		
		2.0 ≤ Vcc < 2.2 V	2000		
tWH(SCLK1) tWH(SCLK3)	Serial I/O1, serial I/O3 clock input "H" pulse width <sup>(1)</sup>	4.5 ≤ Vcc ≤ 5.5 V	120		ns
		4.0 ≤ Vcc < 4.5 V	150		
		2.7 ≤ Vcc < 4.0 V	240		
		2.2 ≤ Vcc < 2.7 V	480		
		2.0 ≤ Vcc < 2.2 V	950		
tWL(SCLK1) tWL(SCLK3)	Serial I/O1, serial I/O3 clock input "L" pulse width <sup>(1)</sup>	4.5 ≤ Vcc ≤ 5.5 V	120		ns
		4.0 ≤ Vcc < 4.5 V	150		
		2.7 ≤ Vcc < 4.0 V	240		
		2.2 ≤ Vcc < 2.7 V	480		
		2.0 ≤ Vcc < 2.2 V	950		
tsu(RxD1-SCLK1) tsu(RxD3-SCLK3)	Serial I/O1, serial I/O3 clock input setup time	4.5 ≤ Vcc ≤ 5.5 V	70		ns
		4.0 ≤ Vcc < 4.5 V	90		
		2.7 ≤ Vcc < 4.0 V	100		
		2.2 ≤ Vcc < 2.7 V	200		
		2.0 ≤ Vcc < 2.2 V	400		
th(SCLK1-RxD1) th(SCLK3-RxD3)	Serial I/O1, serial I/O3 clock input hold time	4.5 ≤ Vcc ≤ 5.5 V	32		ns
		4.0 ≤ Vcc < 4.5 V	40		
		2.7 ≤ Vcc < 4.0 V	50		
		2.2 ≤ Vcc < 2.7 V	100		
		2.0 ≤ Vcc < 2.2 V	200		
tc(SCLK2)	Serial I/O2 clock input cycle time	4.5 ≤ Vcc ≤ 5.5 V	500		ns
		4.0 ≤ Vcc < 4.5 V	650		
		2.7 ≤ Vcc < 4.0 V	1000		
		2.2 ≤ Vcc < 2.7 V	2000		
		2.0 ≤ Vcc < 2.2 V	4000		
tWH(SCLK2)	Serial I/O2 clock input "H" pulse width	4.5 ≤ Vcc ≤ 5.5 V	200		ns
		4.0 ≤ Vcc < 4.5 V	260		
		2.7 ≤ Vcc < 4.0 V	400		
		2.2 ≤ Vcc < 2.7 V	950		
		2.0 ≤ Vcc < 2.2 V	2000		
tWL(SCLK2)	Serial I/O2 clock input "L" pulse width	4.5 ≤ Vcc ≤ 5.5 V	200		ns
		4.0 ≤ Vcc < 4.5 V	260		
		2.7 ≤ Vcc < 4.0 V	400		
		2.2 ≤ Vcc < 2.7 V	950		
		2.0 ≤ Vcc < 2.2 V	2000		
tsu(SIN2-SCLK2)	Serial I/O2 clock input setup time	4.5 ≤ Vcc ≤ 5.5 V	100		ns
		4.0 ≤ Vcc < 4.5 V	130		
		2.7 ≤ Vcc < 4.0 V	200		
		2.2 ≤ Vcc < 2.7 V	400		
		2.0 ≤ Vcc < 2.2 V	800		
th(SCLK2-SIN2)	Serial I/O2 clock input hold time	4.5 ≤ Vcc ≤ 5.5 V	100		ns
		4.0 ≤ Vcc < 4.5 V	130		
		2.7 ≤ Vcc < 4.0 V	150		
		2.2 ≤ Vcc < 2.7 V	300		
		2.0 ≤ Vcc < 2.2 V	600		

NOTES:

- When bit 6 of address 001A<sub>16</sub> and bit 6 of address 0032<sub>16</sub> are "1" (clock synchronous).  
Divide this value by four when bit 6 of address 001A<sub>16</sub> and bit 6 of address 0032<sub>16</sub> are "0" (UART).

Table 20 Switching characteristics (1)  
(VCC = 2.0 to 5.5 V, VSS = 0V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t <sub>WH</sub> (SCLK1) t <sub>WH</sub> (SCLK3)	Serial I/O1, serial I/O3 clock output "H" pulse width	4.5 ≤ V <sub>CC</sub> ≤ 5.5 V 4.0 ≤ V <sub>CC</sub> < 4.5 V 2.7 ≤ V <sub>CC</sub> < 4.0 V 2.2 ≤ V <sub>CC</sub> < 2.7 V 2.0 ≤ V <sub>CC</sub> < 2.2 V	tc(SCLK1)/2-30, tc(SCLK3)/2-30 tc(SCLK1)/2-35, tc(SCLK3)/2-35 tc(SCLK1)/2-40, tc(SCLK3)/2-40 tc(SCLK1)/2-45, tc(SCLK3)/2-45 tc(SCLK1)/2-50, tc(SCLK3)/2-50			ns
t <sub>WL</sub> (SCLK1) t <sub>WL</sub> (SCLK3)	Serial I/O1, serial I/O3 clock output "L" pulse width	4.5 ≤ V <sub>CC</sub> ≤ 5.5 V 4.0 ≤ V <sub>CC</sub> < 4.5 V 2.7 ≤ V <sub>CC</sub> < 4.0 V 2.2 ≤ V <sub>CC</sub> < 2.7 V 2.0 ≤ V <sub>CC</sub> < 2.2 V	tc(SCLK1)/2-30, tc(SCLK3)/2-30 tc(SCLK1)/2-35, tc(SCLK3)/2-35 tc(SCLK1)/2-40, tc(SCLK3)/2-40 tc(SCLK1)/2-45, tc(SCLK3)/2-45 tc(SCLK1)/2-50, tc(SCLK3)/2-50			ns
t <sub>d</sub> (SCLK1-TxD1) t <sub>d</sub> (SCLK3-TxD3)	Serial I/O1, serial I/O3 output delay time <sup>(1)</sup>	4.5 ≤ V <sub>CC</sub> ≤ 5.5 V 4.0 ≤ V <sub>CC</sub> < 4.5 V 2.7 ≤ V <sub>CC</sub> < 4.0 V 2.2 ≤ V <sub>CC</sub> < 2.7 V 2.0 ≤ V <sub>CC</sub> < 2.2 V			140	ns
					200	
					350	
					400	
					420	
t <sub>v</sub> (SCLK1-TxD1) t <sub>v</sub> (SCLK3-TxD3)	Serial I/O1, serial I/O3 output valid time <sup>(1)</sup>	4.5 ≤ V <sub>CC</sub> ≤ 5.5 V 4.0 ≤ V <sub>CC</sub> < 4.5 V 2.7 ≤ V <sub>CC</sub> < 4.0 V 2.2 ≤ V <sub>CC</sub> < 2.7 V 2.0 ≤ V <sub>CC</sub> < 2.2 V	-30 -30 -30 -30 -30			ns
t <sub>r</sub> (SCLK1) t <sub>r</sub> (SCLK3)	Serial I/O1, serial I/O3 rise time of clock output	4.5 ≤ V <sub>CC</sub> ≤ 5.5 V 4.0 ≤ V <sub>CC</sub> < 4.5 V 2.7 ≤ V <sub>CC</sub> < 4.0 V 2.2 ≤ V <sub>CC</sub> < 2.7 V 2.0 ≤ V <sub>CC</sub> < 2.2 V			30	ns
					35	
					40	
					45	
					50	
t <sub>f</sub> (SCLK1) t <sub>f</sub> (SCLK3)	Serial I/O1, serial I/O3 fall time of clock output	4.5 ≤ V <sub>CC</sub> ≤ 5.5 V 4.0 ≤ V <sub>CC</sub> < 4.5 V 2.7 ≤ V <sub>CC</sub> < 4.0 V 2.2 ≤ V <sub>CC</sub> < 2.7 V 2.0 ≤ V <sub>CC</sub> < 2.2 V			30	ns
					35	
					40	
					45	
					50	
t <sub>WH</sub> (SCLK2)	Serial I/O2 clock output "H" pulse width	4.5 ≤ V <sub>CC</sub> ≤ 5.5 V 4.0 ≤ V <sub>CC</sub> < 4.5 V 2.7 ≤ V <sub>CC</sub> < 4.0 V 2.2 ≤ V <sub>CC</sub> < 2.7 V 2.0 ≤ V <sub>CC</sub> < 2.2 V	tc(SCLK2)/2-160 tc(SCLK2)/2-200 tc(SCLK2)/2-240 tc(SCLK2)/2-260 tc(SCLK2)/2-280			ns
t <sub>WL</sub> (SCLK2)	Serial I/O2 clock output "L" pulse width	4.5 ≤ V <sub>CC</sub> ≤ 5.5 V 4.0 ≤ V <sub>CC</sub> < 4.5 V 2.7 ≤ V <sub>CC</sub> < 4.0 V 2.2 ≤ V <sub>CC</sub> < 2.7 V 2.0 ≤ V <sub>CC</sub> < 2.2 V	tc(SCLK2)/2-160 tc(SCLK2)/2-200 tc(SCLK2)/2-240 tc(SCLK2)/2-260 tc(SCLK2)/2-280			ns
t <sub>d</sub> (SCLK2-SOUT2)	Serial I/O2 output delay time	4.5 ≤ V <sub>CC</sub> ≤ 5.5 V 4.0 ≤ V <sub>CC</sub> < 4.5 V 2.7 ≤ V <sub>CC</sub> < 4.0 V 2.2 ≤ V <sub>CC</sub> < 2.7 V 2.0 ≤ V <sub>CC</sub> < 2.2 V			200	ns
					250	
					300	
					350	
					400	
t <sub>v</sub> (SCLK2-SOUT2)	Serial I/O2 output valid time	4.5 ≤ V <sub>CC</sub> ≤ 5.5 V 4.0 ≤ V <sub>CC</sub> < 4.5 V 2.7 ≤ V <sub>CC</sub> < 4.0 V 2.2 ≤ V <sub>CC</sub> < 2.7 V 2.0 ≤ V <sub>CC</sub> < 2.2 V		0		ns
				0		
				0		
				0		
				0		

Fig.64

NOTES:

1. When the P45/TxD1 P-channel output disable bit of the UART1 control register (bit 4 of address 001B16) is "0".

Table 21 Switching characteristics (2)  
( $V_{CC} = 2.0$  to  $5.5$  V,  $V_{SS} = 0$  V,  $T_a = -20$  to  $85$  °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
$t_f(\text{SCLK2})$	Serial I/O2 fall time of clock output	$4.5 \leq V_{CC} \leq 5.5$ V	Fig.64			30	ns
		$4.0 \leq V_{CC} < 4.5$ V				35	
		$2.7 \leq V_{CC} < 4.0$ V				40	
		$2.2 \leq V_{CC} < 2.7$ V				45	
		$2.0 \leq V_{CC} < 2.2$ V				50	
$t_r(\text{CMOS})$	CMOS rise time of output <sup>(1)</sup>	$4.5 \leq V_{CC} \leq 5.5$ V			10	30	ns
		$4.0 \leq V_{CC} < 4.5$ V			12	35	
		$2.7 \leq V_{CC} < 4.0$ V			15	40	
		$2.2 \leq V_{CC} < 2.7$ V			17	45	
		$2.0 \leq V_{CC} < 2.2$ V			20	50	
$t_f(\text{CMOS})$	CMOS fall time of output <sup>(1)</sup>	$4.5 \leq V_{CC} \leq 5.5$ V			10	30	ns
		$4.0 \leq V_{CC} < 4.5$ V			12	35	
		$2.7 \leq V_{CC} < 4.0$ V			15	40	
		$2.2 \leq V_{CC} < 2.7$ V			17	45	
		$2.0 \leq V_{CC} < 2.2$ V			20	50	

## NOTES:

- When the P35/TxD3 P4-channel output disable bit of the UART3 control register (bit 4 of address 003316) is "0".

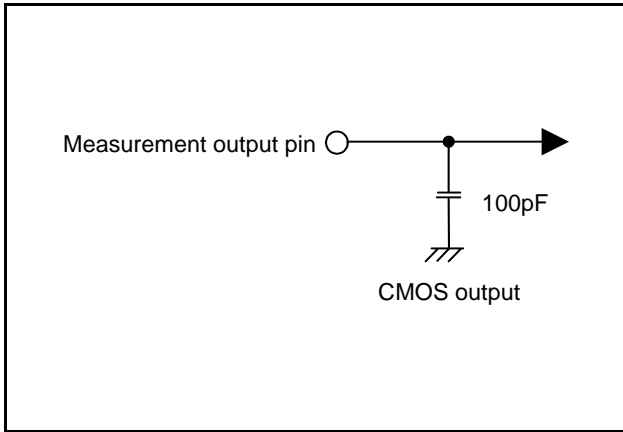


Fig 64. Circuit for measuring output switching characteristics (1)

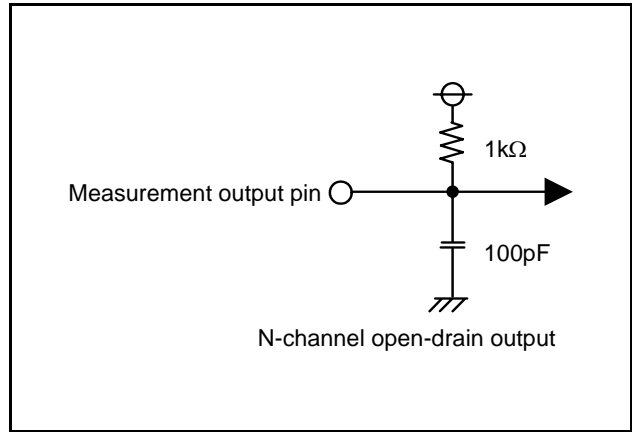


Fig 65. Circuit for measuring output switching characteristics (2)



### Single-chip mode timing diagram

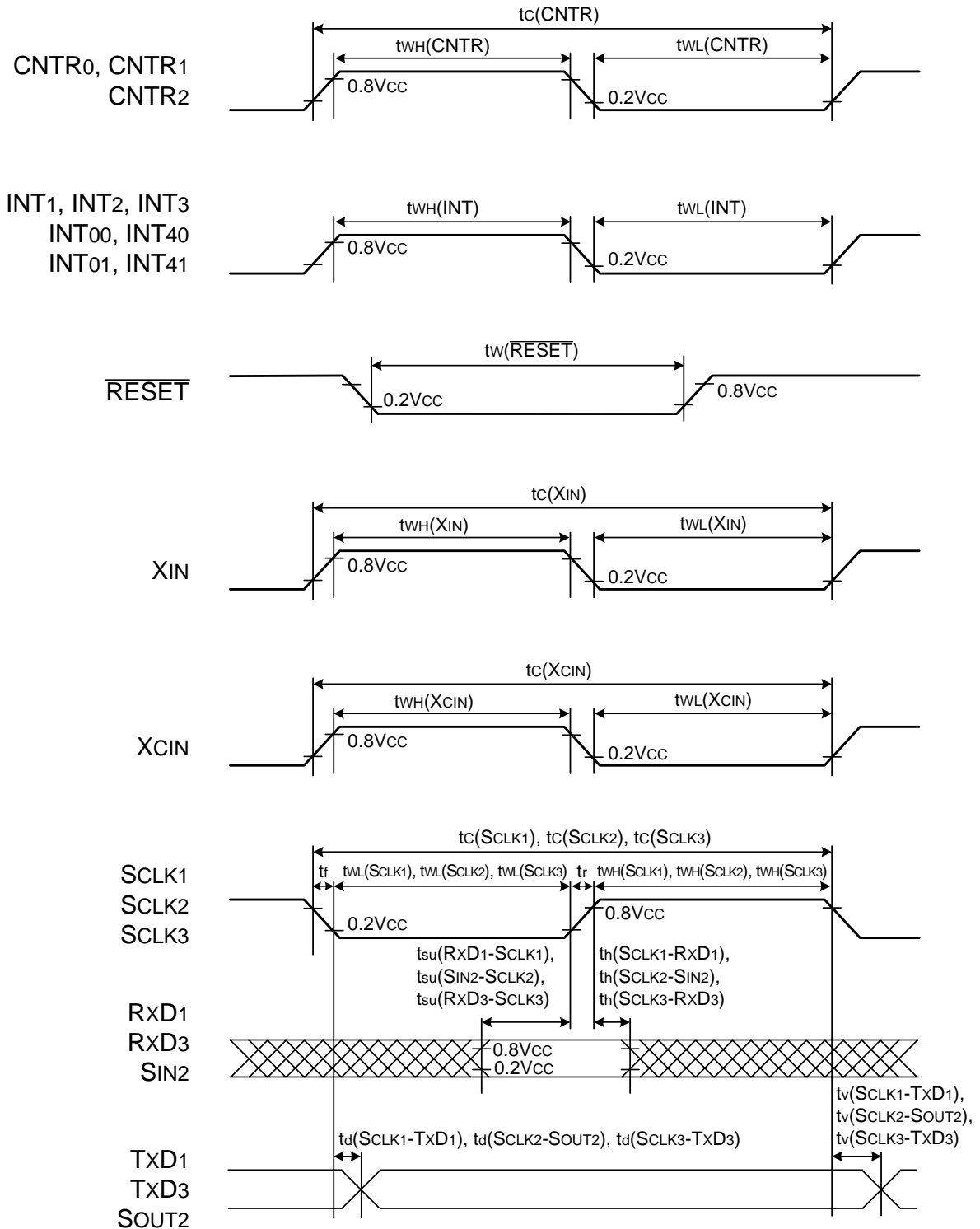
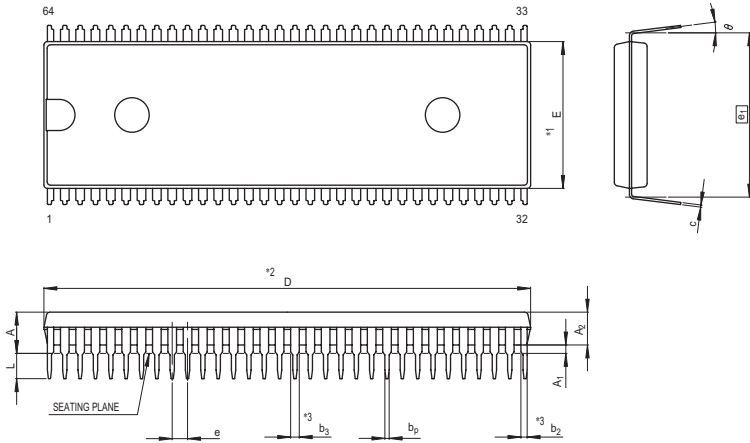


Fig 66. Timing diagram (in single-chip mode)

PACKAGE OUTLINE

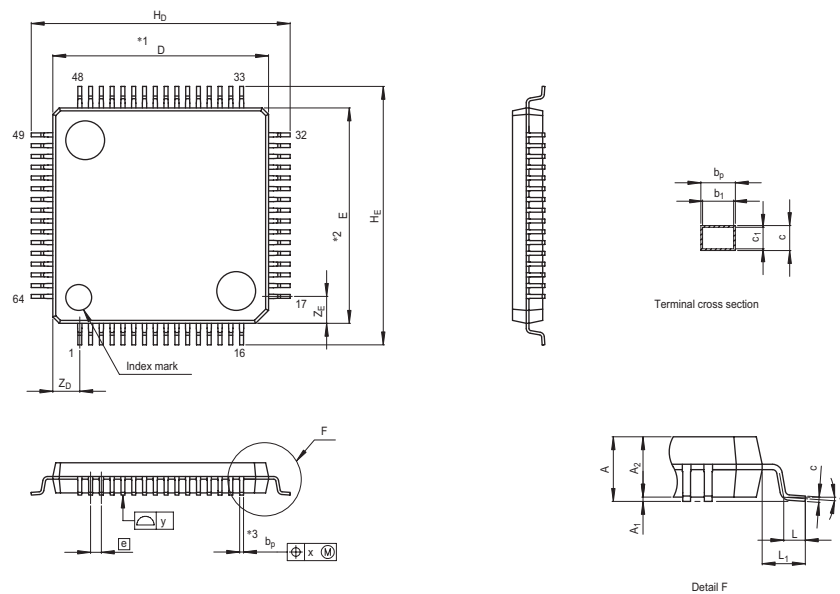
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SDIP64-17x56.4-1.78	PRDP0064BA-A	64P4B	7.9g



NOTE)  
1. DIMENSIONS \*\*1\* AND \*\*2\*  
DO NOT INCLUDE MOLD FLASH.  
2. DIMENSION \*\*3\* DOES NOT  
INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
$\bar{e}$	18.75	19.05	19.35
D	56.2	56.4	56.6
E	16.85	17.0	17.15
A	—	—	5.08
A <sub>1</sub>	0.38	—	—
A <sub>2</sub>	—	3.8	—
b <sub>p</sub>	0.4	0.5	0.6
b <sub>2</sub>	0.65	0.75	1.05
b <sub>3</sub>	0.9	1.0	1.3
c	0.2	0.25	0.32
$\theta$	0°	—	15°
e	1.528	1.778	2.028
L	2.8	—	—

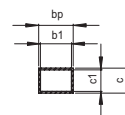
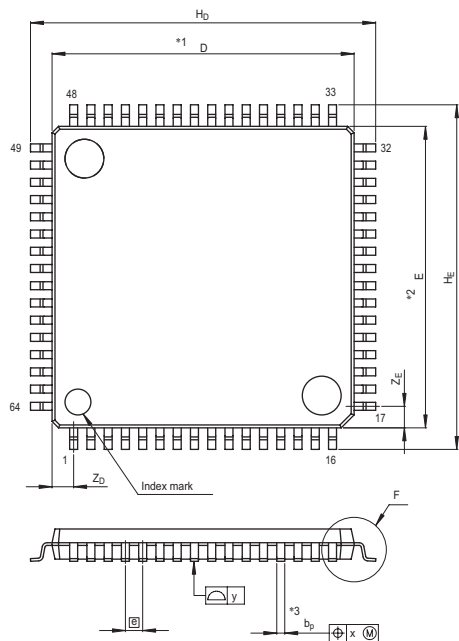
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g



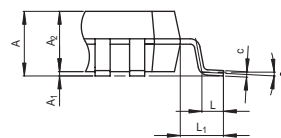
NOTE)  
1. DIMENSIONS \*\*1\* AND \*\*2\*  
DO NOT INCLUDE MOLD FLASH.  
2. DIMENSION \*\*3\* DOES NOT  
INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A <sub>2</sub>	—	1.4	—
H <sub>D</sub>	11.8	12.0	12.2
H <sub>E</sub>	11.8	12.0	12.2
A	—	—	1.7
A <sub>1</sub>	0.05	0.1	0.15
b <sub>p</sub>	0.15	0.20	0.25
b <sub>1</sub>	—	0.18	—
c	0.09	0.145	0.20
c <sub>1</sub>	—	0.125	—
$\theta$	0°	—	8°
$\bar{e}$	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z <sub>D</sub>	—	1.25	—
Z <sub>E</sub>	—	1.25	—
L	0.35	0.5	0.65
L <sub>1</sub>	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-14x14-0.80	PLQP0064GA-A	64P6U-A	0.7g



Terminal cross section



Detail F

NOTE)  
1. DIMENSIONS \*\*1\* AND \*\*2\*  
DO NOT INCLUDE MOLD FLASH.  
2. DIMENSION \*\*3\* DOES NOT  
INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A <sub>2</sub>	—	1.4	—
H <sub>D</sub>	15.8	16.0	16.2
H <sub>E</sub>	15.8	16.0	16.2
A	—	—	1.7
A <sub>1</sub>	0	0.1	0.2
b <sub>p</sub>	0.32	0.37	0.42
b <sub>1</sub>	—	0.35	—
c	0.09	0.145	0.20
c <sub>1</sub>	—	0.125	—
φ	0°	—	8°
Ⓜ	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z <sub>D</sub>	—	1.0	—
Z <sub>E</sub>	—	1.0	—
L	0.3	0.5	0.7
L <sub>1</sub>	—	1.0	—

## APPENDIX

## NOTES ON PROGRAMMING

## 1. Processor Status Register

## (1) Initializing of processor status register

Flags which affect program execution must be initialized after a reset. In particular, it is essential to initialize the T and D flags because they have an important effect on calculations.

<Reason>

After a reset, the contents of the processor status register (PS) are undefined except for the I flag which is "1".

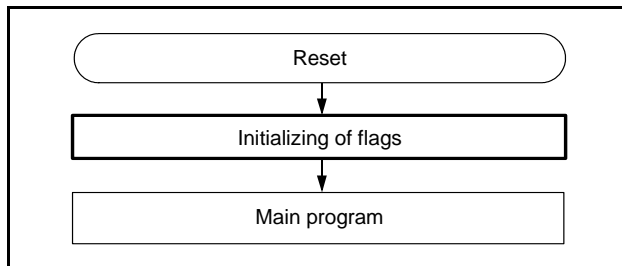


Fig 1. Initialization of processor status register

## (2) How to reference the processor status register

To reference the contents of the processor status register (PS), execute the PHP instruction once then read the contents of (S+1). If necessary, execute the PLP instruction to return the PS to its original status.

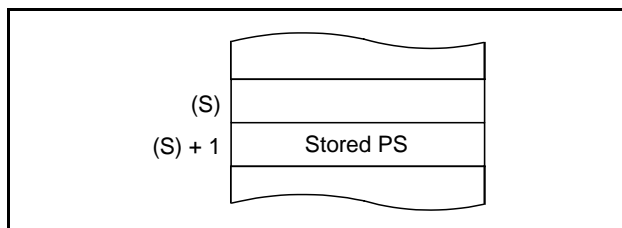


Fig 2. Stack memory contents after PHP instruction execution

## 2. BRK instruction

## (1) Interrupt priority level

When the BRK instruction is executed with the following conditions satisfied, the interrupt execution is started from the address of interrupt vector which has the highest priority.

- Interrupt request bit and interrupt enable bit are set to "1".
- Interrupt disable flag (I) is set to "1" to disable interrupt.

## 3. Decimal calculations

## (1) Execution of decimal calculations

The ADC and SBC are the only instructions which will yield proper decimal notation, set the decimal mode flag (D) to "1" with the SED instruction. After executing the ADC or SBC instruction, execute another instruction before executing the SEC, CLC, or CLD instruction.

## (2) Notes on status flag in decimal mode

When decimal mode is selected, the values of three of the flags in the status register (the N, V, and Z flags) are invalid after a ADC or SBC instruction is executed.

The carry flag (C) is set to "1" if a carry is generated as a result of the calculation, or is cleared to "0" if a borrow is generated. To determine whether a calculation has generated a carry, the C flag must be initialized to "0" before each calculation. To check for a borrow, the C flag must be initialized to "1" before each calculation.

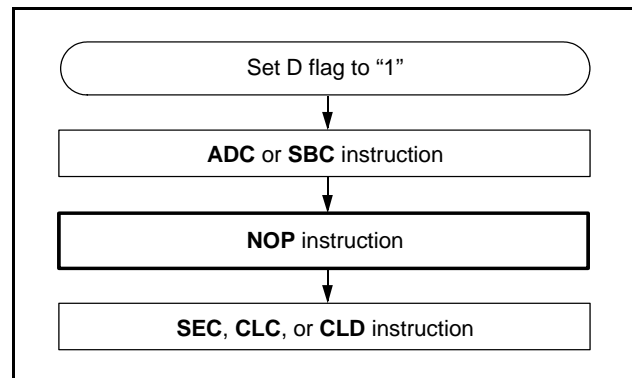


Fig 3. Execution of decimal calculations

## 4. JMP instruction

When using the JMP instruction in indirect addressing mode, do not specify the last address on a page as an indirect address.

## 5. Multiplication and Division Instructions

- The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
- The execution of these instructions does not change the contents of the processor status register.

## 6. Ports

The contents of the port direction registers cannot be read. The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is "1"
- The instruction with the addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instructions (ROR, CLB, or SEB, etc.) to a direction register.

Use instructions such as LDM and STA, etc., to set the port direction registers.

## 7. Instruction Execution Timing

The instruction execution time can be obtained by multiplying the frequency of the internal clock  $\phi$  by the number of cycles mentioned in the 740 Family Software Manual.

The frequency of the internal clock  $\phi$  is the twice the  $X_{IN}$  cycle in high-speed mode, 8 times the  $X_{IN}$  cycle in middle-speed mode, and the twice the  $X_{CIN}$  in low-speed mode.

## 8. Reserved Area, Reserved Bit

Do not write any data to the reserved area in the SFR area and the special page. (Do not change the contents after reset.)

## 9. CPU Mode Register

Be sure to fix bit 3 of the CPU mode register (address 003B16) to "1".

**NOTES ON PERIPHERAL FUNCTIONS****Notes on Input and Output Ports****1. Notes in standby state**

In standby state<sup>\*1</sup> for low-power dissipation, do not make input levels of an I/O port “undefined”. Even when an I/O port of Nchannel open-drain is set as output mode, if output data is “1”, the aforementioned notes are necessary.

Pull-up (connect the port to VCC) or pull-down (connect the port to VSS) these ports through a resistor.

When determining a resistance value, note the following points:

- External circuit
- Variation of output levels during the ordinary operation

When using built-in pull-up resistor, note on varied current values:

- When setting as an input port : Fix its input level
- When setting as an output port : Prevent current from flowing out to external

<Reason>

Exclusive input ports are always in a high-impedance state. An output transistor becomes an OFF state when an I/O port is set as input mode by the direction register, so that the port enter a highimpedance state. At this time, the potential which is input to the input buffer in a microcomputer is unstable in the state that input levels are “undefined”. This may cause power source current.

Even when an I/O port of N-channel open-drain is set as output mode by the direction register, if the contents of the port latch is “1”, the same phenomenon as that of an input port will occur.

**NOTES:**

1. Standby state : stop mode by executing STP instruction  
wait mode by executing WIT instruction

**2. Modifying output data with bit managing instruction**

When the port latch of an I/O port is modified with the bit managing instruction<sup>\*2</sup>, the value of the unspecified bit may be changed.

<Reason>

The bit managing instructions are read-modify-write form instructions for reading and writing data by a byte unit. Accordingly, when these instructions are executed on a bit of the port latch of an I/O port, the following is executed to all bits of the port latch.

- As for bit which is set for input port:  
The pin state is read in the CPU, and is written to this bit after bit managing.
- As for bit which is set for output port:  
The bit value is read in the CPU, and is written to this bit after bit managing.

Note the following:

- Even when a port which is set as an output port is changed for an input port, its port latch holds the output data.
- As for a bit of which is set for an input port, its value may be changed even when not specified with a bit managing instruction in case where the pin state differs from its port latch contents.

**NOTES:**

2. Bit managing instructions : SEB, and CLB instructions

**Termination of Unused Pins****1. Terminate unused pins**

(1) Output ports : Open

(2) I/O ports :

- Set the I/O ports for the input mode and connect them to VCC or VSS through each resistor of 1 kΩ to 10 kΩ

Ports that permit the selecting of a built-in pull-up resistor can also use this resistor. Set the I/O ports for the output mode and open them at “L” or “H”.

- When opening them in the output mode, the input mode of the initial status remains until the mode of the ports is switched over to the output mode by the program after reset. Thus, the potential at these pins is undefined and the power source current may increase in the input mode. With regard to an effects on the system, thoroughly perform system evaluation on the user side.
- Since the direction register setup may be changed because of a program runaway or noise, set direction registers by program periodically to increase the reliability of program.

(3) The AVSS pin when not using the A/D converter :

- When not using the A/D converter, handle a power source pin for the A/D converter, AVSS pin as follows:  
AVSS: Connect to the VSS pin.

**2. Termination remarks**

(1) I/O ports :

Do not open in the input mode.

<Reason>

- The power source current may increase depending on the firststage circuit.
- An effect due to noise may be easily produced as compared with proper termination (2) in 1 and shown on the above.

(2) I/O ports :

When setting for the input mode, do not connect to VCC or VSS directly.

<Reason>

If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur between a port and VCC (or VSS).

(3) I/O ports :

When setting for the input mode, do not connect multiple ports in a lump to VCC or VSS through a resistor.

<Reason>

If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur between ports.

- At the termination of unused pins, perform wiring at the shortest possible distance (20 mm or less) from micro-computer pins.

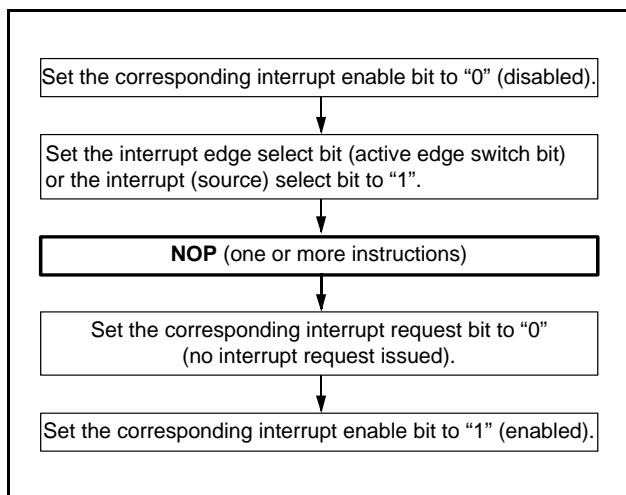
**Notes on Interrupts**

**1. Change of relevant register settings**

When the setting of the following registers or bits is changed, the interrupt request bit may be set to "1". When not requiring the interrupt occurrence synchronized with these setting, take the following sequence.

- Interrupt edge selection register (address 003A16)
- Timer XY mode register (address 002316)
- Timer Z mode register (address 002A16)

Set the above listed registers or bits as the following sequence.



**Fig 4. Sequence of changing relevant register**

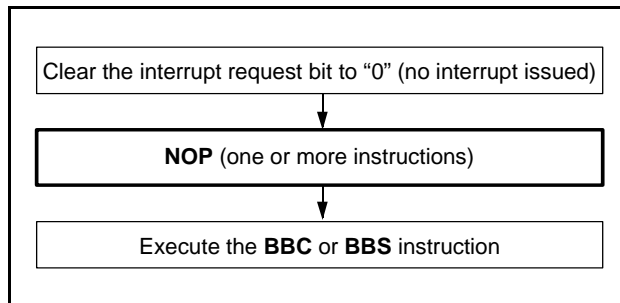
<Reason>

When setting the followings, the interrupt request bit may be set to "1".

- When setting external interrupt active edge  
 Concerned register: Interrupt edge selection register (address 003A16)  
 Timer XY mode register (address 002316)  
 Timer Z mode register (address 002A16)
- When switching interrupt sources of an interrupt vector address where two or more interrupt sources are allocated.  
 Concerned register: Interrupt source selection register (address 003916)

**2. Check of interrupt request bit**

When executing the BBC or BBS instruction to an interrupt request bit of an interrupt request register immediately after this bit is set to "0", execute one or more instructions before executing the BBC or BBS instruction.



**Fig 5. Sequence of check of interrupt request bit**

<Reason>

If the BBC or BBS instruction is executed immediately after an interrupt request bit of an interrupt request register is cleared to "0", the value of the interrupt request bit before being cleared to "0" is read.

**Notes on 8-bit Timer (timer 1, 2, X, Y)**

- If a value  $n$  (between 0 and 255) is written to a timer latch, the frequency division ratio is  $1/(n+1)$ .
- When switching the count source by the timer 12, X and Y count source selection bits, the value of timer count is altered in unconsiderable amount owing to generating of thin pulses in the count input signals.  
Therefore, select the timer count source before set the value to the prescaler and the timer.
- Set the double-function port of the CNTR0/CNTR1 pin and port P54/P55 to output in the pulse output mode.
- Set the double-function port of CNTR0/CNTR1 pin and port P54/P55 to input in the event counter mode and the pulse width measurement mode.

**Notes on 16-bit Timer (timer Z)****1. Pulse output mode**

- Set the double-function port of the CNTR2 pin and port P47 to output.

**2. Pulse period measurement mode**

- Set the double-function port of the CNTR2 pin and port P47 to input.
- A read-out of timer value is impossible in this mode. The timer can be written to only during timer stop (no measurement of pulse period).
- Since the timer latch in this mode is specialized for the read-out of measured values, do not perform any write operation during measurement.
- “FFFF16” is set to the timer when the timer underflows or when the valid edge of measurement start/completion is detected.  
Consequently, the timer value at start of pulse period measurement depends on the timer value just before measurement start.

**3. Pulse width measurement mode**

- Set the double-function port of the CNTR2 pin and port P47 to input.
- A read-out of timer value is impossible in this mode. The timer can be written to only during timer stop (no measurement of pulse period).
- Since the timer latch in this mode is specialized for the read-out of measured values, do not perform any write operation during measurement.
- “FFFF16” is set to the timer when the timer underflows or when the valid edge of measurement start/completion is detected.  
Consequently, the timer value at start of pulse width measurement depends on the timer value just before measurement start.

**4. Programmable waveform generating mode**

- Set the double-function port of the CNTR2 pin and port P47 to output.

**5. Programmable one-shot generating mode**

- Set the double-function port of CNTR2 pin and port P47 to output, and of INT1 pin and port P42 to input in this mode.
- This mode cannot be used in low-speed mode.
- If the value of the CNTR2 active edge switch bit is changed during one-shot generating enabled or generating one-shot pulse, then the output level from CNTR2 pin changes.

**6. All modes**

- Timer Z write control

Which write control can be selected by the timer Z write control bit (bit 3) of the timer Z mode register (address 002A16), writing data to both the latch and the timer at the same time or writing data only to the latch.

When the operation “writing data only to the latch” is selected, the value is set to the timer latch by writing data to the address of timer Z and the timer is updated at next underflow. After reset release, the operation “writing data to both the latch and the timer at the same time” is selected, and the value is set to both the latch and the timer at the same time by writing data to the address of timer Z.

In the case of writing data only to the latch, if writing data to the latch and an underflow are performed almost at the same time, the timer value may become undefined.

- Timer Z read control

A read-out of timer value is impossible in pulse period measurement mode and pulse width measurement mode. In the other modes, a read-out of timer value is possible regardless of count operating or stopped.

However, a read-out of timer latch value is impossible.

- Switch of interrupt active edge of CNTR2 and INT1

Each interrupt active edge depends on setting of the CNTR2 active edge switch bit and the INT1 active edge selection bit.

- Switch of count source

When switching the count source by the timer Z count source selection bits, the value of timer count is altered in inconsiderable amount owing to generating of thin pulses on the count input signals.

Therefore, select the timer count source before setting the value to the prescaler and the timer.



## Notes on Serial Interface

### 1. Notes when selecting clock synchronous serial I/O

#### (1) Stop of transmission operation

As for serial I/O<sub>i</sub> (i = 1, 3) that can be used as either a clock synchronous or an asynchronous (UART) serial I/O, clear the serial I/O<sub>i</sub> enable bit and the transmit enable bit to "0" (serial I/O<sub>i</sub> and transmit disabled).

<Reason>

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O<sub>i</sub> enable bit is cleared to "0" (serial I/O<sub>i</sub> disabled), the internal transmission is running (in this case, since pins TxDi, RxDi, SCLKi, and  $\overline{\text{SRDY}}_i$  function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O<sub>i</sub> enable bit is set to "1" at this time, the data during internally shifting is output to the TxDi pin and an operation failure occurs.

#### (2) Stop of receive operation

As for serial I/O<sub>i</sub> (i = 1, 3) that can be used as either a clock synchronous or an asynchronous (UART) serial I/O, clear the receive enable bit to "0" (receive disabled), or clear the serial I/O<sub>i</sub> enable bit to "0" (serial I/O<sub>i</sub> disabled).

#### (3) Stop of transmit/receive operation

As for serial I/O<sub>i</sub> (i = 1, 3) that can be used as either a clock synchronous or an asynchronous (UART) serial I/O, clear both the transmit enable bit and receive enable bit to "0" (transmit and receive disabled).

(when data is transmitted and received in the clock synchronous serial I/O mode, any one of data transmission and reception cannot be stopped.)

<Reason>

In the clock synchronous serial I/O mode, the same clock is used for transmission and reception. If any one of transmission and reception is disabled, a bit error occurs because transmission and reception cannot be synchronized.

In this mode, the clock circuit of the transmission circuit also operates for data reception. Accordingly, the transmission circuit does not stop by clearing only the transmit enable bit to "0" (transmit disabled). Also, the transmission circuit is not initialized by clearing the serial I/O<sub>i</sub> enable bit to "0" (serial I/O<sub>i</sub> disabled) (refer to (1) in 1.).

### 2. Notes when selecting clock asynchronous serial I/O

#### (1) Stop of transmission operation

Clear the transmit enable bit to "0" (transmit disabled). The transmission operation does not stop by clearing the serial I/O<sub>i</sub> enable bit (i = 1, 3) to "0".

<Reason>

This is the same as (1) in 1.

#### (2) Stop of receive operation

Clear the receive enable bit to "0" (receive disabled).

#### (3) Stop of transmit/receive operation

Only transmission operation is stopped.

Clear the transmit enable bit to "0" (transmit disabled). The transmission operation does not stop by clearing the serial I/O<sub>i</sub> enable bit (i = 1, 3) to "0".

<Reason>

This is the same as (1) in 1.

Only receive operation is stopped.

Clear the receive enable bit to "0" (receive disabled).

### 3. $\overline{\text{SRDY}}_i$ (i = 1, 3) output of reception side

When signals are output from the  $\overline{\text{SRDY}}_i$  pin on the reception side by using an external clock in the clock synchronous serial I/O mode, set all of the receive enable bit, the  $\overline{\text{SRDY}}_i$  output enable bit, and the transmit enable bit to "1" (transmit enabled).

### 4. Setting serial I/O<sub>i</sub> (i = 1, 3) control register again

Set the serial I/O<sub>i</sub> control register again after the transmission and the reception circuits are reset by clearing both the transmit enable bit and the receive enable bit to "0".

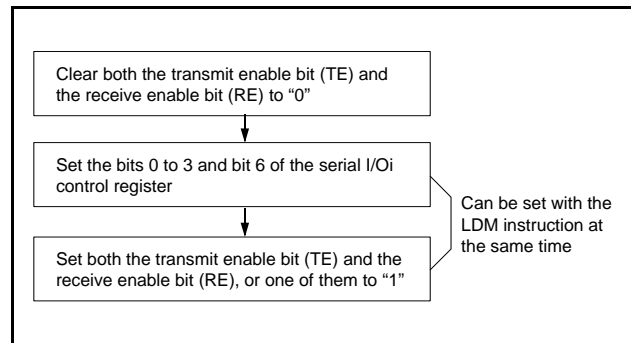


Fig 6. Sequence of setting serial I/O<sub>i</sub> (i = 1, 3) control register again

### 5. Data transmission control with referring to transmit shift register completion flag

After the transmit data is written to the transmit buffer register, the transmit shift register completion flag changes from "1" to "0" with a delay of 0.5 to 1.5 shift clocks. When data transmission is controlled with referring to the flag after writing the data to the transmit buffer register, note the delay.

### 6. Transmission control when external clock is selected

When an external clock is used as the synchronous clock for data transmission, set the transmit enable bit to "1" at "H" of the SCLKi (i = 1, 3) input level. Also, write the transmit data to the transmit buffer register at "H" of the SCLKi input level.

### 7. Transmit interrupt request when transmit enable bit is set

When using the transmit interrupt, take the following sequence.

- (1) Set the serial I/O<sub>i</sub> transmit interrupt enable bit (i = 1, 3) to "0" (disabled).
- (2) Set the transmit enable bit to "1".
- (3) Set the serial I/O<sub>i</sub> transmit interrupt request bit (i = 1, 3) to "0" after 1 or more instruction has executed.
- (4) Set the serial I/O<sub>i</sub> transmit interrupt enable bit (i = 1, 3) to "1" (enabled).

<Reason>

When the transmission enable bit is set to "1", the transmit buffer empty flag and transmit shift register shift completion flag are also set to "1".

Therefore, regardless of selecting which timing for the generating of transmit interrupts, the interrupt request is generated and the transmit interrupt request bit is set at this point.

### 8. Writing to baud rate generator i (BRGi) (i = 1, 3)

Write data to the baud rate generator i (BRGi) (i = 1, 3) while the transmission/reception operation is stopped.



**Notes on PWM**

The PWM starts from “H” level after the PWM enable bit is set to enable and “L” level is temporarily output from the PWM pin. The length of this “L” level output is as follows:

$$\frac{n+1}{2 \cdot f(XIN)} \quad (s) \quad \text{(Count source selection bit = “0”, where n is the value set in the prescaler)}$$

$$\frac{n+1}{f(XIN)} \quad (s) \quad \text{(Count source selection bit = “1”, where n is the value set in the prescaler)}$$

**Notes on A/D Converter****1. Analog input pin**

Make the signal source impedance for analog input low, or equip an analog input pin with an external capacitor of 0.01  $\mu\text{F}$  to 1  $\mu\text{F}$ . Further, be sure to verify the operation of application products on the user side.

<Reason>

An analog input pin includes the capacitor for analog voltage comparison. Accordingly, when signals from signal source with high impedance are input to an analog input pin, charge and discharge noise generates. This may cause the A/D conversion precision to be worse.

**2. A/D converter power source pin**

The AVSS pin is A/D converter power source pins. Regardless of using the A/D conversion function or not, connect it as following :

- AVSS : Connect to the VSS line

<Reason>

If the AVSS pin is opened, the microcomputer may have a failure because of noise or others.

**3. Clock frequency during A/D conversion**

The comparator consists of a capacity coupling, and a charge of the capacity will be lost if the clock frequency is too low. Thus, make sure the following during an A/D conversion.

- $f(XIN)$  is 500 kHz or more
- Do not execute the STP instruction

**4. Difference between at 8-bit reading in 10-bit A/D mode and at 8-bit A/D mode**

At 8-bit reading in the 10-bit A/D mode, “-1/2 LSB” correction is not performed to the A/D conversion result.

In the 8-bit A/D mode, the A/D conversion characteristics is the same as 3802 group’s characteristics because “-1/2 LSB” correction is performed.

**Notes on D/A Converter****1. Vcc when using D/A converter**

The D/A converter accuracy when VCC is 4.0 V or less differs from that of when VCC is 4.0 V or more. When using the D/A converter, we recommend using a VCC of 4.0 V or more.

**2. D/Ai conversion register when not using D/A converter**

When a D/A converter is not used, set all values of the D/Ai conversion registers (i = 1, 2) to “0016”. The initial value after reset is “0016”.

**Notes on Watchdog Timer**

- Make sure that the watchdog timer H does not underflow while waiting Stop release, because the watchdog timer keeps counting during that term.
- When the STP instruction disable bit has been set to “1”, it is impossible to switch it to “0” by a program.

**Notes on RESET Pin****Connecting capacitor**

In case where the RESET signal rise time is long, connect a ceramic capacitor or others across the RESET pin and the VSS pin.

Use a 1000 pF or more capacitor for high frequency use. When connecting the capacitor, note the following :

- Make the length of the wiring which is connected to a capacitor as short as possible.
- Be sure to verify the operation of application products on the user side.

<Reason>

If the several nanosecond or several ten nanosecond impulse noise enters the RESET pin, it may cause a microcomputer failure.

**Notes on Low-speed Operation Mode****1. Using sub-clock**

To use a sub-clock, fix bit 3 of the CPU mode register to “1” or control the Rd (refer to Figure 7) resistance value to a certain level to stabilize an oscillation. For resistance value of Rd, consult the oscillator manufacturer.

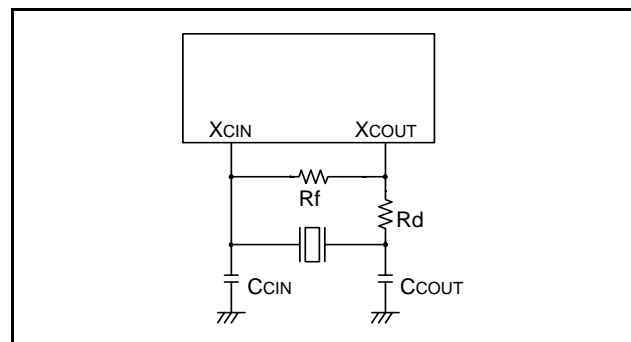


Fig 7. Ceramic resonator circuit

<Reason>

When bit 3 of the CPU mode register is set to “0”, the sub-clock oscillation may stop.

**2. Switch between middle/high-speed mode and low-speed mode**

If you switch the mode between middle/high-speed and low-speed, stabilize both XIN and XCIN oscillations. The sufficient time is required for the sub clock to stabilize, especially immediately after power on and at returning from stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency on condition that  $f(XIN) > 3 \cdot f(XCIN)$ .

**Quartz-Crystal Oscillator**

When using the quartz-crystal oscillator of high frequency, such as 16 MHz etc., it may be necessary to select a specific oscillator with the specification demanded.

**Notes on Restarting Oscillation**

## • Restarting oscillation

Usually, when the MCU stops the clock oscillation by STP instruction and the STP instruction has been released by an external interrupt source, the fixed values of Timer 1 and Prescaler 12 (Timer 1 = "0116", Prescaler 12 = "FF16") are automatically reloaded in order for the oscillation to stabilize. The user can inhibit the automatic setting by writing "1" to bit 0 of MISRG (address 001016).

However, by setting this bit to "1", the previous values, set just before the STP instruction was executed, will remain in Timer 1 and Prescaler 12. Therefore, you will need to set an appropriate value to each register, in accordance with the oscillation stabilizing time, before executing the STP instruction.

<Reason>

Oscillation will restart when an external interrupt is received. However, internal clock  $\phi$  is supplied to the CPU only when Timer 1 starts to underflow. This ensures time for the clock oscillation using the ceramic resonators to be stabilized.

**Notes on Using Stop Mode**

## • Register setting

Since values of the prescaler 12 and Timer 1 are automatically reloaded when returning from the stop mode, set them again, respectively. (When the oscillation stabilizing time set after STP instruction released bit is "0")

## • Clock restoration

After restoration from the stop mode to the normal mode by an interrupt request, the contents of the CPU mode register previous to the STP instruction execution are retained. Accordingly, if both main clock and sub clock were oscillating before execution of the STP instruction, the oscillation of both clocks is resumed at restoration.

In the above case, when the main clock side is set as a system clock, the oscillation stabilizing time for approximately 8,000 cycles of the XIN input is reserved at restoration from the stop mode. At this time, note that the oscillation on the sub clock side may not be stabilized even after the lapse of the oscillation stabilizing time of the main clock side.

**Notes on Wait Mode**

## • Clock restoration

If the wait mode is released by a reset when XCIN is set as the system clock and XIN oscillation is stopped during execution of the WIT instruction, XCIN oscillation stops, XIN oscillations starts, and XIN is set as the system clock.

In the above case, the RESET pin should be held at "L" until the oscillation is stabilized.

**Notes on Handling of Power Source Pins**

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (VCC pin) and GND pin (VSS pin), and between power source pin (VCC pin) and analog power source input pin (AVSS pin). Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of 0.01  $\mu$ F–0.1  $\mu$ F is recommended.

**Power Source Voltage**

When the power source voltage value of a microcomputer is less than the value which is indicated as the recommended operating conditions, the microcomputer does not operate normally and may perform unstable operation.

In a system where the power source voltage drops slowly when the power source voltage drops or the power supply is turned off, reset a microcomputer when the power source voltage is less than the recommended operating conditions and design a system not to cause errors to the system by this unstable operation.

**Electric Characteristic Differences Between Flash Memory, Mask ROM and QzROM Version MCUs**

There are differences in the manufacturing processes and the mask pattern among flash memory, mask ROM, and QzROM version MCUs due to the differences of the ROM type. Even when the ROM type is the same, when the memory size is different, the manufacturing processes and the mask pattern differ. For these reasons, the oscillation circuit constants and the characteristics such as a characteristic value, operation margin, noise immunity, and noise radiation within the limits of electrical characteristics may differ.

When manufacturing an application system, please perform sufficient evaluations in each product. Especially, when switching a product (example: change from the mask ROM version to QzROM version), please perform sufficient evaluations by the switching product in the stage before mass-producing an application system.

**Product Shipped in Blank**

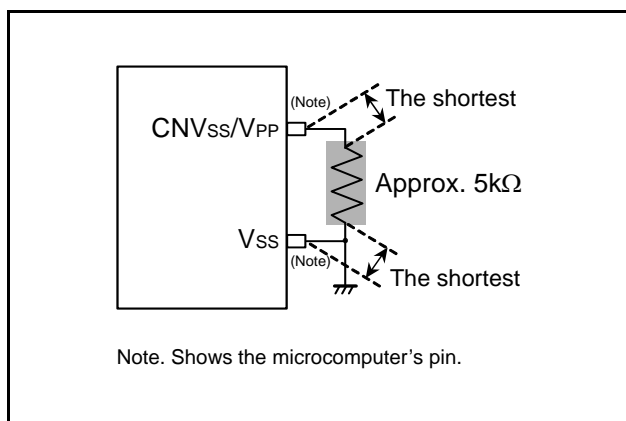
As for the product shipped in blank, Renesas does not perform the writing test to user ROM area after the assembly process though the QzROM writing test is performed enough before the assembly process. Therefore, a writing error of approx.0.1 % may occur. Moreover, please note the contact of cables and foreign bodies on a socket, etc. because a writing environment may cause some writing errors.

**QzROM Version**

Connect the CNVSS/VPP pin the shortest possible to the GND pattern which is supplied to the VSS pin of the microcomputer. In addition connecting an approximately 5 kΩ resistor in series to the GND could improve noise immunity. In this case as well as the above mention, connect the pin the shortest possible to the GND pattern which is supplied to the VSS pin of the microcomputer.

• Reason

The CNVSS/VPP pin is the power source input pin for the built-in QzROM. When programming in the QzROM, the impedance of the VPP pin is low to allow the electric current for writing to flow into the built-in QzROM. Because of this, noise can enter easily. If noise enters the VPP pin, abnormal instruction codes or data are read from the QzROM, which may cause a program runaway.



**Fig 8. Wiring for the CNVSS/VPP**

**Notes On QzROM Writing Orders**

When ordering the QzROM product shipped after writing, submit the mask file (extension: .mask) which is made by the mask file converter MM.

Be sure to set the ROM option (“MASK option” written in the mask file converter) setup when making the mask file by using the mask file converter MM.

**Notes On ROM Code Protect (QzROM product shipped after writing)**

As for the QzROM product shipped after writing, the ROM code protect is specified according to the mask option setup data in the mask file which is submitted at ordering.

Renesas Technology corp. uses the mask option setup data at the ROM code protect address (address FFDB16) when writing to the QzROM. Consequently, the actual written value might differ from the ordered value as the contents of the ROM code protect address.

The ROM option setup data in the mask file is “0016” for protect enabled, “FE16” (protect enabled to the protect area 1 only) or “FF16” for protect disabled. Therefore, the contents of the ROM code protect address of the QzROM product shipped after writing are “0016”, “FE16” or “FF16”.

Note that the mask file which has nothing at the ROM option data or has the data other than “0016”, “FE16” and “FF16” can not be accepted.

**DATA REQUIRED FOR QzROM WRITING ORDERS**

The following are necessary when ordering a QzROM product shipped after writing:

1. QzROM Writing Confirmation Form\*
2. Mark Specification Form\*
3. ROM data.....Mask file

\* For the QzROM writing confirmation form and the mark specification form, refer to the “Renesas Technology Corp.” Homepage (<http://www.renesas.com/homepage.jsp>).

Note that we cannot deal with special font marking (customer's trademark etc.) in QzROM microcomputer.

## REVISION HISTORY

## 3803 Group (Spec.H QzROM version) Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Sep. 30, 2005	–	First edition issued
1.10	Nov. 14, 2005	20	Fig 14. Port block diagram (3) (18) Port P56 revised
		61	Fig 54. Block diagram of Watchdog timer; STP instruction disable bit → STP instruction function selection bit revised
		69	QzROM version; approximately 1 k to 5 kΩ resistor → approximately 5 kΩ resistor Fig 47. Wiring for the CNVSS/VPP added Notes On QzROM Writing Orders; (extension: .mask) → (extension: .msk) revised
		82-83	Package Outline revised
		84-91	Appendix added