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HD74CDC2510B

3.3-V Phase-lock Loop Clock Driver

Description

The HD74CDC2510B is a high-performance, low-skew, low-jitter, phase-lock loop clock driver. It uses a phase-lock loop (PLL) to precisely align, in both frequency and phase, the feedback (FBOUT) output to the clock (CLK) input signal. It is specifically designed for use with synchronous DRAMs. The HD74CDC2510B operates at 3.3 V V_{CC} and is designed to drive up to five clock loads per output.

Bank of outputs provide ten low-skew, low-jitter copies of the input clock. Output signal duty cycles are adjusted to 50 percent independent of the duty cycle at the input clock. Bank of outputs can be enabled or disabled via the control (G) inputs. When the G inputs are high, the outputs switch in phase and frequency with CLK; when the G inputs are low, the outputs are disabled to the logic-low state.

Unlike many products containing PLLs, the HD74CDC2510B does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, HD74CDC2510B requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required, following power up and application of a fixed-frequency, fixed-phase signal at CLK, as well as following any changes to the PLL reference or feedback signals. The PLL can be bypassed for test purposes by strapping AV_{CC} to ground.

Features

- Meets "PC SDRAM registered DIMM design support document, Rev. 1.2"
- Phase-lock loop clock distribution for synchronous DRAM applications
- External feedback (FBIN) pin is used to synchronize the outputs to the clock input
- No external RC network required
- Support spread spectrum clock (SSC) synthesizers
- Ordering Information

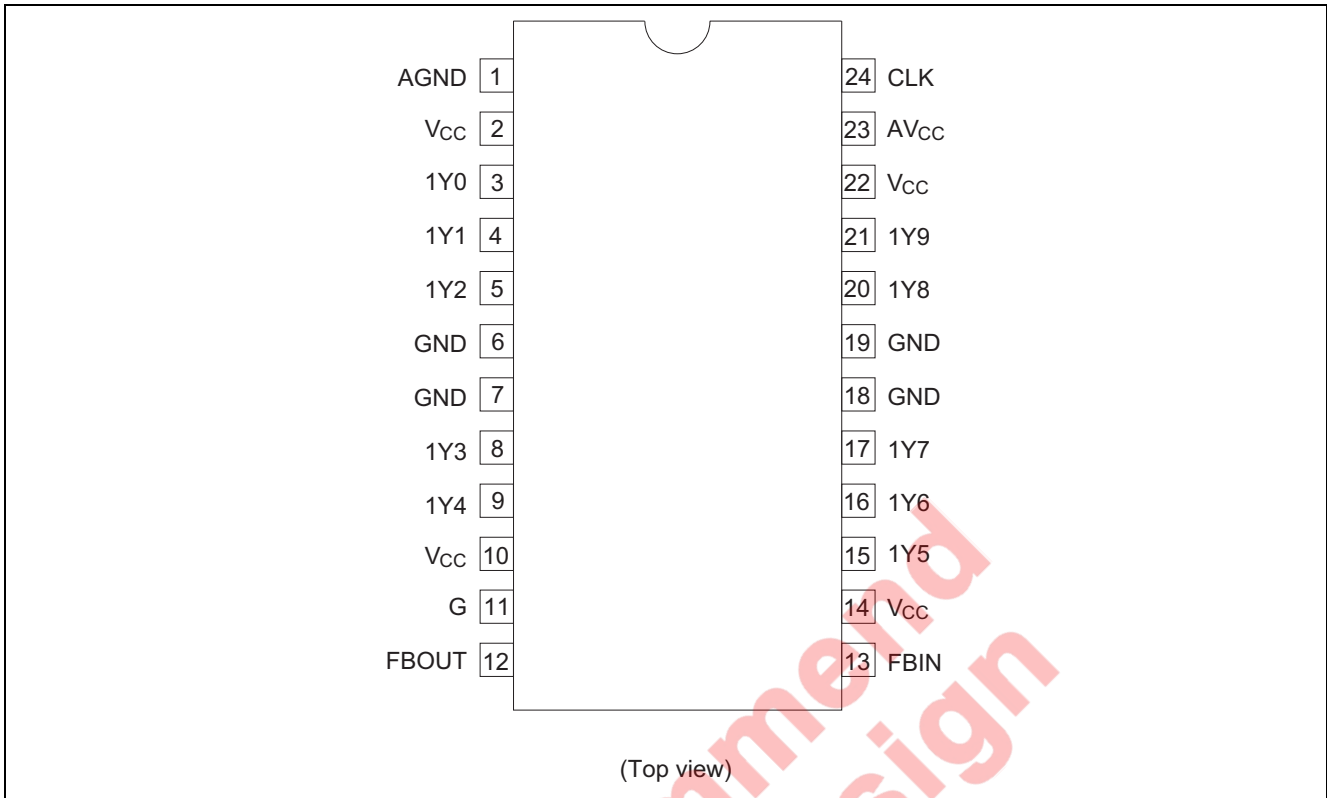| Part Name	Package Type	Package Code (Previous code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74CDC2510BTEL	TSSOP-24 pin	PTSP0024JB-A (TTP-24DBV)	T	EL (1,000 pcs / Reel)

*Only by a change of a suffix (A to B) for standardization, there isn't any change of the product.

Function Table

Inputs		Outputs	
G	CLK	1Y (0:9)	FBOUT
X	L	L	L
L	H	L	H
H	H	H	H

H :   High level

L :   Low level

X :   Immaterial

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Pin Arrangement

AGND	1		24	CLK
V_{CC}	2		23	AV_{CC}
1Y0	3		22	V_{CC}
1Y1	4		21	1Y9
1Y2	5		20	1Y8
GND	6		19	GND
GND	7		18	GND
1Y3	8		17	1Y7
1Y4	9		16	1Y6
V_{CC}	10		15	1Y5
G	11		14	V_{CC}
FBOUT	12		13	FBIN

(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	–0.5 to 4.6	V	
Input voltage [*1]	V_I	–0.5 to 6.5	V	
Output voltage [*1, 2]	V_O	–0.5 to V_{CC} +0.5	V	
Input clamp current	I_{IK}	–50	mA	$V_I < 0$
Output clamp current	I_{OK}	±50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	±50	mA	$V_O = 0$ to V_{CC}
Supply current	I_{CC} or I_{GND}	±100	mA	
Maximum power dissipation at Ta = 55°C (in still air) [*3]	P_T	0.7	W	
Storage temperature	T_{stg}	–65 to +150	°C	

Notes: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
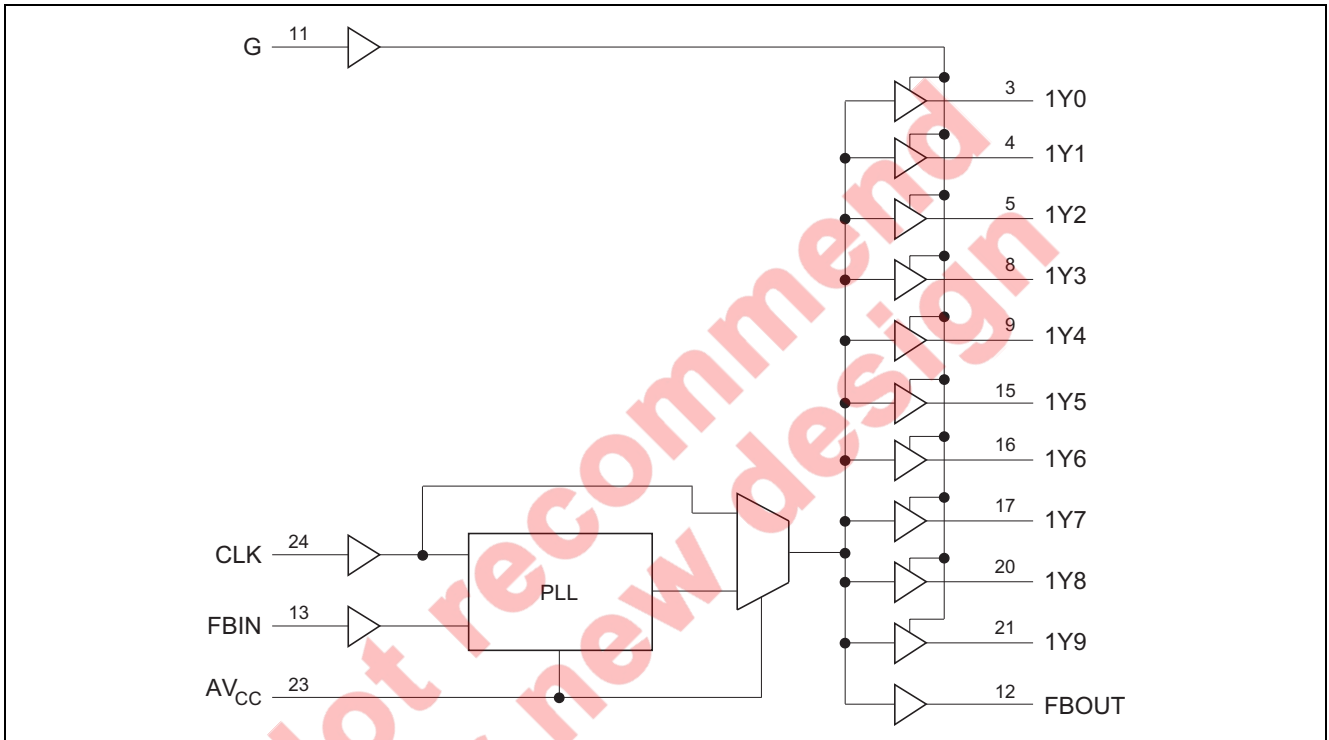
1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

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Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage	V_{CC}	3.0	—	3.6	V	
Input voltage	V_{IH}	2.0	—	—	V	
	V_{IL}	—	—	0.8		
	V_I	0	—	V_{CC}		
Output current	I_{OH}	—	—	−12	mA	
	I_{OL}	—	—	12		
Operating temperature	T_a	0	—	85	°C	

Note: Unused inputs must be held high or low to prevent them from floating.

Logic Diagram

Pin Function

Pin name	No.	Type	Description
CLK	24	I	Clock input. CLK provides the clock signal to be distributed by the HD74CDC2510B clock driver. CLK is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
FBIN	13	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard-wired to FBOUT to complete the PLL. The integrated PLL synchronizes CLK and FBIN so that there is nominally zero phase error between CLK and FBIN.
G	11	I	Output bank enable. G is the output enable for outputs 1Y(0:9). When G is low, outputs 1Y(0:9)are disabled to a logic-low state. When G is high, all outputs 1Y(0:9) are enabled and switch at the same frequency as CLK.
FBOUT	12	O	Feedback output. FBOUT is dedicated for external feedback. It switches at the same frequency as CLK. When externally wired to FBIN, FBOUT completes the feedback loop of the PLL.
1Y(0:9)	3, 4, 5, 8, 9, 15, 16, 17, 20, 21	O	Clock outputs. These outputs provide low-skew copies of CLK. Output bank 1Y(0:9) is enabled via the G input. These outputs can be disabled to a logic low state by deasserting the G control input.
AV_{CC}	23	Power	Analog power supply. AV_{CC} provides the power reference for the analog circuitry. In addition, AV_{CC} can be used to bypass the PLL for test purposes. When AV_{CC} is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs.
AGND	1	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
V_{CC}	2, 10, 14, 22	Power	Power supply
GND	6, 7, 18,19	Ground	Ground

Electrical Characteristics

Item	Symbol	Min	Typ [1]	Max	Unit	Test Conditions
Input clamp voltage	V_{IK}	—	—	–1.2	V	V_{CC} = 3 V, I_I = –18 mA
Output voltage	V_{OH}	V_{CC}–0.2	—	—	V	V_{CC} = Min to Max, I_{OH} = –100 μA
		2.1	—	—		V_{CC} = 3 V, I_{OH} = –12 mA
		2.4	—	—		V_{CC} = 3 V, I_{OH} = –6 mA
	V_{OL}	—	—	0.2		V_{CC} = Min to Max, I_{OL} = 100 μA
		—	—	0.8		V_{CC} = 3 V, I_{OL} = 12 mA
		—	—	0.55		V_{CC} = 3 V, I_{OL} = 6 mA
Input current	I_{IN}	—	—	±5	μA	V_{CC} = 3.6 V, V_{IN} = V_{CC} or GND
Quiescent supply current	I_{CC}	—	—	10	μA	AV_{CC} = GND, V_{CC} = 3.6 V, V_I = V_{CC} or GND, I_O = 0
	ΔI_{CC}	—	—	500	μA	AV_{CC} = GND, V_{CC} = 3.3 to 3.6 V One input at V_{CC}–0.6 V, Other inputs at V_{CC} or GND
Input capacitance	C_{IN}	—	4	—	pF	V_{CC} = 3.3 V, V_I = V_{CC} or GND
Output capacitance	C_O	—	6	—	pF	V_{CC} = 3.3 V, V_O = V_{CC} or GND

Note: 1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

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Switching Characteristics

$(C_L = 30 \text{ pF}, Ta = 0 \text{ to } 85°C)$

Item	Symbol	V_{CC} = 3.3 V±0.3 V			Unit	From (Input)	To (Output)
		Min	Typ	Max			
Phase error time	t_{pe}	–150	—	150	ps	66 MHz < CLKIN↑ ≤ 100 MHz	FBIN↑
Between output pins skew *1	$t_{sk(O)}$	—	—	200	ps	Any Y or FBOUT, F (clkin = 100 MHz)	Any Y or FBOUT
Cycle to cycle jitter		–100	—	100	ps	F (clkin = 100 MHz)	Any Y or FBOUT
Duty cycle		45	—	55	%	F (clkin = 100 MHz)	Any Y or FBOUT
Output rise / fall time	t_{TLH}	5.0	—	1.0	volts/ns		Any Y or FBOUT
	t_{THL}	5.0	—	1.0			Any Y or FBOUT
Analog power supply rejection (DC to 10 MHz)	Vapsr *2	100	—	—	$mV_{P–P}$		AV_{CC}

Notes: The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.

1. The $t_{sk(O)}$ specification is only valid for equal loading of all outputs.
2. This parameter is characterized but not tested.

Timing Requirements

Item	Symbol	Min	Max	Unit	Test Conditions
Input clock frequency	f_{clock}	50	125	MHz	
Input clock duty cycle		40	60	%	
Stabilization time *1		—	1	ms	After power up

Note: 1. Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. In order for phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics table are not applicable.

Test Circuit
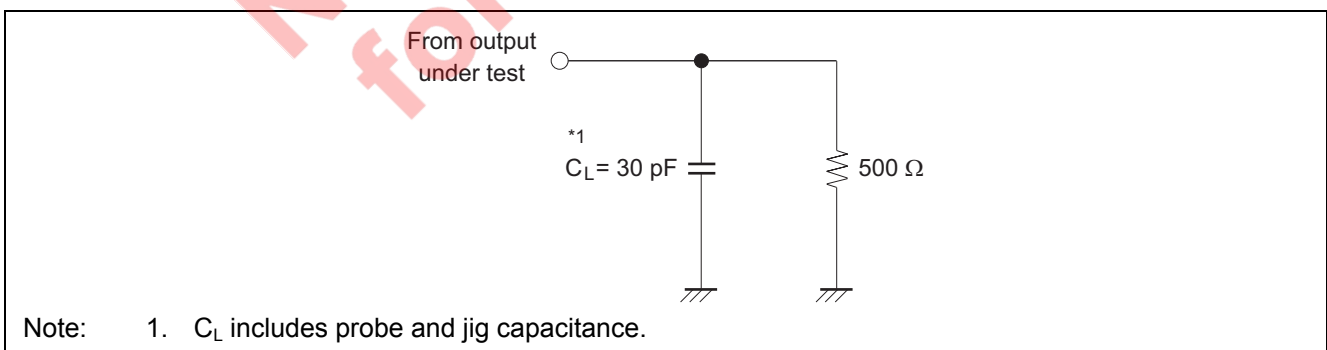
Note: 1. C_L includes probe and jig capacitance.

Waveforms – 1

Input — 50% V_CC — 50% V_CC — 3 V — 0 V

Output (= FBOUT) — 50% V_CC — 0.4 V — 2 V — 2 V — 0.4 V — V_OH — V_OL — t_TLH — t_THL

Notes: 1. All input pulses are supplied by generators having the following characteristics: PRR ≤ 100 MHz, Z_O = 50 Ω, t_r = 1.2 ns, t_f = 1.2 ns.
2. The outputs are measured one at a time with one transition per measurement.

Waveforms – 2

CLKIN — $t_{phase\ error}$

FBIN

FBOUT — $t_{sk\ (o)}$

Any Y

Any Y — $t_{sk\ (o)}$

Any Y
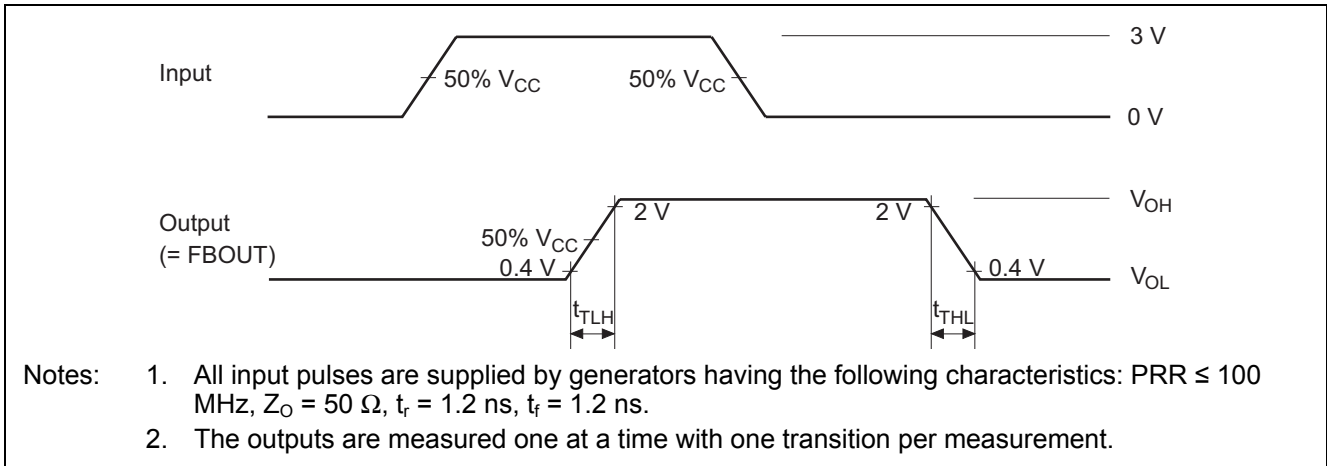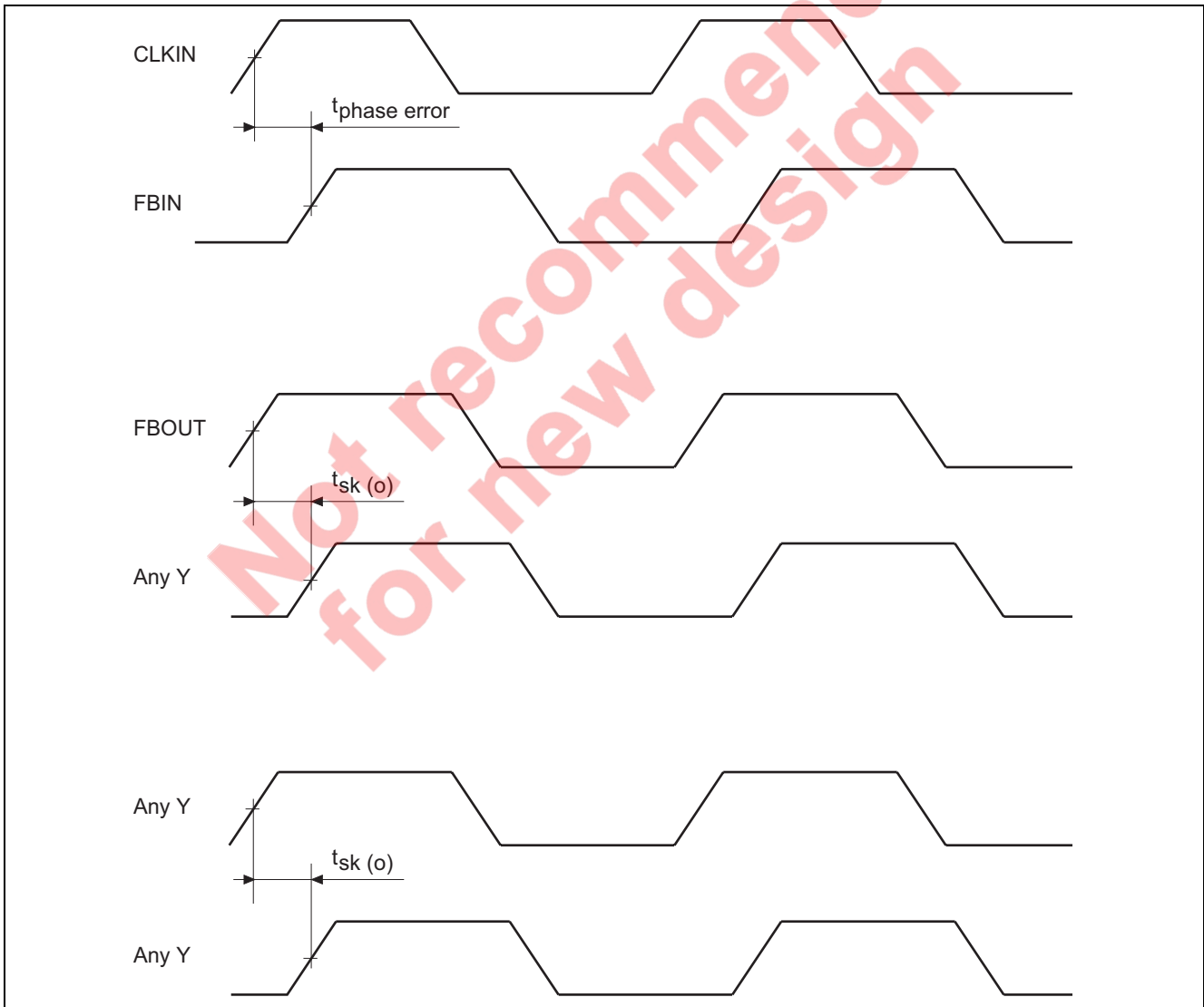
Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TSSOP24-4.4x7.8-0.65	PTSP0024JB-A	TTP-24DBV	0.08g
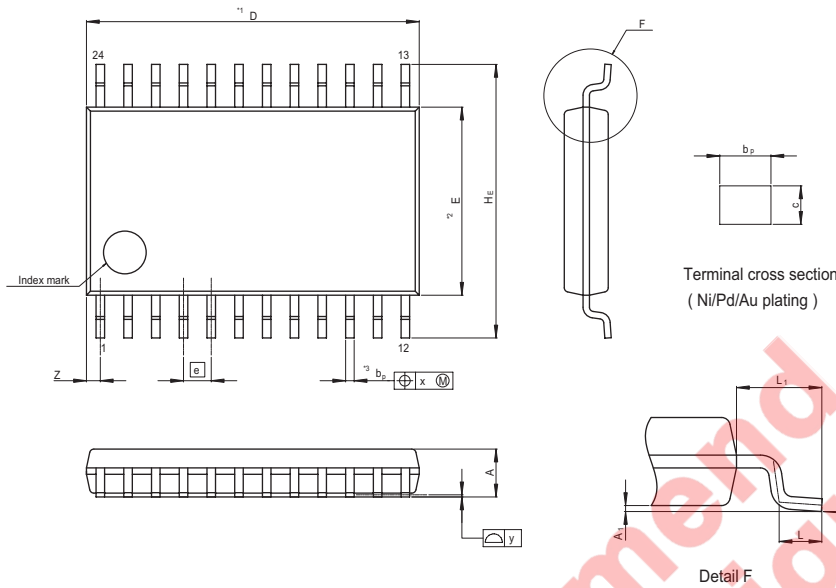
NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.

Index mark

Terminal cross section
(Ni/Pd/Au plating)

Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.80	8.10
E	—	4.40	—
A_2	—	—	—
A_1	0.03	0.07	0.10
A	—	—	1.10
b_p	0.15	0.20	0.25
b_1	—	—	—
c	0.10	0.15	0.20
c_1	—	—	—
θ	0°	—	8°
H_E	6.20	6.40	6.60
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z	—	—	0.65
L	0.4	0.5	0.6
L_1	—	1.0	—

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RenesasTechnology Corp. Sales Strategic Planning Div.   Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

RENESAS SALES OFFICES

http://www.renesas.com

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Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.
Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510