

# HAT1127H

## Silicon P Channel Power MOS FET Power Switching

REJ03G1330-0500

Rev.5.00

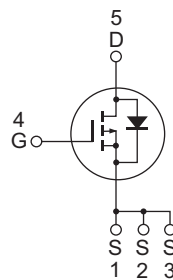
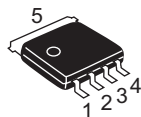
Jan 20, 2006

### Features

- Capable of -4.5 V gate drive
- Low drive current
- High density mounting
- Ultra Low on-resistance  
 $R_{DS(on)} = 3.6 \text{ m}\Omega$  typ. (at  $V_{GS} = -10 \text{ V}$ )

### Outline

RENESAS Package code: PTZZ0005DA-A  
(Package name: LFPAK)



1, 2, 3 Source  
4 Gate  
5 Drain

### Absolute Maximum Ratings

( $T_a = 25^\circ\text{C}$ )

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	-30	V
Gate to source voltage	$V_{GSS}$	-20/+10	V
Drain current	$I_D$	-40	A
Drain peak current	$I_{D(pulse)}$ <sup>Note1</sup>	-160	A
Body-drain diode reverse drain current	$I_{DR}$	-40	A
Channel dissipation	$P_{ch}$ <sup>Note2</sup>	30	W
Channel to Case Thermal Impedance	$\theta_{ch-c}$ <sup>Note2</sup>	4.17	$^\circ\text{C/W}$
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

Notes: 1.  $PW \leq 10 \mu\text{s}$ , duty cycle  $\leq 1\%$

2.  $T_c = 25^\circ\text{C}$

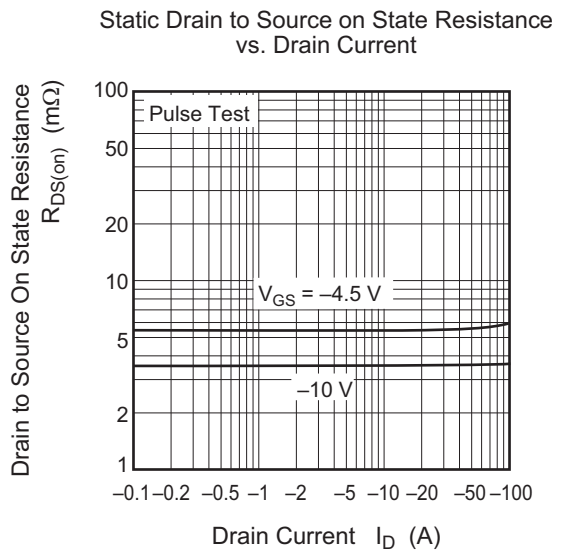
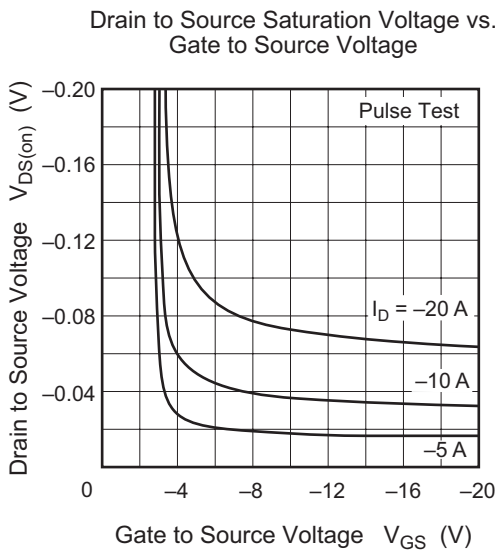
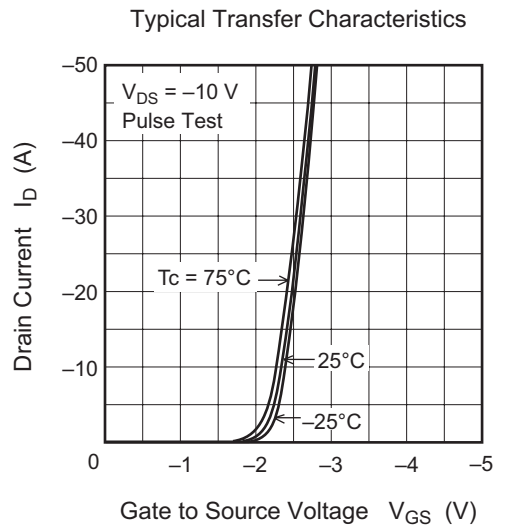
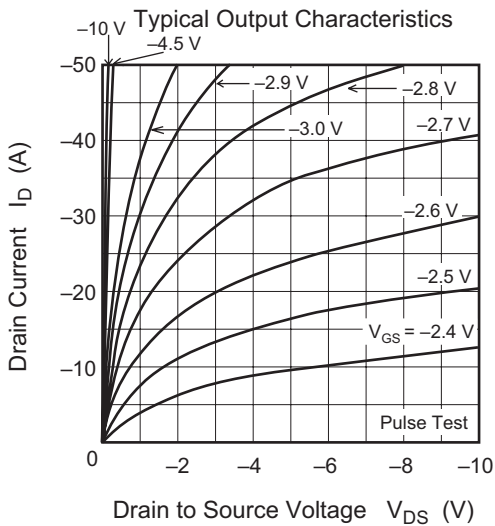
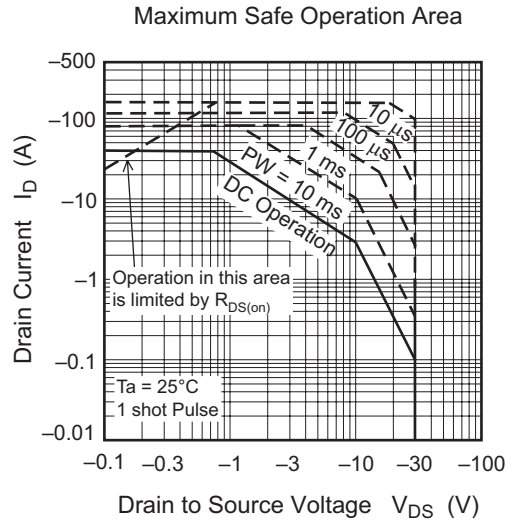
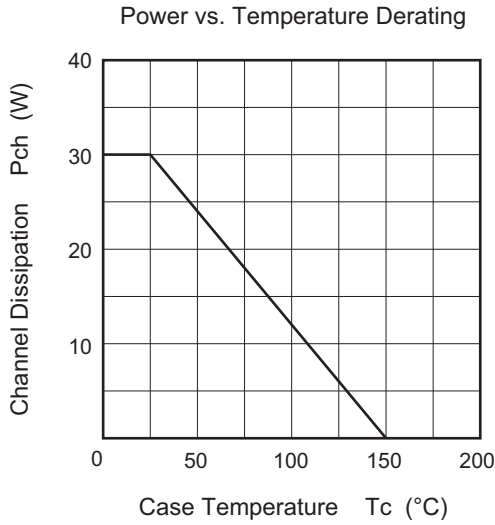
## Electrical Characteristics

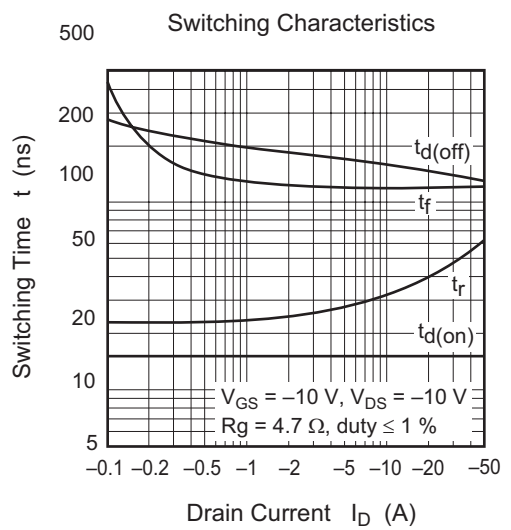
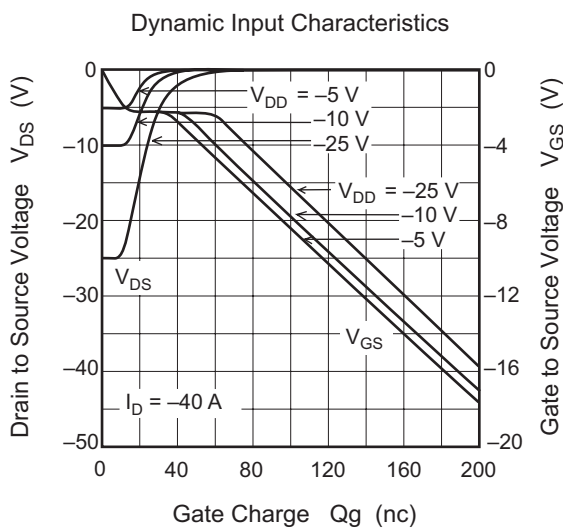
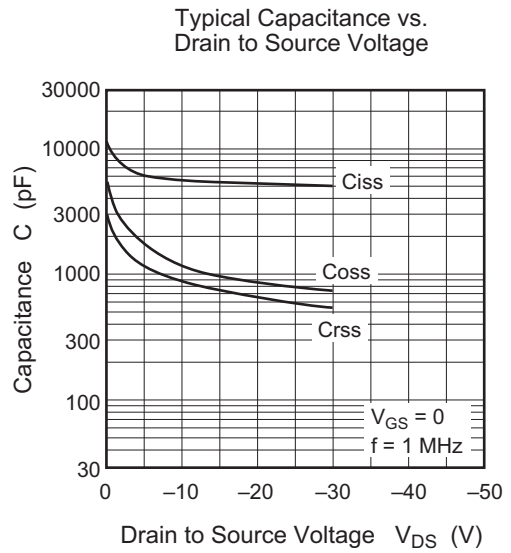
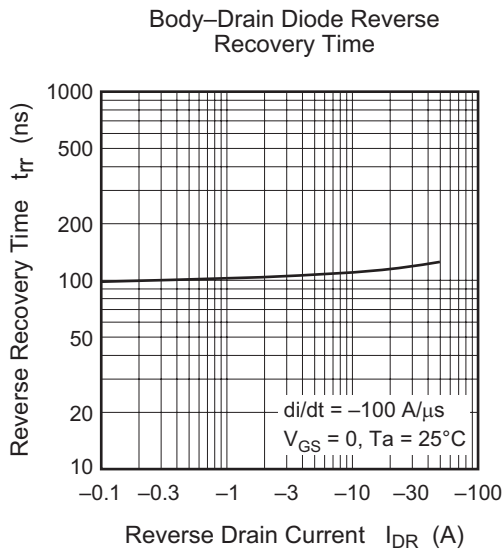
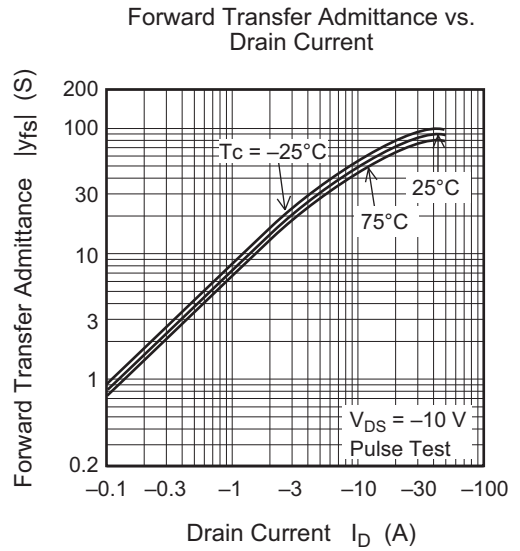
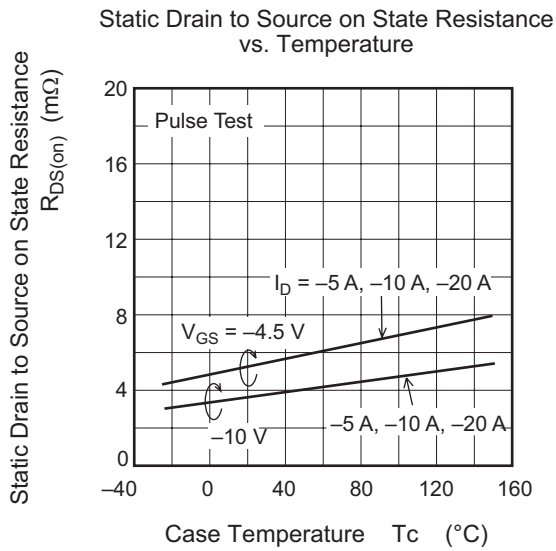
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-30	—	—	V	$I_D = -10 \text{ mA}$ , $V_{GS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 0.1$	$\mu\text{A}$	$V_{GS} = -20/+10 \text{ V}$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	-1	$\mu\text{A}$	$V_{DS} = -30 \text{ V}$ , $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.5	V	$V_{DS} = -10 \text{ V}$ , $I_D = -1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	3.6	4.5	$\text{m}\Omega$	$I_D = -20 \text{ A}$ , $V_{GS} = -10 \text{ V}$ <sup>Note3</sup>
	$R_{DS(on)}$	—	5.3	7.7	$\text{m}\Omega$	$I_D = -20 \text{ A}$ , $V_{GS} = -4.5 \text{ V}$ <sup>Note3</sup>
Forward transfer admittance	$ y_{fs} $	40	70	—	S	$I_D = -20 \text{ A}$ , $V_{DS} = -10 \text{ V}$ <sup>Note3</sup>
Input capacitance	$C_{iss}$	—	5600	—	pF	$V_{DS} = -10 \text{ V}$ , $V_{GS} = 0$ , $f = 1 \text{ MHz}$
Output capacitance	$C_{oss}$	—	1180	—	pF	
Reverse transfer capacitance	$C_{rss}$	—	890	—	pF	
Total gate charge	$Q_g$	—	125	—	nC	$V_{DD} = -10 \text{ V}$ , $V_{GS} = -10 \text{ V}$ , $I_D = -40 \text{ A}$
Gate to source charge	$Q_{gs}$	—	15	—	nC	
Gate to drain charge	$Q_{gd}$	—	28	—	nC	
Turn-on delay time	$t_{d(on)}$	—	25	—	ns	$V_{GS} = -10 \text{ V}$ , $I_D = -20 \text{ A}$ , $V_{DD} \cong -10 \text{ V}$ , $R_L = 0.5 \Omega$ , $R_g = 4.7 \Omega$
Rise time	$t_r$	—	40	—	ns	
Turn-off delay time	$t_{d(off)}$	—	130	—	ns	
Fall time	$t_f$	—	115	—	ns	
Body-drain diode forward voltage	$V_{DF}$	—	-0.88	-1.15	V	$I_F = -40 \text{ A}$ , $V_{GS} = 0$ <sup>Note3</sup>
Body-drain diode reverse recovery time	$t_{rr}$	—	120	—	ns	$I_F = -40 \text{ A}$ , $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

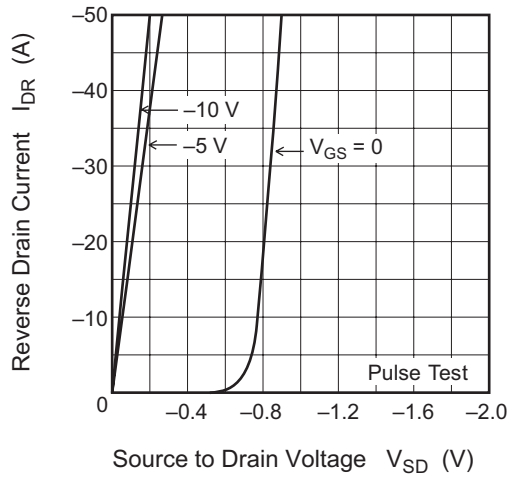
Notes: 3. Pulse test

Main Characteristics

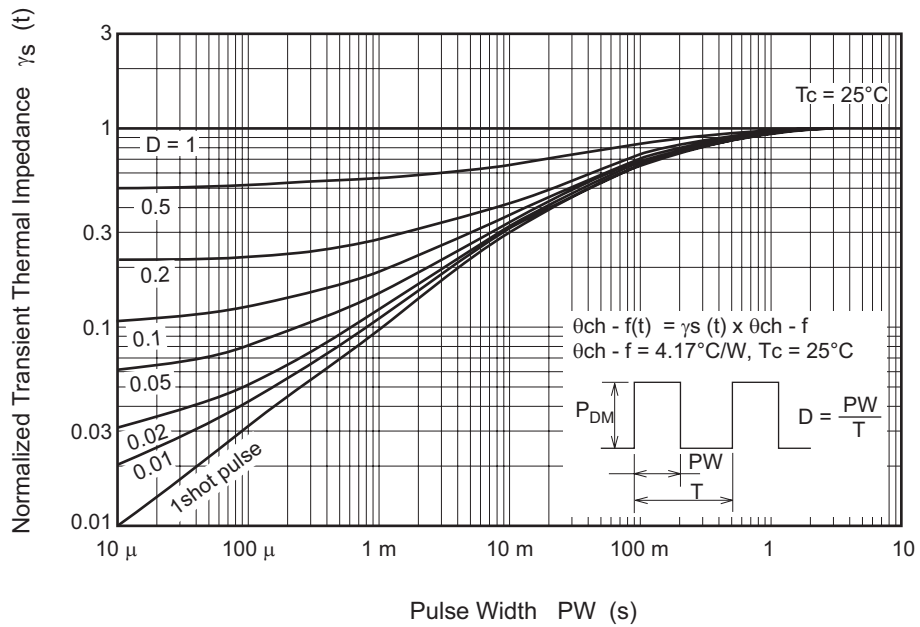




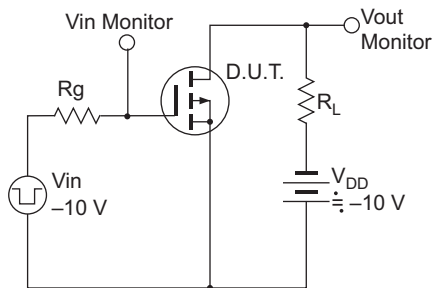
Reverse Drain Current vs. Source to Drain Voltage



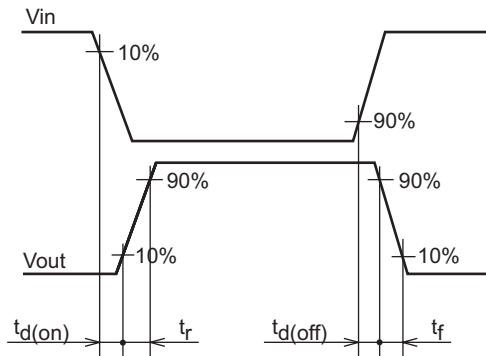
Normalized Transient Thermal Impedance vs. Pulse Width



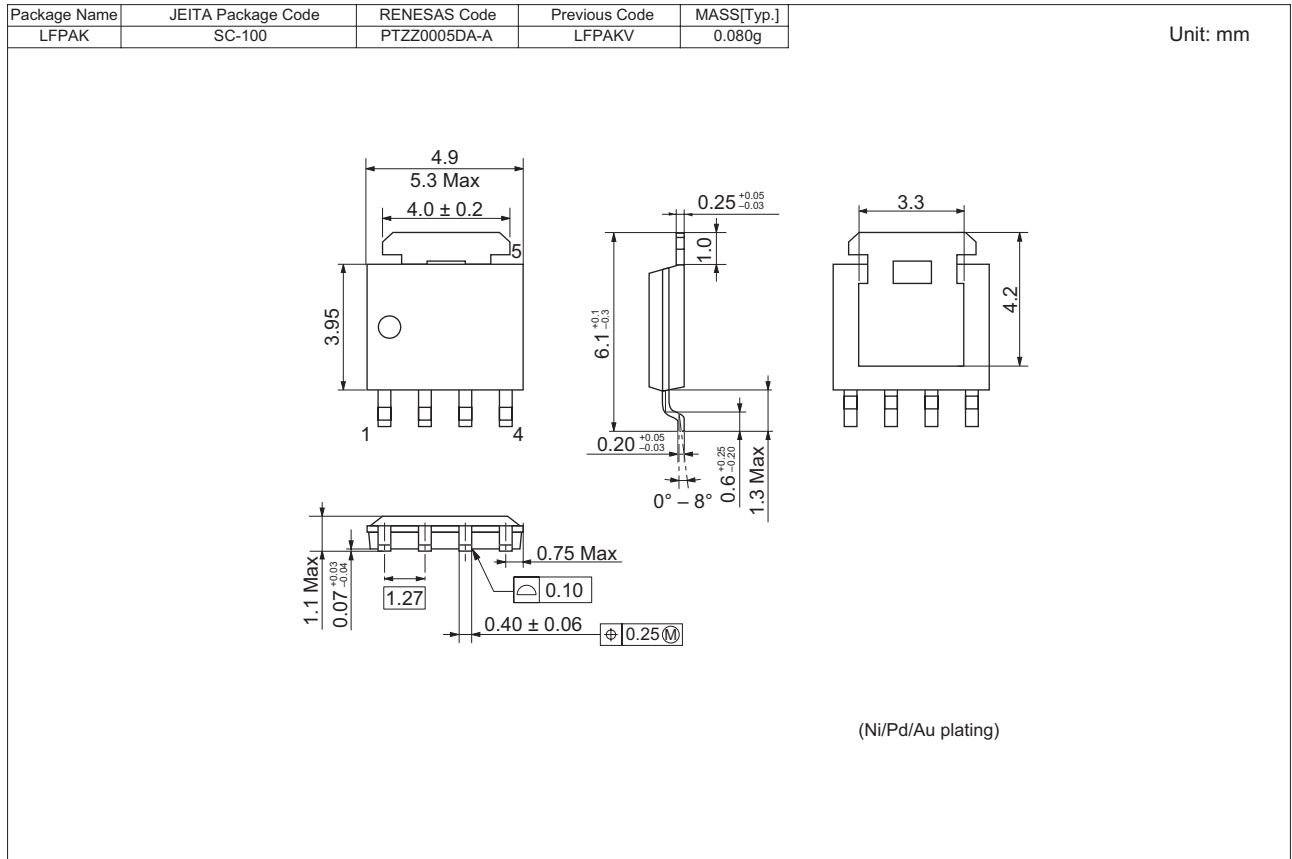
Switching Time Test Circuit



Waveform



Package Dimensions



Ordering Information

Part Name	Quantity	Shipping Container
HAT1127H-EL-E	2500 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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