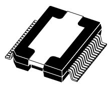
TDA7575B

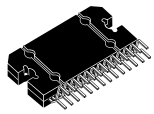
2 x 75W multifunction dual-bridge power amplifier with integrated digital diagnostics

Features

- Multipower bcd technology
- MOSFET output power stage
- DMOS power output
- New Hi-efficiency (class AB)
- Single-channel 1Ω driving capability
- High output power capability 2x28W/4Ω @ 14.4V, 1KHz, 10% THD
- Max. output power 2x75W/2Ω, 1x150W/1Ω
- Single-channel 1Ω driving capability
  - 84W undistorted power
  - Full I^2C bus driving with 4 address possibilities:
    - St-by
    - Play/mute
    - Gain 12/26dB
    - Full digital diagnostic (AC and DC loads)
- Possibility to disable the I^2C bus
- Differential inputs
- Full fault protection
- DC offset detection
- Two independent short circuit protections
- Diagnostic on clipping detector with selectable threshold (2%/10%)
- Clipping detector as diagnostic pin when I^2C bus is disabled
- St-by/mute pins
- ESD protection



PowerSO36 (Slug up)



Flexiwatt 27

Description

The TDA7575B is a new MOSFET dual bridge amplifier specially intended for car radio applications. Thanks to the DMOS output stage the TDA7575B has a very low distortion allowing a clear powerful sound.

Among the features, its superior efficiency performance coming from the internal exclusive structure, makes it the most suitable device to simplify the thermal management in high power sets.The dissipated output power under average listening condition is in fact reduced up to 50% when compared to the level provided by conventional class AB solutions.

This device is equipped with a full diagnostic array that communicates the status of each speaker through the I^2C bus. The TDA7575B has also the possibility of driving loads down to 1Ω paralleling the outputs into a single channel. It is also possible to disable the I^2C and control the TDA7575B by means of the usual ST-BY and MUTE pins.

Table 1. Device summary

Order code	Package	Packing
TDA7575B	Flexiwatt 27	Tube
TDA7575BPD	PowerSSO36 (slug up)	Tube
TDA7575BPDTR	PowerSSO36 (slug up)	Tape and reel

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1 Block and pins diagrams

Figure 1. Block diagram

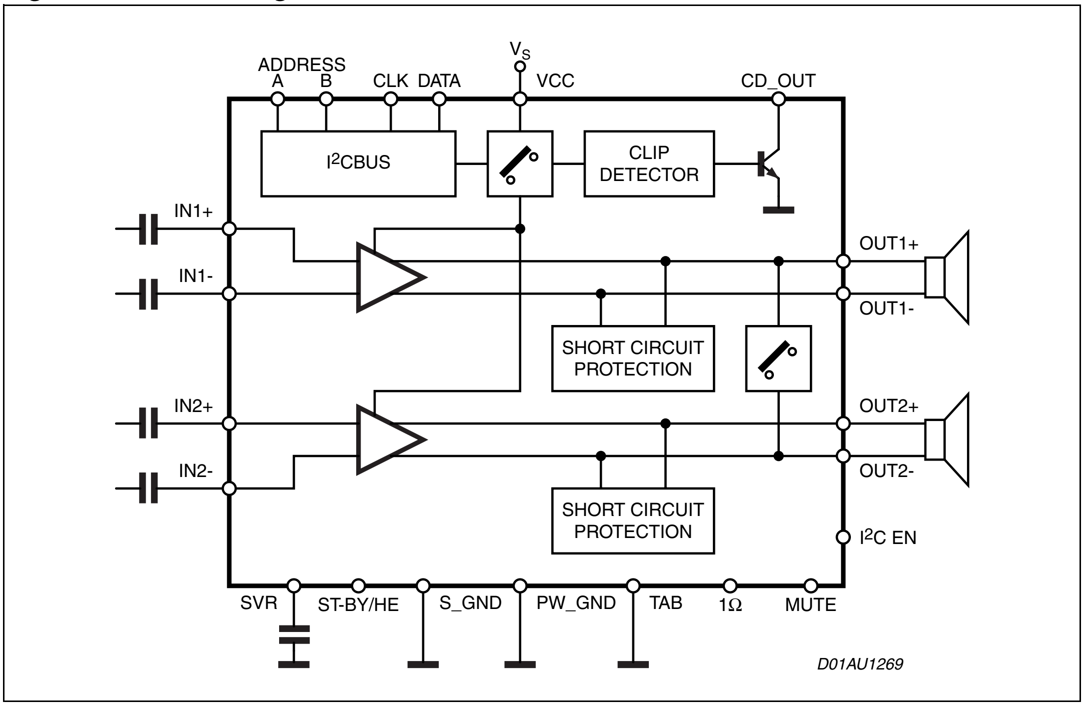
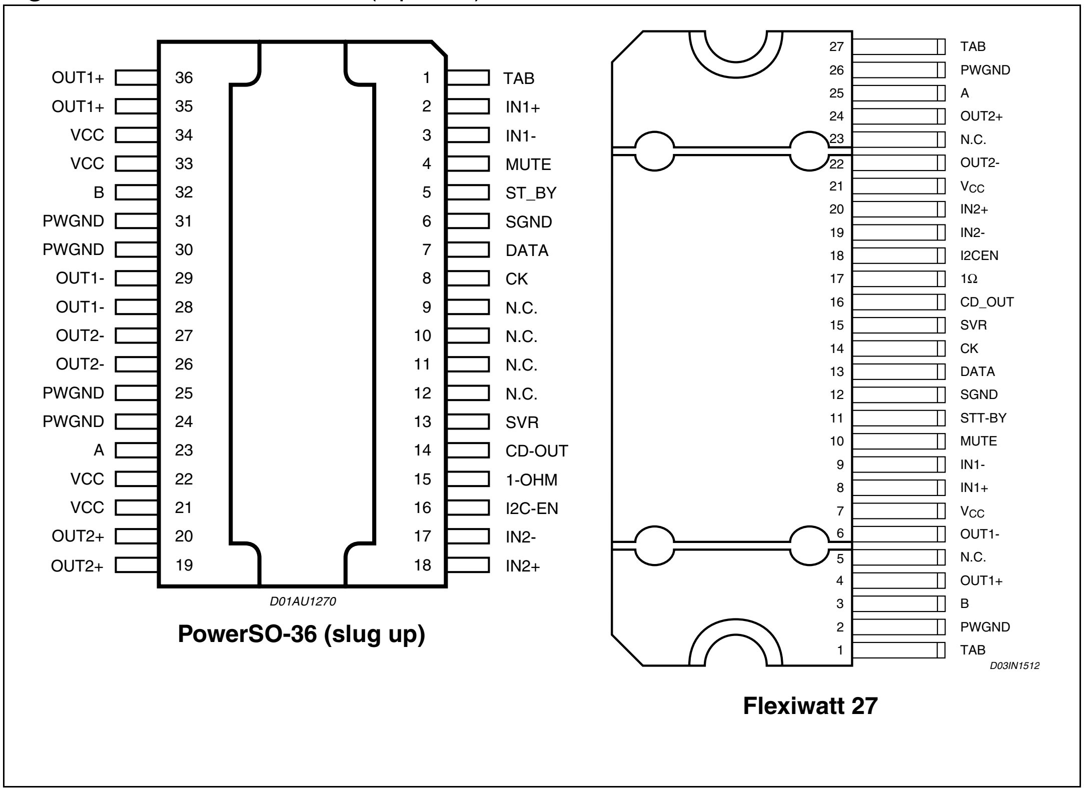


Figure 2. Pin connections (top view)



2 Electrical specifications

2.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{op}	Operating supply voltage	18	V
V_S	DC supply voltage	28	V
V_{peak}	Peak supply voltage (for t = 50ms)	50	V
V_{CK}	CK pin voltage	6	V
V_{DATA}	Data pin voltage	6	V
I_O	Output peak current (not repetitive t = 100ms)	8	A
I_O	Output peak current (repetitive f > 10Hz)	6	A
P_{tot}	Power dissipation T_{case} = 70°C	86	W
T_{stg}, T_j	Storage and junction temperature	-55 to 150	°C

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter		PowerSO36	Flexiwatt 27	Unit
$R_{th\ j\text{-}case}$	Thermal resistance junction to case	Max	1	1	°C/W

2.3 Electrical characteristics

Table 4. Electrical characteristics
(V_S = 14.4V; f=1KHz; R_L=4Ω; T_{amb}= 25°C unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Power amplifier						
V_S	Supply voltage range		8		18	V
I_d	Total quiescent drain current		50	130	200	mA
Po	Output power	Max. power(1)	35	40		W
		THD = 10% THD = 1%; BTL mode	25	28 22		W
		R_L = 2Ω; THD 10% R_L = 2Ω; THD 1% R_L = 2Ω; Max. power(1)	45 70	50 37 75		W

Table 4. Electrical characteristics (continued)
(V_S = 14.4V; f=1KHz; R_L=4Ω; T_{amb}= 25°C unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Po	Output power	Single channel configuration (1Ω pin >2.5V); R_L = 1Ω; THD 3% Max. power(1)	80 140	84 150		W
THD	Total harmonic distortion	P_O = 1-12W; STD MODE HE MODE; P_O = 1-2W HE MODE; P_O = 4-8W		0.03 0.03 0.5	0.1 0.1	%
		P_O = 1-12W, f = 10kHz		0.15	0.5	%
		R_L = 2; HE MODE; Po = 3W		0.03	0.5	%
		Single channel configuration (1Ω pin >2.5V); R_L = 1; P_O = 4-30W		0.02	0.1	%
C_T	Cross talk	R_g = 600Ω; P_O = 1W	60	75		dB
R_{IN}	Input impedance		60	100	130	KΩ
G_{V1}	Voltage gain 1 (default)		25	26	27	dB
ΔG_{V1}	Voltage gain match 1		-1	0	1	dB
G_{V2}	Voltage gain 2		11	12	13	dB
ΔG_{V2}	Voltage gain match 2		-1	0	1	dB
E_{IN1}	Output noise voltage gain 1	R_g = 600Ω; Gv = 26dB filter 20 to 22kHz		40	60	μV
E_{IN2}	Output noise voltage gain 2	R_g = 600Ω; Gv = 12dB filter 20 to 22kHz		15	25	μV
SVR	Supply voltage rejection	f = 100Hz to 10kHz; V_r = 1Vpk; R_g = 600Ω	50	60		dB
BW	Power bandwidth	(-3dB)	100			KHz
A_{SB}	Stand-by attenuation		90	100		dB
I_{SB}	Stand-by current consumption	$V_{st\text{-}by}$ = 0V		2	10	μA
A_M	Mute attenuation		80	90		dB
V_{OS}	Offset voltage	Mute & play	-45	0	45	mV
V_{AM}	Min. supply mute threshold		7	7.5	8	V
CMRR	Input CMRR	V_{CM} = 1Vpk-pk; Rg = 0 Ω	56	60		dB
V_{MC}	Maximum common mode input level	f = 1kHz			1	Vrms
SR	Slew rate		1.5	4		V/μs
ΔV_{OS}	During mute ON/OFF output offset voltage	ITU R-ARM weighted see *Figure 23*	-10		+10	mV
	During St-By ON/OFF output offset voltage		-10		+10	mV

Table 4. Electrical characteristics (continued)
(V_S = 14.4V; f=1KHz; R_L=4Ω; T_{amb}= 25°C unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
T_{ON}	Turn on delay	D2 (IB1) 0 to 1		15	40	ms
T_{OFF}	Turn off delay	D2 (IB1) 1 to 0		15	40	ms
V_{OFF}	St-by pin for st-by		0		1.5	V
V_{SB}	St-by pin for standard bridge		3.5		5	V
V_{HE}	St-by pin for Hi-eff		7		18	V
I_O	St-by pin current	1.5 < $V_{stby/HE}$ < 18V	7	160	200	µA
	St-by pin current	V_{stby} < 1.5V	-10	0	10	µA
V_m	Mute pin voltage for mute mode		0		1.5	V
V_m	Mute pin voltage for play mode		3.5		18	V
I_m	Mute pin current (st_by)	V_{mute} = 0V, V_{stby} < 1.5V	-5	0	5	µA
I_m	Mute pin current (operative)	0V < V_{mute} < 18V, V_{stby} > 3.5V		65	100	µA
V_{I2C}	I^2C pin voltage for I^2C disabled		0		1.5	V
V_{I2C}	I^2C pin voltage for I^2C enabled		2.5		18	V
I^2C	I^2C pin current (st-by)	0V < I^2C EN < 18V, V_{stby} < 1.5V	-5	0	5	µA
I^2C	I^2C pin current (operative)	I^2C EN <18V, V_{stby}>3.5V	7	11	15	µA
$V_{1\Omega}$	1Ω pin voltage for 2ch mode		0		1.5	V
$V_{1\Omega}$	1Ω pin voltage for 1Ω mode		2.5		18	V
$I_{1\Omega}$	1Ω pin current (st-by)	0V < 1Ω <18V, V_{stby} < 1.5V	-5	0	5	µA
$I_{1\Omega}$	1Ω pin current (operative)	1Ω <18V, V_{stby} > 3.5V	7	11	15	µA
La	A pin voltage	Low logic level	0		1.5	V
Ha		High logic level	2.5		18	V
Ia	A pin current (st-by)	0V < A < 18V, V_{stby} < 1.5V	-5	0	5	µA
Ia	A pin current (operative)	A<18V, V_{stby} > 3.5V	7	11	15	µA
Lb	B pin voltage	Low logic level	0		1.5	V
Hb		High logic level	2.5		18	V
Ib	B pin current (st-by)	0V < B < 18V, V_{stby} < 1.5V	-5	0	5	µA
Ib	B pin current (operative)	B < 18V, V_{stby} > 3.5V	7	11	15	µA
T_W	Thermal warning			150		°C
T_{PI}	Thermal protection intervention			170		°C
I_{CDH}	Clip pin high leakage current	CD off, 0V < V_{CD} < 5.5V	-15	0	15	µA
I_{CDL}	Clip pin low sink current	CD on; V_{CD} < 300mV	1			mA
CD	Clip detect THD level	D0 (IB1) = 0	0.8	1.3	2.5	%
		D0 (IB1) = 1	5	10	15	%
(*) ST-BY Pin high enables I^2C bus; ST-BY Pin low puts the device in ST-BY condition.(see “prog” for more details)						

Table 4. Electrical characteristics (continued)
(V_S = 14.4V; f=1KHz; R_L=4Ω; T_{amb}= 25°C unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Turn on diagnostics (Power amplifier mode)						
Pgnd	Short to GND det. (below this limit, the Output is considered in Short Circuit to GND)	Power amplifier in st-by condition			1.2	V
Pvs	Short to Vs det. (above this limit, the Output is considered in Short Circuit to VS)		V_s -0.9			V
Pnop	Normal operation thresholds.(Within these limits, the Output is considered without faults).		1.8		V_s -1.5	V
Lsc	Shorted load det.				0.5	Ω
Lop	Open load det.		130			Ω
Lnop	Normal load det.		1.5		70	Ω
TUrn on diagnostics (Line driver mode)						
Pgnd	Short to GND det. (below this limit, the Output is considered in Short Circuit to GND)	Power amplifier in st-by			1.2	V
Pvs	Short to Vs det. (above this limit, the Output is considered in Short Circuit to VS)		V_s -0.9			V
Pnop	Normal operation thresholds.(Within these limits, the Output is considered without faults).		1.8		V_s -1.5	V
Lsc	Shorted load det.				1.5	Ω
Lop	Open load det.		400			Ω
Lnop	Normal load det.		4.5		200	Ω
Permanent diagnostics (Power amplifier mode or line driver mode)						
Pgnd	Short to GND det. (below this limit, the Output is considered in Short Circuit to GND)	Power amplifier in Mute or Play condition, one or more short circuits protection activated			1.2	V
Pvs	Short to Vs det. (above this limit, the Output is considered in Short Circuit to VS)		V_s - 0.9			V
Pnop	Normal operation thresholds.(Within these limits, the Output is considered without faults).		1.8		V_s -1.5	V
Lsc	Shorted load det.	Pow. amp. mode			0.5	Ω
		Line driver mode			1.5	Ω

Table 4. Electrical characteristics (continued)
(V_S = 14.4V; f=1KHz; R_L=4Ω; T_{amb}= 25°C unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_O	Offset detection	Power amplifier in play condition AC input signals = 0	±1.5	±2	±2.5	V
I_{NLH}	Normal load current detection	V_O < (V_S - 5)pk IB2 (D0) = 0	500			mA
I_{NLL}	Normal load current detection	V_O < (V_S - 5)pk IB2 (D0) = 1	250			mA
I_{OLH}	Open load current detection	V_O < (V_S - 5)pk IB2 (D0) = 0			250	mA
I_{OLL}	Open load current detection	V_O < (V_S - 5)pk IB2 (D0) =1			125	mA
I^2C bus interface						
f_{SCL}	Clock frequency				400	KHz
V_{IL}	Input low voltage				1.5	V
V_{IH}	Input high voltage		2.3			V

1. Saturated sqare wave output.

3 Electrical characteristics curves

Figure 3. Quiescent drain current vs. supply voltage

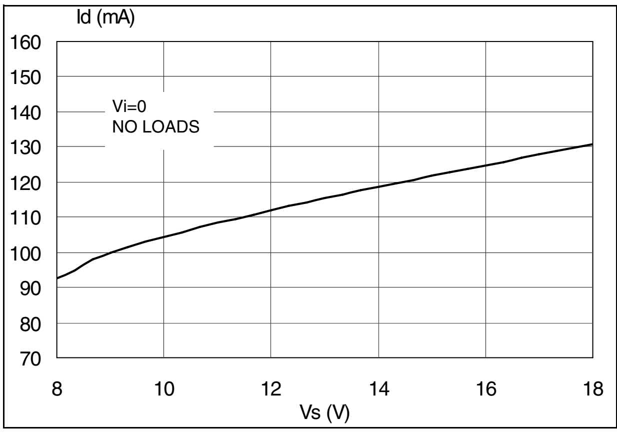


Figure 4. Output power vs. supply voltage

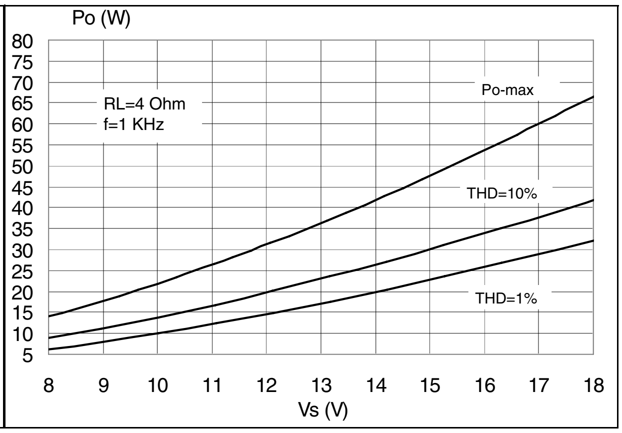


Figure 5. Output power vs. supply voltage

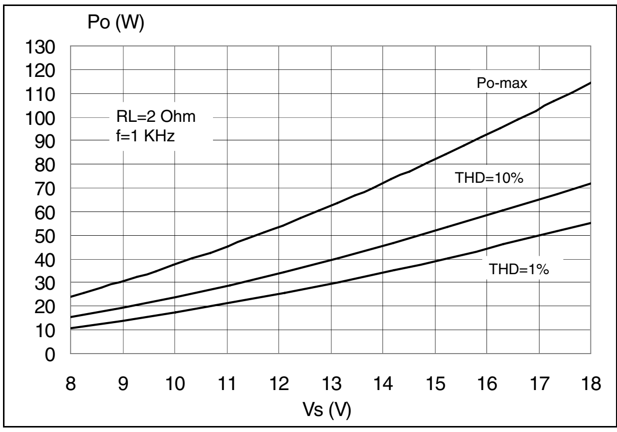


Figure 6. Output power vs. supply voltage

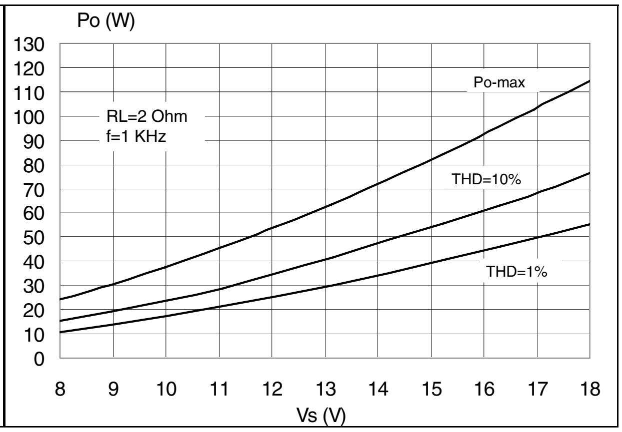


Figure 7. Distortion vs. output power

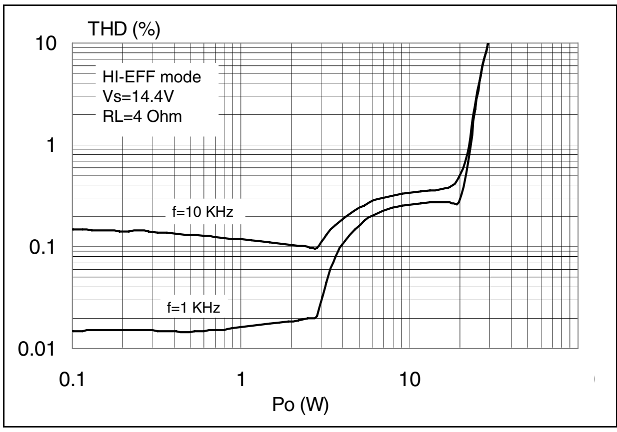


Figure 8. Distortion vs. output power

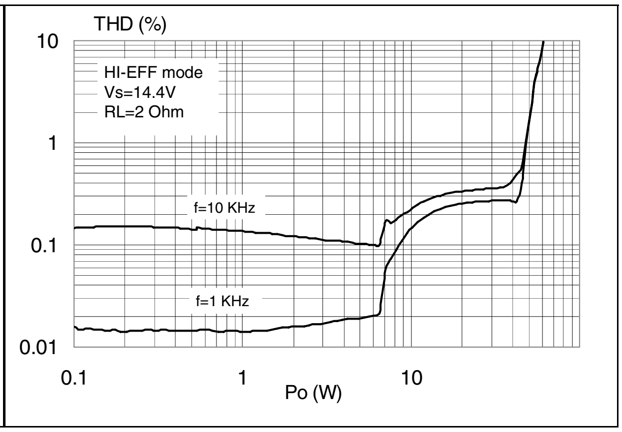


Figure 9. Distortion vs. output power

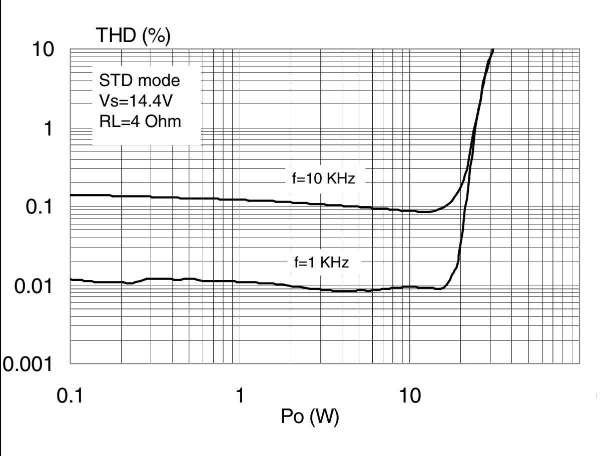


Figure 10. Distortion vs. output power

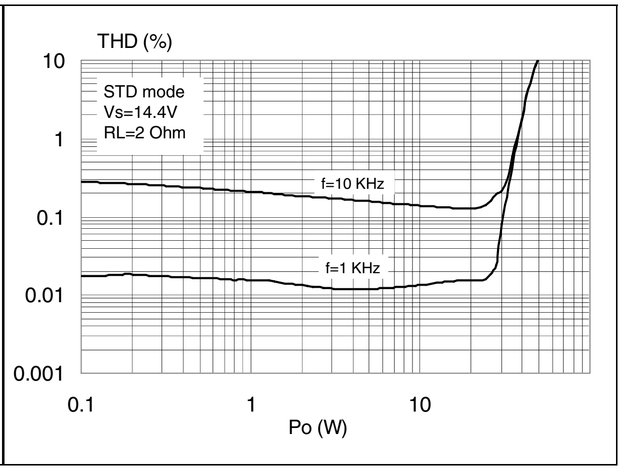


Figure 11. Distortion vs. output power

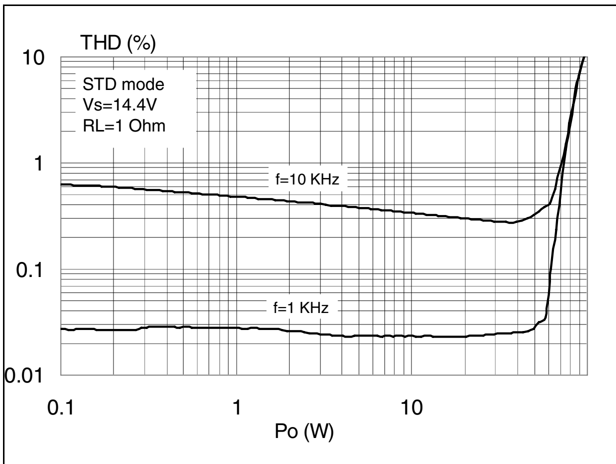


Figure 12. Distortion vs. frequency

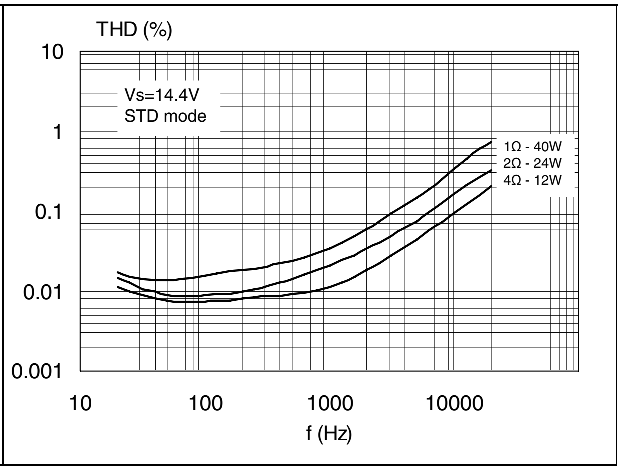


Figure 13. Distortion vs. output voltage (LD mode)

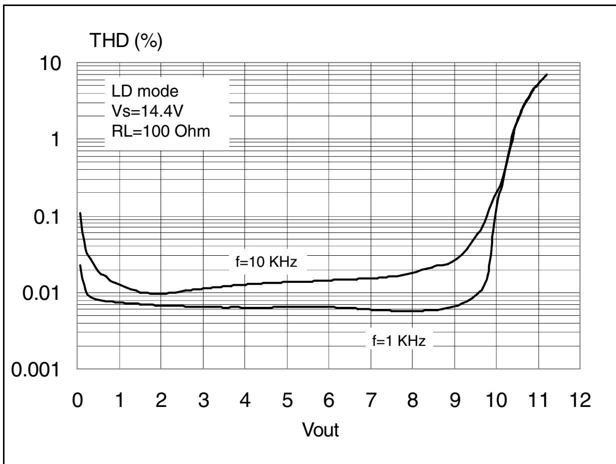


Figure 14. Cross talk vs. frequency

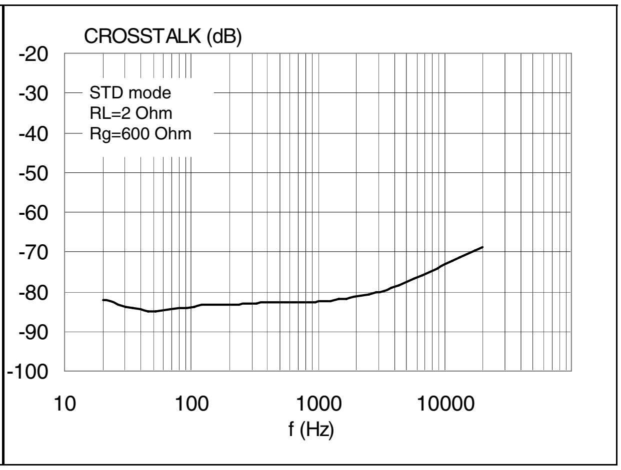


Figure 15. Cross talk vs. frequency (LD mode)

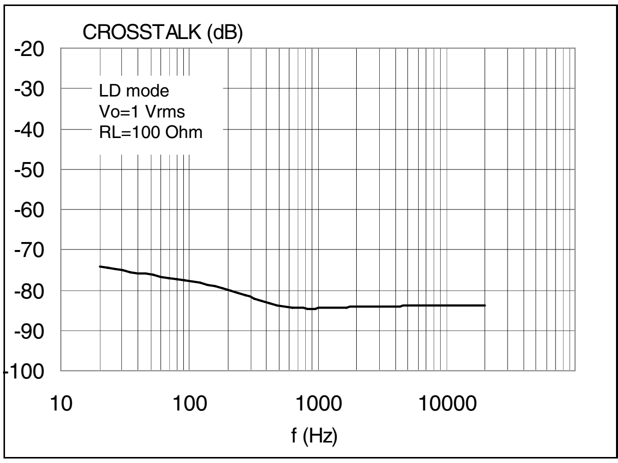


Figure 16. CMRRR vs. frequency

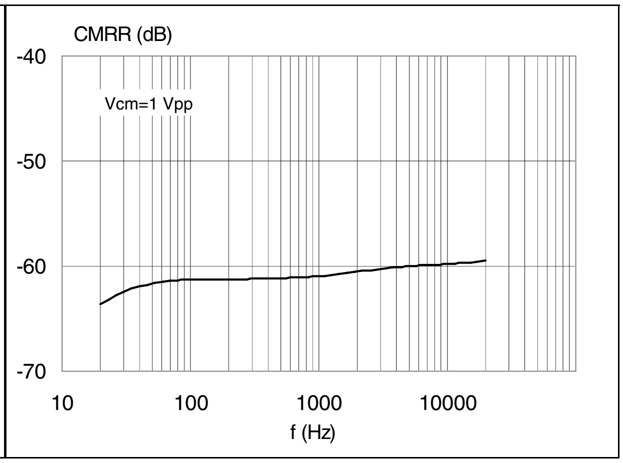


Figure 17. Output attenuation vs. supply voltage (vs. dependent muting)

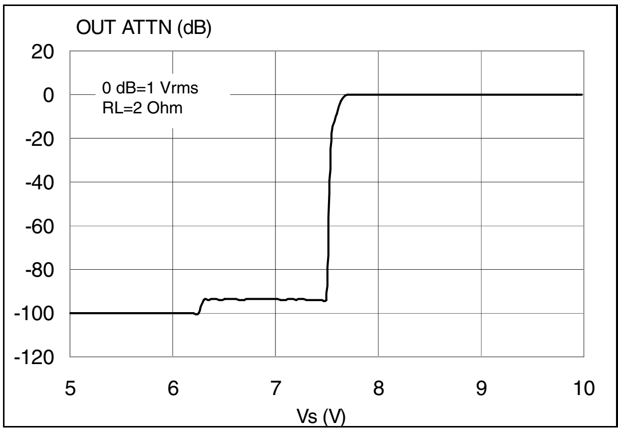


Figure 18. Output attenuation vs. mute pin voltage

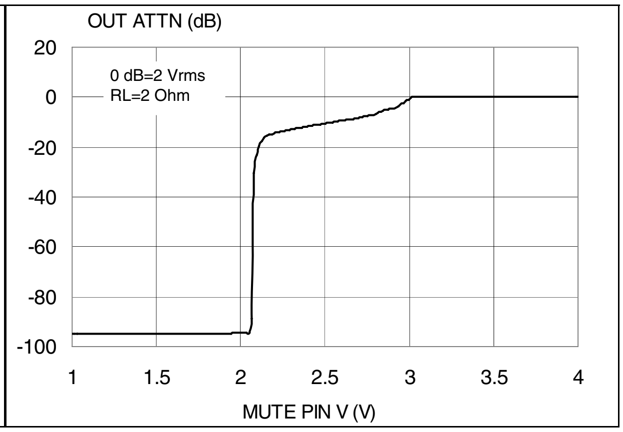


Figure 19. Power dissipation vs. output power (4Ω - SINE)

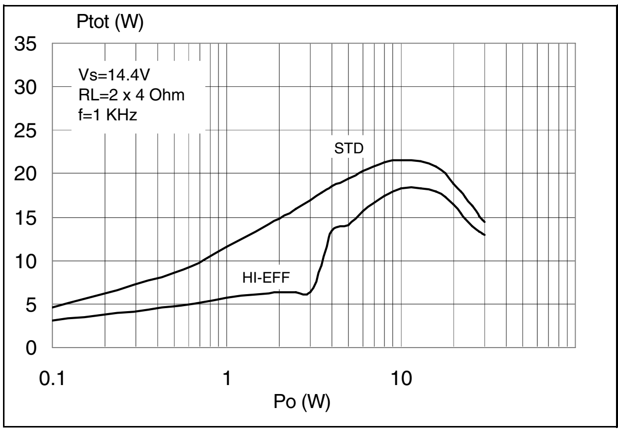


Figure 20. Power dissipation vs. output power (2Ω - SINE)

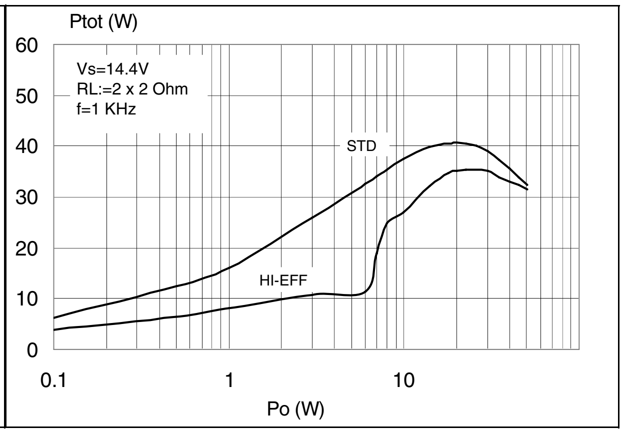


Figure 21. Power dissipation vs. average output power (Audio program simulation, 4Ω)

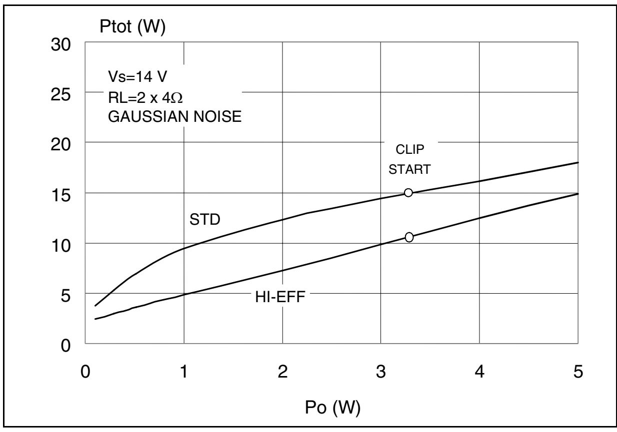


Figure 22. Power dissipation vs. average output power (Audio program simulation, 2Ω)

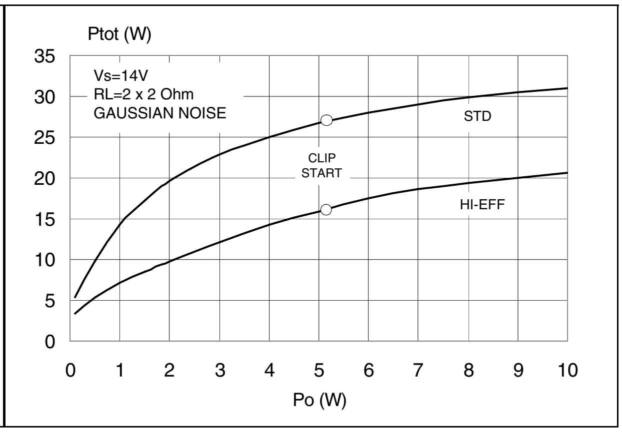
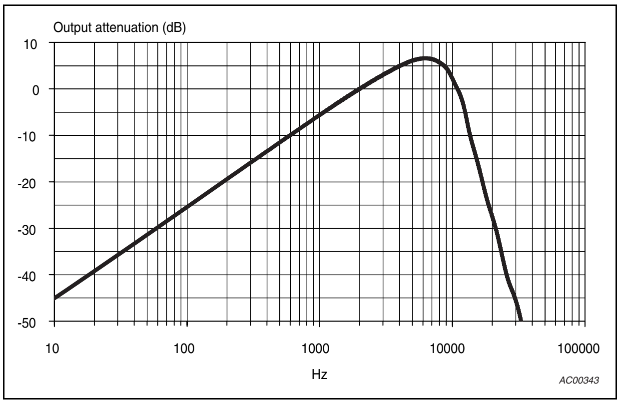


Figure 23. ITU R-ARM frequency response, weighting filter for transient pop



4 Application circuit

Figure 24. Application circuit (TDA7575B)

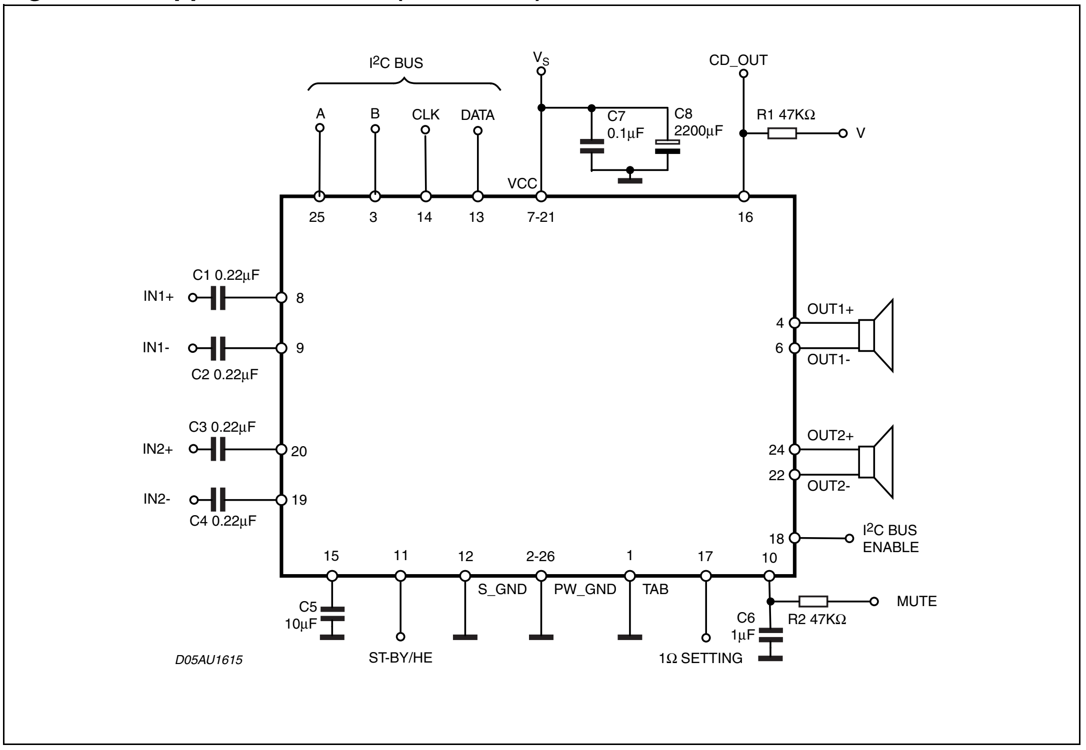
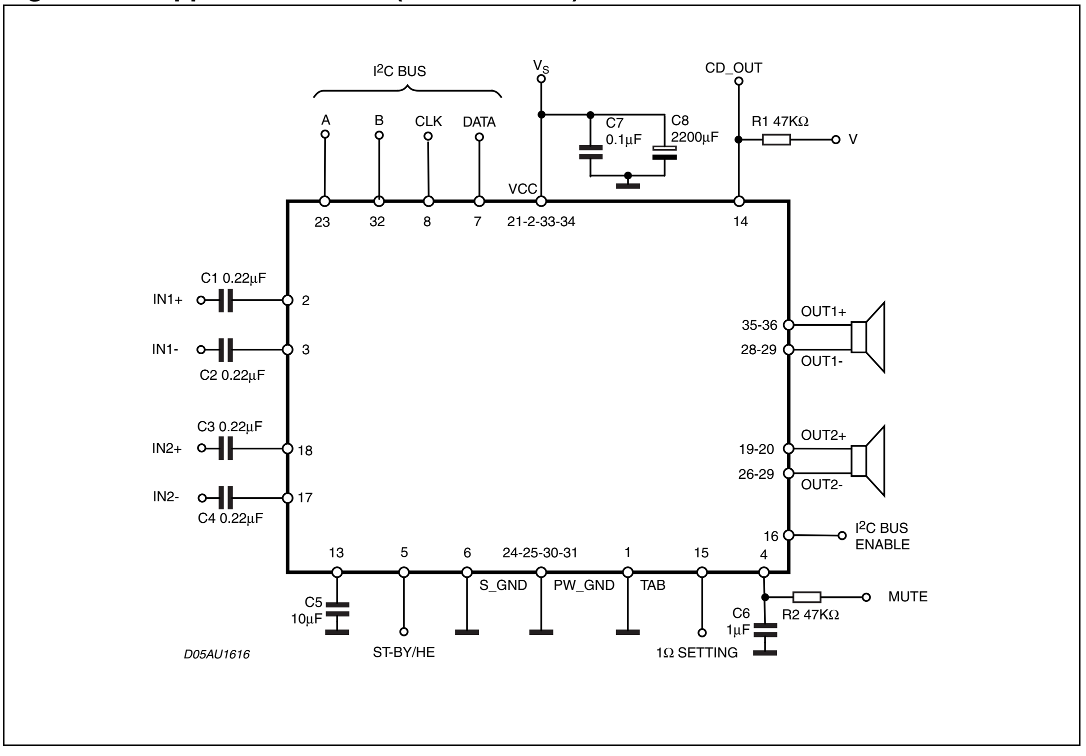


Figure 25. Application circuit (TDA7575BPD)



5 I^2C bus interface

Data transmission from microprocessor to the TDA7575B and vice versa takes place through the 2 wires I^2C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

5.1 Data validity

As shown by *Figure 26*, the data on the SDA line must be stable during the high period of the clock.
The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

5.2 Start and stop conditions

As shown by *Figure 27* a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH.
The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

5.3 Byte format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

5.4 Acknowledge

The transmitter(*) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see *Figure 28*). The receiver(**) the acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.

(*) Transmitter
- = master (μP) when it writes an address to the TDA7575B
- = slave (TDA7575B) when the μP reads a data byte from TDA7575B

(**) Receiver
- = slave (TDA7575B) when the μP writes an address to the TDA7575B
- = master (μP) when it reads a data byte from TDA7575B

Figure 26. Data validity on the I^2C bus

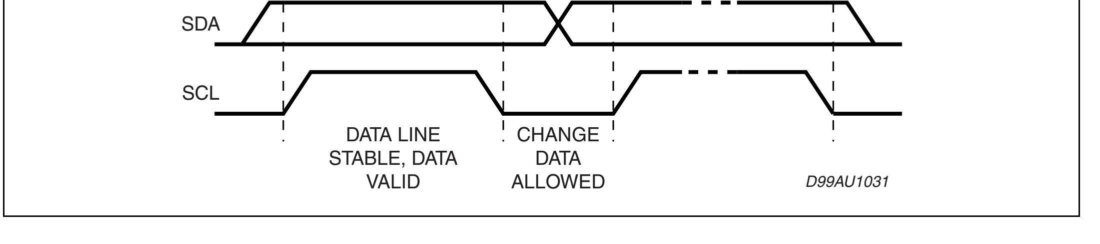


Figure 27. Timing diagram on the I^2C bus

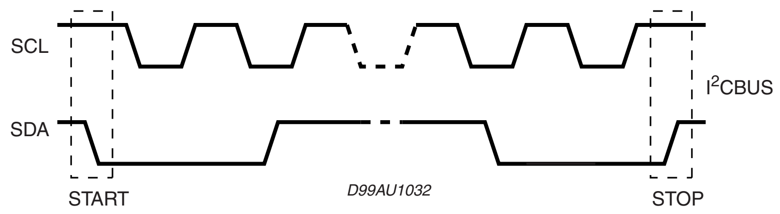
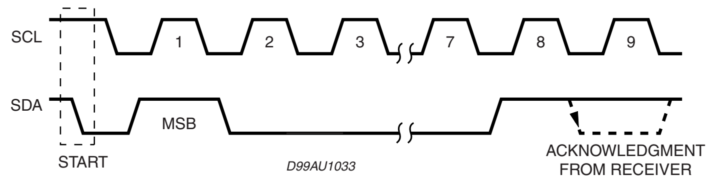


Figure 28. Timing acknowledge clock pulse



5.5 1Ω capability setting

It is possible to drive 1Ω load paralleling the outputs into a single channel.

In order to implement this feature, outputs are to be connected on the board as follows:

OUT1+ (PIN35 and PIN36) shorted to OUT2+ (PIN19 and PIN20)

OUT1- (PIN28 and PIN29) shorted to OUT2- (PIN26 and PIN27).

It is recommended to minimize the impedance on the board between OUT2 and the load in order to minimize THD distortion. It is also recommended to control the maximum mismatch impedance between V_{CC} pins (PIN21/PIN22 respect to PIN33/PIN34) and between PWGND pins (PIN24/PIN25 respect to PIN30/PIN31), mismatch that must not exceed a value of 20 mΩ.

With 1Ω feature settled the active input is IN2 (PIN17 and PIN18), therefore IN1 pins should be let floating.

It is possible to set the load capability acting on 1Ω pin as follows:

1Ω PIN (PIN15) < 1.5V: two channels mode (for a minimum load of 2Ω)

1Ω PIN (PIN15) > 2.5V: one channel mode (for 1Ω load).

IT IS TO REMEMBER THAT 1

OHM FUNCTION IS A HARDWARE SELECTION.

Therefore it is recommended to leave 1Ω PIN floating or shorted to GND to set the two channels mode configuration, or to short 1Ω PIN to V_{CC} to set the one channel (1Ω) configuration.

5.6 I^2C abilitation setting

It is possible to disable the I^2C interface by acting on I^2C PIN (PIN16) and control the TDA7575B by means of the usual ST-BY and MUTE pins. In order to activate or deactivate this feature, I^2C PIN must be set as follows:

I^2C PIN (PIN16) < 1.5V: I^2C bus interface deactivated

I^2C PIN (PIN16) > 2.5V: I^2C bus interface activated

It is also possible to let I^2C PIN floating to deactivate the I^2C bus interface, or to short I^2C PIN to V_{CC} to activate it.

In particular:

I^2C ENABLED: I^2C pin (PIN16) > 2.5V

- STD MODE: V_{stby} (PIN5) > 3.5V, IB2(D1)=0
- HE MODE: V_{stby} (PIN5) > 3.5V, IB2(D1)=1
- PLAY MODE: V_{mute} (pin 4) >3.5V, IB1 (D2) = 1

The amplifier can always be switched off by putting V_{stby} to 0V, but with I^2C enabled it can be turn on only through I^2C (with V_{stby}>3.5V).

I^2C DISABLED: I^2C pin (PIN16) < 1.5V

- STD MODE: 3.5V < st-by (PIN5) < 5
- HE MODE: V_{stby} (PIN5) > 7V
- PLAY MODE: V_{mute} (pin 4) >3.5V

For both STD and HE MODE the play/mute mode can be set acting on V_{mute} pin.

When I^2C BUS is disabled, when a fault is detected PIN 14 (CD-OUT) is pulled down by the internal logic circuitry. The faults detected are the short circuit to ground, to V_{CC} and across the load (after an aver current detection).

6 Software specifications

All the functions of the TDA7575B are activated by I^2C interface.

The bit 0 of the "ADDRESS BYTE" defines if the next bytes are write instruction (from µP to TDA7575B) or read instruction (from TDA7575B to µP).

Table 5. Address selection

A6	1
A5	1
A4	0
A3	1
A2	0
A1	B
A0	A
R/W	X

If R/W = 0, the µP sends 2 "Instruction Bytes": IB1 and IB2.

Table 6. IB1

D7	0
D6	Diagnostic enable (D6 = 1) Diagnostic defeat (D6 = 0)
D5	Offset Detection enable (D5 = 1) Offset Detection defeat (D5 = 0)
D4	Gain = 26dB (D4 = 0) Gain = 12dB (D4 = 1)
D3	0
D2	Mute (D2 = 0) Unmute (D2 = 1)
D1	0
D0	CD 2% (D0 = 0) CD 10% (D0 = 1)

Table 7. IB2

D7	0
D6	0
D5	0
D4	Stand-by on - Amplifier not working - (D4 = 0) Stand-by off - Amplifier working - (D4 = 1)
D3	Power Amplifier Mode Diagnostic (D3 = 0); Line Driver Mode Diagnostic (D3 = 1)
D2	Current Detection Diagnostic Enabled (D2 = 1) Current Detection Diagnostic Defeat (D2 = 0)
D1	Power amplifier working in standard mode (D1 = 0) Power amplifier working in high efficiency mode (D1 = 1)
D0	Current Detection Threshold HIGH (D7 =0) Current Detection Threshold LOW (D7 =1)

If R/W = 1, the TDA7575B sends 2 "Diagnostics Bytes" to µP: DB1 and DB2.

Table 8. DB1

D7	Thermal warming (if Tchip ≥ 150°C, D7 = 1)	
D6	Diag. cycle not activated or not terminated (D6 = 0) Diag. cycle terminated (D6 = 1)	
D5	Channel 1 current detection IB2 (D0) = 0 Output peak current < 250 mA - Open load (D5 = 1) Output peak current > 500 mA - Normal load (D5 = 0)	Channel LF current detection IB2 (D0) = 1 Output peak current < 125 mA - Open load (D5 = 1) Output peak current > 250 mA - Normal load (D5 = 0)
D4	Channel 1 Turn-on diagnostic (D4 = 0) Permanent diagnostic (D4 = 1)	
D3	Channel 1 Normal load (D3 = 0) Short load (D3 = 1)	
D2	Channel 1 Turn-on diag.: No open load (D2 = 0) Open load detection (D2 = 1) Offset diag.: No output offset (D2 = 0) Output offset detection (D2 = 1)	
D1	Channel 1 No short to V_{cc} (D1 = 0) Short to V_{cc} (D1 = 1)	
D0	Channel 1 No short to GND (D1 = 0) Short to GND (D1 = 1)	

Table 9. DB2

D7	Offset detection not activated (D7 = 0) Offset detection activated (D7 = 1)	
D6	Current sensor not activated (D6 = 0) Current sensor activated (D6 = 1)	
D5	Channel LR Current detection IB2 (D0) = 0 Output peak current < 250 mA - Open load (D5 = 1) Output peak current > 500 mA - Normal load (D5 = 0)	Channel LR Current detection IB2 (D0) = 1 Output peak current < TBD mA - Open load (D5 = 1) Output peak current > TBD mA - Normal load (D5 = 0)
D4	Channel 2 Turn-on diagnostic (D4 = 0) Permanent diagnostic (D4 = 1)	
D3	Channel 2 Normal load (D3 = 0) Short load (D3 = 1)	
D2	Channel 2 Turn-on diag.: No open load (D2 = 0) Open load detection (D2 = 1) Permanent diag.: No output offset (D2 = 0) Output offset detection (D2 = 1)	
D1	Channel 2 No short to V_{cc} (D1 = 0) Short to V_{cc} (D1 = 1)	
D0	Channel 2 No short to GND (D1 = 0) Short to GND (D1 = 1)	

6.1 Examples of bytes sequence

1 - Turn-On diagnostic - Write operation

Start	Address byte with D0 = 0	ACK	IB1 with D6 = 1	ACK	IB2	ACK	STOP

2 - Turn-On diagnostic - Read operation

Start	Address byte with D0 = 1	ACK	DB1	ACK	DB2	ACK	STOP

The delay from 1 to 2 can be selected by software, starting from T.B.D. ms

3a - Turn-On of the power amplifier with mute on, diagnostic defeat.

Start	Address byte with D0 = 0	ACK	IB1	ACK	IB2	ACK	STOP
			X000XXXX		XXX1XX1X		

3b - Turn-Off of the power amplifier

Start	Address byte with D0 = 0	ACK	IB1	ACK	IB2	ACK	STOP
			X0XXXXXX		XXX0XXXX		

4 - Offset detection procedure enable

Start	Address byte with D0 = 0	ACK	IB1	ACK	IB2	ACK	STOP
			XX1XX1XX		XXX1XXXX		

5 - Offset detection procedure stop and reading operation (the results are valid only for the offset detection bits (D2 of the bytes DB1, DB2, DB3, DB4).

Start	Address byte with D0 = 1	ACK	DB1	ACK	DB2	ACK	STOP

- The purpose of this test is to check if a D.C. offset (2V typ.) is present on the outputs, produced by input capacitor with anomalous leakage current or humidity between pins.
- The delay from 4 to 5 can be selected by software, starting from T.B.D. ms

7 Diagnostics functional description

7.1 Turn-on diagnostic

It is activated at the turn-on (stand-by out) under I^2C bus request. Detectable output faults are:

- SHORT TO GND
- SHORT TO Vs
- SHORT ACROSS THE SPEAKER
- OPEN SPEAKER

To verify if any of the above misconnections are in place, a subsonic (inaudible) current pulse (*Figure 29*) is internally generated, sent through the speaker(s) and sunk back. The Turn On diagnostic status is internally stored until a successive diagnostic pulse is requested (after a I^2C reading).

If the "stand-by out" and "diag. enable" commands are both given through a single programming step, the pulse takes place first (power stage still in stand-by mode, low, outputs = high impedance).

Afterwards, when the Amplifier is biased, the PERMANENT diagnostic takes place. The previous Turn On state is kept until a short appears at the outputs.

Figure 29. Turn - on diagnostic: working principle

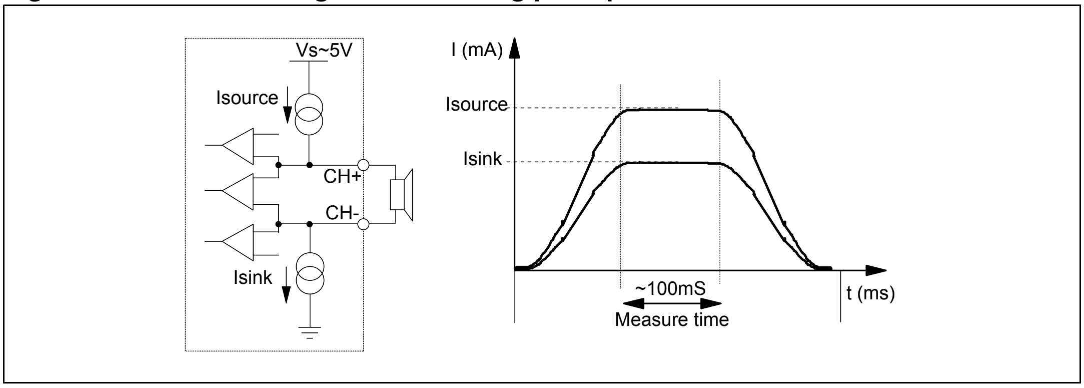


Fig. *Figure 30* and *Figure 31* show SVR and OUTPUT waveforms at the turn-on (stand-by out) with and without Turn-on diagnostic.

Figure 30. SVR and output behavior - case 1: without turn-on diagnostic

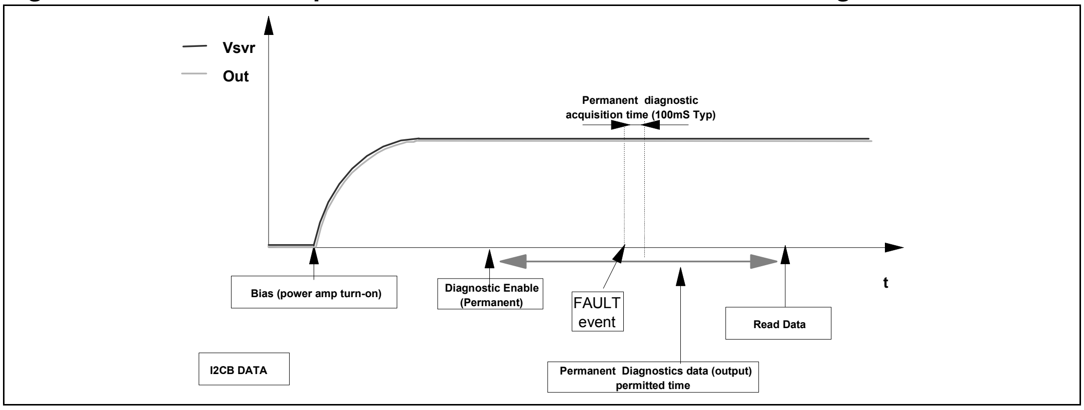
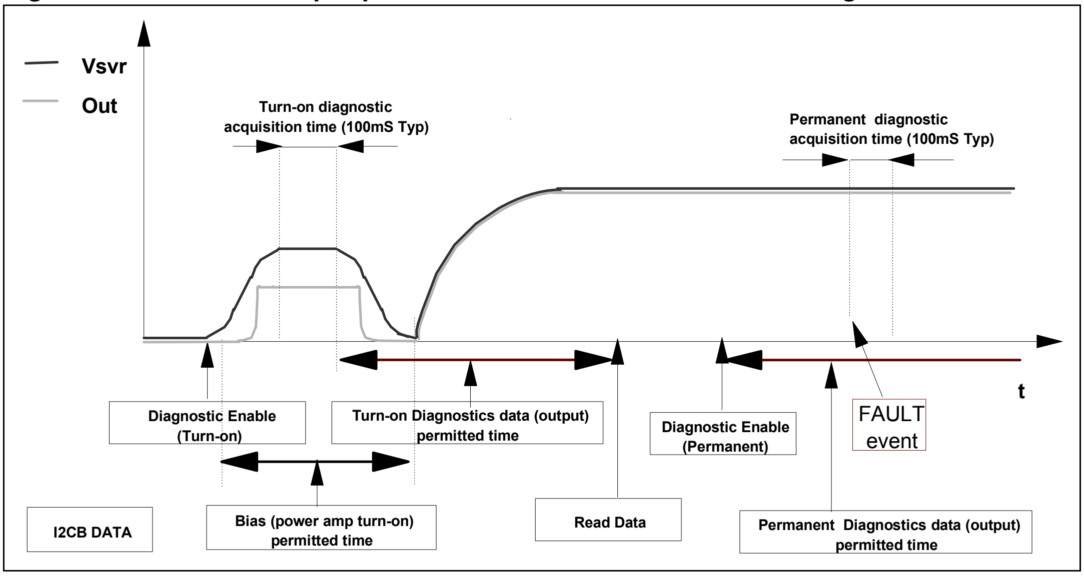
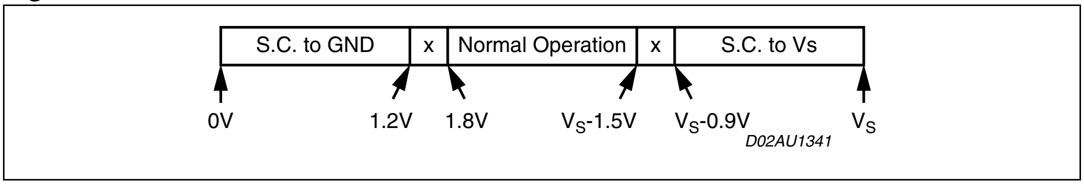


Figure 31. SVR and output pin behavior - case 2: with turn-on diagnostic



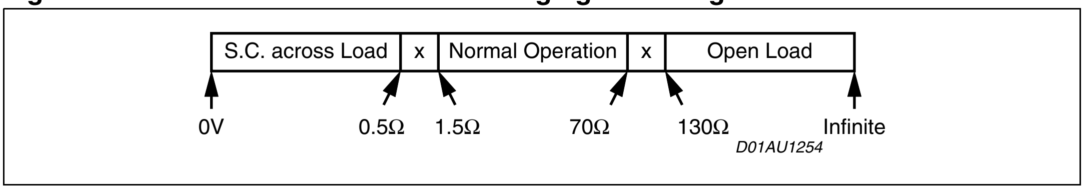
The information related to the outputs status is read and memorized at the end of the current pulse top. The acquisition time is 100 ms (typ.). No audible noise is generated in the process. As for SHORT TO GND / Vs the fault-detection thresholds remain unchanged from 26 dB to 12 dB gain setting. They are as follows:

Figure 32. Short circuit detection thresholds



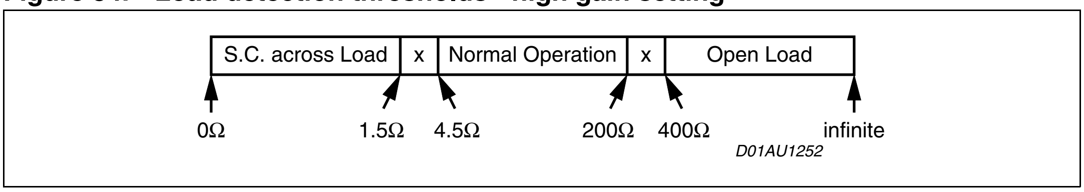
Concerning SHORT ACROSS THE SPEAKER / OPEN SPEAKER, the threshold varies from 26 dB to 12 dB gain setting, since different loads are expected (either normal speaker's impedance or high impedance). The values in case of 26 dB gain are as follows:

Figure 33. Load detection thresholds - high gain setting



If the Line-Driver mode (Gv= 12 dB and Line Driver Mode diagnostic = 1) is selected, the same thresholds will change as follows:

Figure 34. Load detection thresholds - high gain setting



7.2 Permanent diagnostics

Detectable conventional faults are:
- SHORT TO GND
- SHORT TO Vs
- SHORT ACROSS THE SPEAKER

The following additional features are provided:
- OUTPUT OFFSET DETECTION

The TDA7575B has 2 operating statuses:
1. RESTART mode. The diagnostic is not enabled. Each audio channel operates independently from each other. If any of the a.m. faults occurs, only the channel(s) interested is shut down. A check of the output status is made every 1 ms (fig. 30). Restart takes place when the overload is removed.
2. DIAGNOSTIC mode. It is enabled via I^2C bus and self activates if an output overload (such to cause the intervention of the short-circuit protection) occurs to the speakers outputs. Once activated, the diagnostics procedure develops as follows (fig. 31):
   - To avoid momentary re-circulation spikes from giving erroneous diagnostics, a check of the output status is made after 1ms: if normal situation (no overloads) is detected, the diagnostic is not performed and the channel returns back active.
   - Instead, if an overload is detected during the check after 1 ms, then a diagnostic cycle having a duration of about 100 ms is started.
   - After a diagnostic cycle, the audio channel interested by the fault is switched to RESTART mode. The relevant data are stored inside the device and can be read by the microprocessor. When one cycle has terminated, the next one is activated by an I^2C reading. This is to ensure continuous diagnostics throughout the car-radio operating time.
   - To check the status of the device a sampling system is needed. The timing is chosen at microprocessor level (over than half a second is recommended).

Figure 35. Restart timing without diagnostic enable (permanent) each 1ms time, a sampling of the fault is done

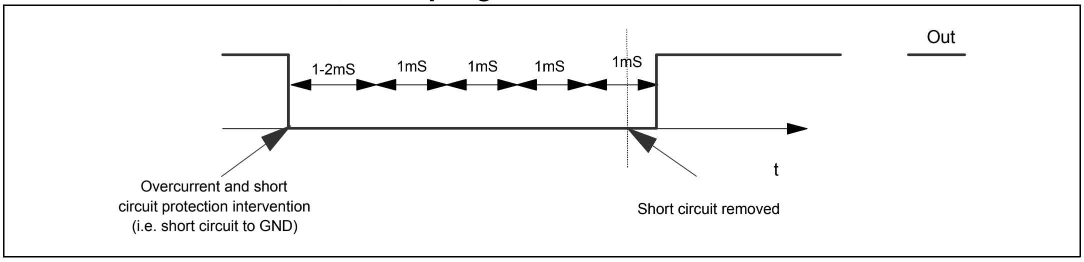
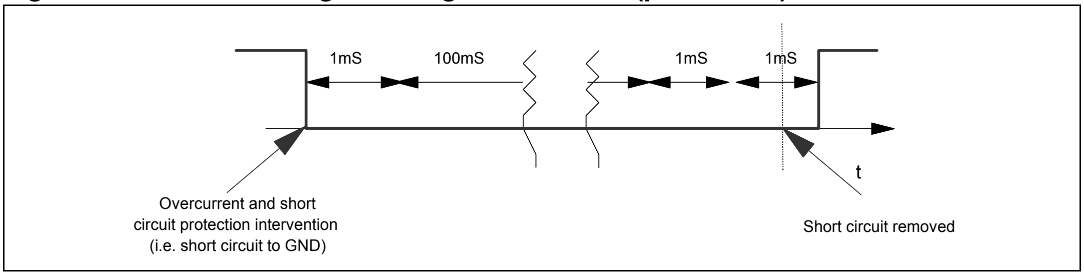


Figure 36. Restart timing with diagnostic enable (permanent)



7.3 Output DC offset detection

Any DC output offset exceeding +/- 2 V are signalled out. This inconvenient might occur as a consequence of initially defective or aged and worn-out input capacitors feeding a DC component to the inputs, so putting the speakers at risk of overheating.

This diagnostic has to be performed with low-level output AC signal (or Vin = 0).

The test is run with selectable time duration by microprocessor (from a "start" to a "stop" command):

- START = Last reading operation or setting IB1 - D5 - (OFFSET enable) to 1
- STOP = Actual reading operation

Excess offset is signalled out if persistent throughout the assigned testing time. This feature is disabled if any overloads leading to activation of the short-circuit protection occurs in the process.

7.4 AC diagnostic

It is targeted at detecting accidental disconnection of tweeters in 2-way speaker and, more in general, presence of capacitively (AC) coupled loads.

This diagnostic is based on the notion that the overall speaker's impedance (woofer + parallel tweeter) will tend to increase towards high frequencies if the tweeter gets disconnected, because the remaining speaker (woofer) would be out of its operating range (high impedance). The diagnostic decision is made according to peak output current thresholds, and it is enabled by setting (IB2-D2) = 1. Two different detection levels are available:

- HIGH CURRENT THRESHOLD IB2 (D7) = 0

  Iout > 500mApk = NORMAL STATUS

  Iout < 250mApk = OPEN TWEETER
- LOW CURRENT THRESHOLD IB2 (D7) = 1

  Iout > 250mApk = NORMAL STATUS

  Iout < 125mApk = OPEN TWEETER

To correctly implement this feature, it is necessary to briefly provide a signal tone (with the amplifier in "play") whose frequency and magnitude are such to determine an output current higher than 500mApk with IB2(D7)=0 (higher than 250mApk with IB2(D7)=1) in normal conditions and lower than 250mApk with IB2(D7)=0 (lower than 125mApk with IB2(D7)=1) should the parallel tweeter be missing.

The test has to last for a minimum number of 3 sine cycles starting from the activation of the AC diagnostic function IB2<D2>) up to the I^2C reading of the results (measuring period). To confirm presence of tweeter, it is necessary to find at least 3 current pulses over the above threholds over all the measuring period, else an "open tweeter" message will be issued.

The frequency / magnitude setting of the test tone depends on the impedance characteristics of each specific speaker being used, with or without the tweeter connected (to be calculated case by case). High-frequency tones (> 10 KHz) or even ultrasonic signals are recommended for their negligible acoustic impact and also to maximize the impedance module's ratio between with tweeter-on and tweeter-off.

Figure 37 shows the Load Impedance as a function of the peak output voltage and the relevant diagnostic fields.
This feature is disabled if any overloads leading to activation of the short-circuit protection occurs in the process.

Figure 37. Current detection high: Load impedance |Z| vs. output peak voltage

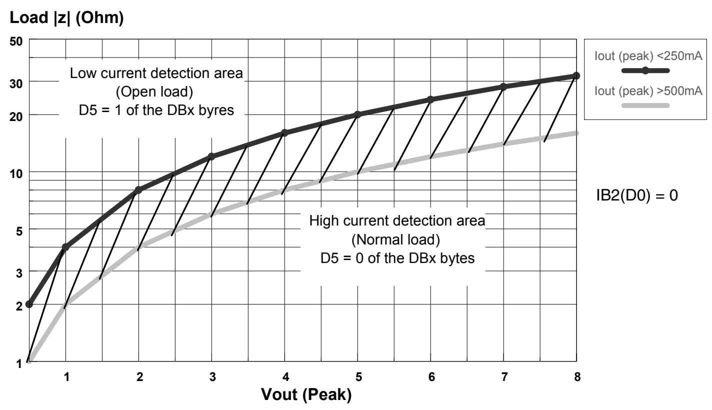
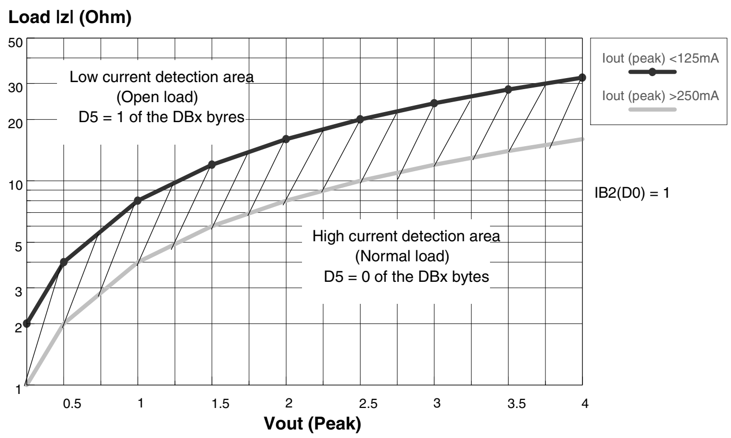


Figure 38. Current detection low: Load impedance |Z| vs. output peak voltage



7.5 Multiple faults

When more misconnections are simultaneously in place at the audio outputs, it is guaranteed that at least one of them is initially read out. The others are notified after successive cycles of I^2C reading and faults removal, provided that the diagnostic is enabled. This is true for both kinds of diagnostic (Turn on and Permanent).

The table below shows all the couples of double-fault possible. It should be taken into account that a short circuit with the 4Ω speaker unconnected is considered as double fault.

Table 10. Double fault table for turn on diagnostic

	S. GND (sc)	S. GND (sk)	S. Vs	S. Across L.	Open L.
S. GND (sc)	S. GND	S. GND	S. Vs + S. GND	S. GND	S. GND
S. GND (sk)	/	S. GND	S. Vs	S. GND	Open L. (*)
S. Vs	/	/	S. Vs	S. Vs	S. Vs
S. Across L.	/	/	/	S. Across L.	N.A.
Open L.	/	/	/	/	Open L. (*)

S. GND (so) / S. GND (sk) in the above table make a distinction according to which of the 2 outputs is shorted to ground (test-current source side= so, test-current sink side = sk). More precisely, in both the Channels SO = CH+, and SK = CH-.

In Permanent Diagnostic the table is the same, with only a difference concerning Open Load(*), which is not among the recognizable faults. Should an Open Load be present during the device's normal working, it would be detected at a subsequent Turn on Diagnostic cycle (i.e. at the successive Car Radio Turn on).

7.6 Faults availability

All the results coming from I^2C bus, by read operations, are the consequence of measurements inside a defined period of time. If the fault is stable throughout the whole period, it will be sent out. This is true for DC diagnostic (Turn on and Permanent), for Offset Detector.

To guarantee always resident functions, every kind of diagnostic cycles (Turn on, Permanent, Offset) will be reactivate after any I^2C reading operation. So, when the micro reads the I^2C, a new cycle will be able to start, but the read data will come from the previous diag. cycle (i.e. The device is in Turn On state, with a short to Gnd, then the short is removed and micro reads I^2C. The short to Gnd is still present in bytes, because it is the result of the previous cycle. If another I^2C reading operation occurs, the bytes do not show the short). In general to observe a change in Diagnostic bytes, two I^2C reading operations are necessary.

7.7 I^2C programming/reading sequences

A correct turn on/off sequence respectful of the diagnostic timings and producing no audible noises could be as follows (after battery connection):

- TURN-ON: (STAND-BY OUT + DIAG ENABLE) --- 500 ms (min) --- MUTING OUT
- TURN-OFF: MUTING IN --- 20 ms --- (DIAG DISABLE + STAND-BY IN)

Car Radio Installation: DIAG ENABLE (write) --- 200ms --- I^2C read (repeat until All faults disappear).

- OFFSET TEST: Device in Play (no signal) --
- OFFSET ENABLE - 30ms - I^2C reading

(repeat I^2C reading until high-offset message disappears).

8 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

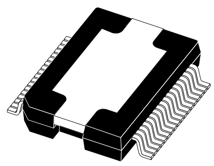
ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 39. PowerSO36 (slug up) mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.25		3.43	0.128		0.135
A2	3.1		3.2	0.122		0.126
A4	0.8		1	0.031		0.039
A5		0.2			0.008	
a1	0.030		-0.040	0.0011		-0.0015
b	0.22		0.38	0.008		0.015
c	0.23		0.32	0.009		0.012
D	15.8		16	0.622		0.630
D1	9.4		9.8	0.37		0.38
D2		1			0.039	
E	13.9		14.5	0.547		0.57
E1	10.9		11.1	0.429		0.437
E2			2.9			0.114
E3	5.8		6.2	0.228		0.244
E4	2.9		3.2	0.114		1.259
e		0.65			0.026	
e3		11.05			0.435	
G	0		0.075	0		0.003
H	15.5		15.9	0.61		0.625
h			1.1			0.043
L	0.8		1.1	0.031		0.043
N			10°			10°
s			8°			8°

(1) "D and E1" do not include mold flash or protusions.
Mold flash or protusions shall not exceed 0.15mm (0.006")
(2) No intrusion allowed inwards the leads.

OUTLINE AND MECHANICAL DATA



PowerSO36 (SLUG UP)

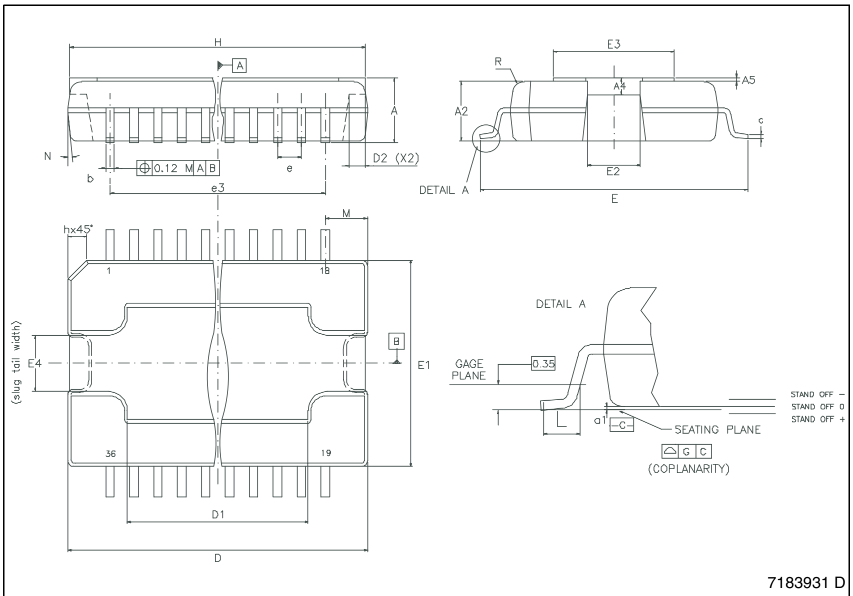
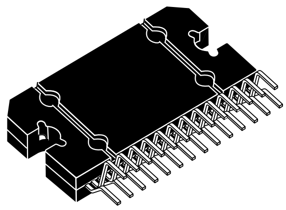


Figure 40. Flexiwatt 27 mechanical data and package dimensions

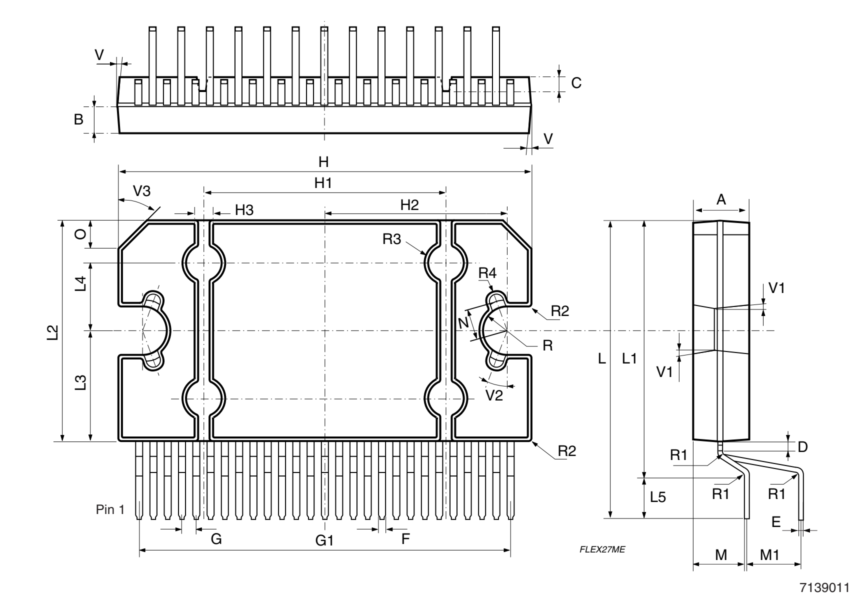
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.45	4.50	4.65	0.175	0.177	0.183
B	1.80	1.90	2.00	0.070	0.074	0.079
C		1.40			0.055	
D	0.75	0.90	1.05	0.029	0.035	0.041
E	0.37	0.39	0.42	0.014	0.015	0.016
F (1)			0.57			0.022
G	0.80	1.00	1.20	0.031	0.040	0.047
G1	25.75	26.00	26.25	1.014	1.023	1.033
H (2)	28.90	29.23	29.30	1.139	1.150	1.153
H1		17.00			0.669	
H2		12.80			0.503	
H3		0.80			0.031	
L (2)	22.07	22.47	22.87	0.869	0.884	0.904
L1	18.57	18.97	19.37	0.731	0.747	0.762
L2 (2)	15.50	15.70	15.90	0.610	0.618	0.626
L3	7.70	7.85	7.95	0.303	0.309	0.313
L4		5			0.197	
L5		3.5			0.138	
M	3.70	4.00	4.30	0.145	0.157	0.169
M1	3.60	4.00	4.40	0.142	0.157	0.173
N		2.20			0.086	
O		2			0.079	
R		1.70			0.067	
R1		0.5			0.02	
R2		0.3			0.12	
R3		1.25			0.049	
R4		0.50			0.019	
V	5° (Typ.)					
V1	3° (Typ.)					
V2	20° (Typ.)					
V3	45° (Typ.)					

(1): dam-bar protusion not included
(2): molding protusion included

OUTLINE AND MECHANICAL DATA



Flexiwatt27 (vertical)



9 Revision history

Table 11. Document revision history

Date	Revision	Changes
30-Oct-2007	1	Initial release.