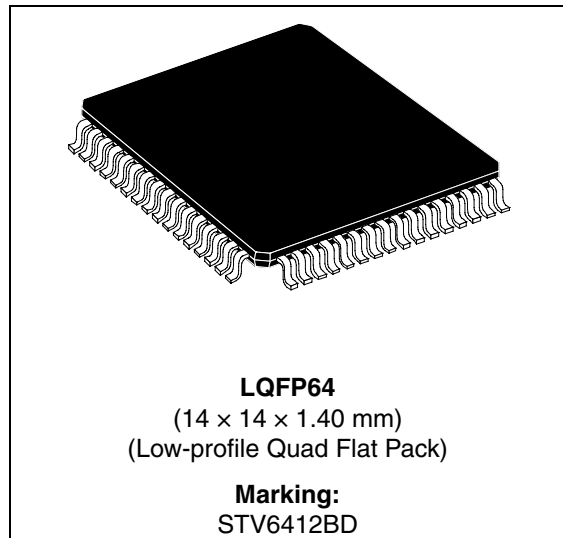


Audio/video switch matrix

Features

- I²C bus control
- Standby mode with interrupt signal output
- Video section
 - 4 CVBS inputs, 3 CVBS outputs (one with selectable chroma trap filter)
 - 3 Y/C inputs, 2 Y/C outputs
 - Switchable LPFs (low pass filters) on 6 inputs
 - 6 dB gain on all CVBS/Y and C outputs
 - Integrated 150 Ω buffers
 - 1 Y/C adder
 - 2 RGB/FB inputs, 1 tri-state RGB/FB output with 6 dB adjustable gain (from +3 dB to +9 dB)
 - Video muting on all outputs
 - 2 slow blanking inputs/outputs
 - Sync bottom clamp on all CVBS/Y and RGB inputs, average clamp on C inputs
 - SVHS switch on C VCR output
 - Bandwidth: 15 MHz
 - Crosstalk: 50 dB minimum
- Audio section
 - 4 Stereo inputs, 3 stereo outputs
 - 1 mono-sound output
 - Stereo-to-mono sound capability
 - 0/6/9 dB selectable gain on one stereo input
 - Full range volume control with soft control
 - Audio muting on all outputs



Description

The STV6412B is a highly integrated I²C bus-controlled audio and video switch matrix, optimized for use in digital set-top box applications. It provides all the audio and video routings required in a full two-SCART set-top box design.

In an LQFP64 (14 × 14 × 1.4 mm) package, the STV6412B is compatible with the STV6412A.

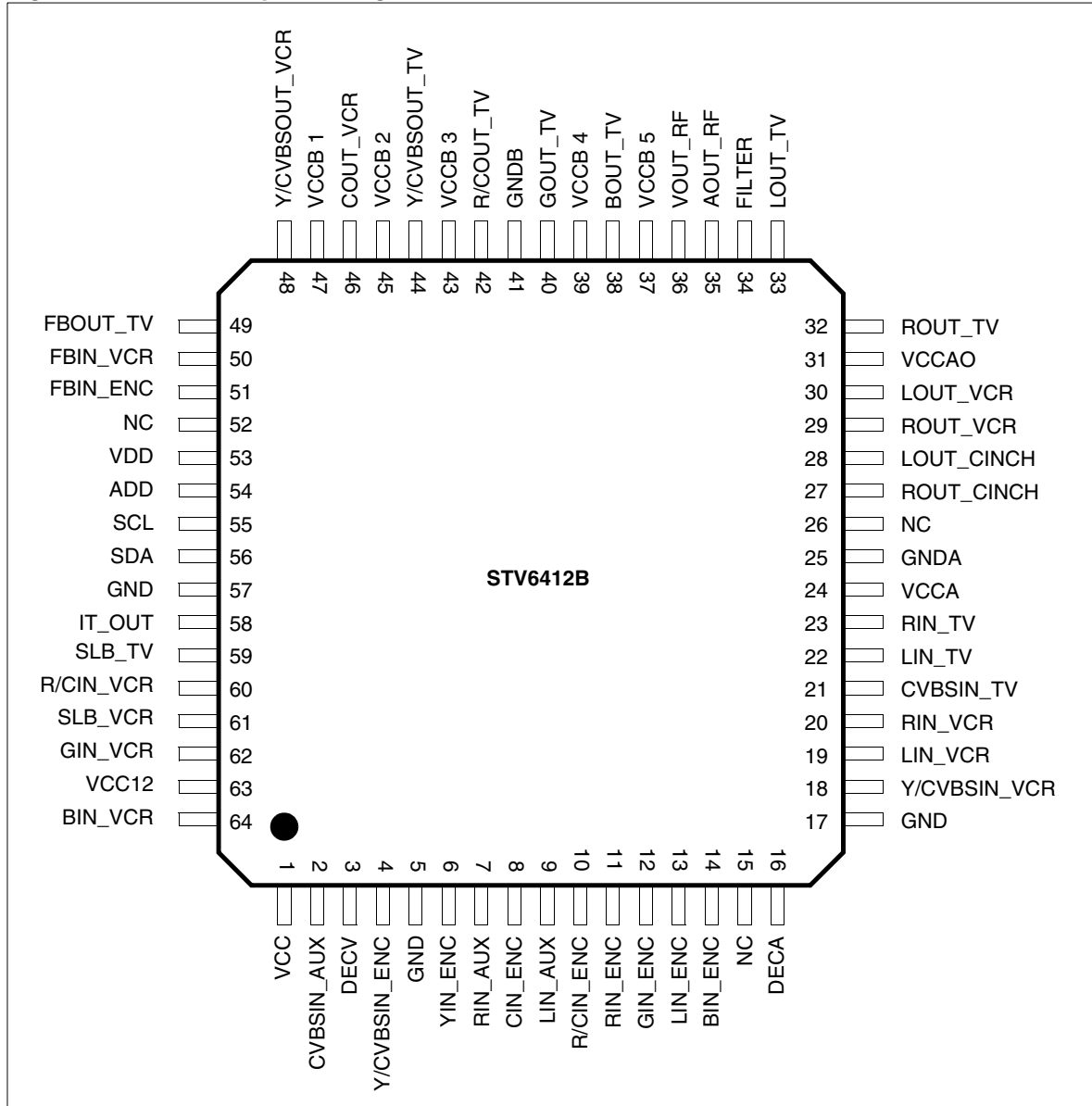
Table 1: Device summary

Order code	Packaging
STV6412BD	Tray
STV6412BDT	Tape and reel

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1 General information

Figure 1. STV6412B pinout diagram



1.1 I/O pin description

Table 1. I/O pin description

Pin No.	Symbol	Description
1	VCC	+5 V supply
2	CVBSIN_AUX	CVBS input from auxiliary
3	DECV	Video decoupling capacitor
4	Y/CVBSIN_ENC	Y/CVBS input from encoder
5	GND	Ground
6	YIN_ENC	Y input from encoder
7	RIN_AUX	Audio right input from auxiliary
8	CIN_ENC	Chroma input from encoder
9	LIN_AUX	Audio left input from auxiliary
10	R/CIN_ENC	Red/Chroma input from encoder
11	RIN_ENC	Audio right input from encoder
12	GIN_ENC	Green input from encoder
13	LIN_ENC	Audio left input from encoder
14	BIN_ENC	Blue input from encoder
15	NC	Not connected
16	DECA	Audio decoupling capacitor
17	GND	Ground
18	Y/CVBSIN_VCR	Y/CVBS input from VCR SCART
19	LIN_VCR	Audio left input from VCR SCART
20	RIN_VCR	Audio right input from VCR SCART
21	CVBSIN_TV	CVBS input from TV SCART
22	LIN_TV	Audio left input from TV SCART
23	RIN_TV	Audio right input from TV SCART
24	VCCA (see Figure 2)	9V audio supply voltage output if VCCAO is used as 12V supply voltage input or 9V audio supply voltage input, VCCAO must be used as 9V supply voltage input
25	GNDA	Audio ground
26	NC	Not connected
27	ROUT_CINCH	Audio right output to CINCH
28	LOUT_CINCH	Audio left output to CINCH
29	ROUT_VCR	Audio right output to VCR SCART
30	LOUT_VCR	Audio left output to VCR SCART

Table 1. I/O pin description (continued)

Pin No.	Symbol	Description
31	VCCAO (see Figure 2)	12V supply voltage input, VCCA is regulated 9V output for decoupling or 9V supply voltage input, VCCA must be used as 9V supply voltage input
32	ROUT_TV	Audio right output to TV SCART
33	LOUT_TV	Audio left output to TV SCART
34	FILTER	Chroma trap filter
35	AOUT_RF	Audio (L+R) output to RF modulator
36	VOOUT_RF	CVBS video output to RF modulator
37	VCCB5	Video output buffer supply pin
38	BOUT_TV	Blue output to TV SCART
39	VCCB4	Video output buffer supply pin
40	GOUT_TV	Green output to TV SCART
41	GNDB	Video buffer ground
42	R/COOUT_TV	Red/Chroma output to TV SCART
43	VCCB3	Video output buffer supply pin
44	Y/CVBSOUT_TV	Y/CVBS output to TV SCART
45	VCCB2	Video output buffer supply pin
46	COOUT_VCR	Chroma output to VCR SCART
47	VCCB1	Video output buffer supply pin
48	Y/CVBSOUT_VCR	Y/CVBS output to VCR SCART
49	FBOOUT_TV	Fast blanking output to TV SCART
50	FBIN_VCR	Fast blanking input from VCR SCART
51	FBIN_ENC	Fast blanking input from encoder
52	NC	Not connected
53	VDD	+5 V I ² C supply
54	ADD	I ² C address selection
55	SCL	I ² C bus clock
56	SDA	I ² C bus data
57	GND	Ground digital
58	IT_OUT	Interrupt output
59	SLB_TV	Slow blanking input/output from TV SCART
60	R/CIN_VCR	Red input (or C input) from VCR SCART
61	SLB_VCR	Slow blanking input/output from VCR SCART
62	GIN_VCR	Green Input from VCR SCART

Table 1. I/O pin description (continued)

Pin No.	Symbol	Description
63	VCC12	+12 V supply
64	BIN_VCR	Blue input from VCR SCART

Figure 2. Power supply configuration

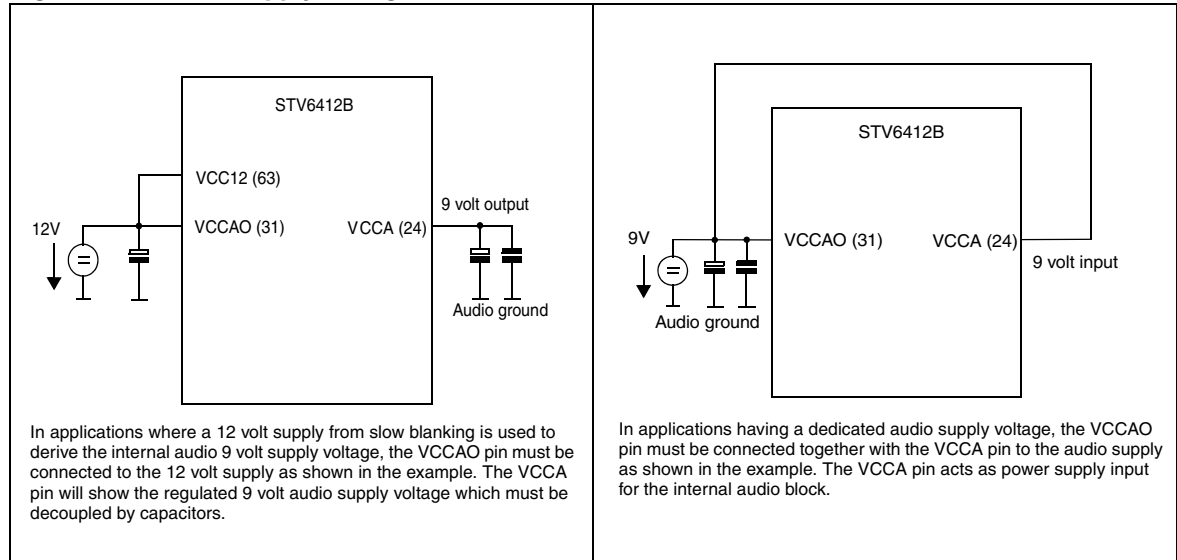


Figure 3. STV6412B block diagram

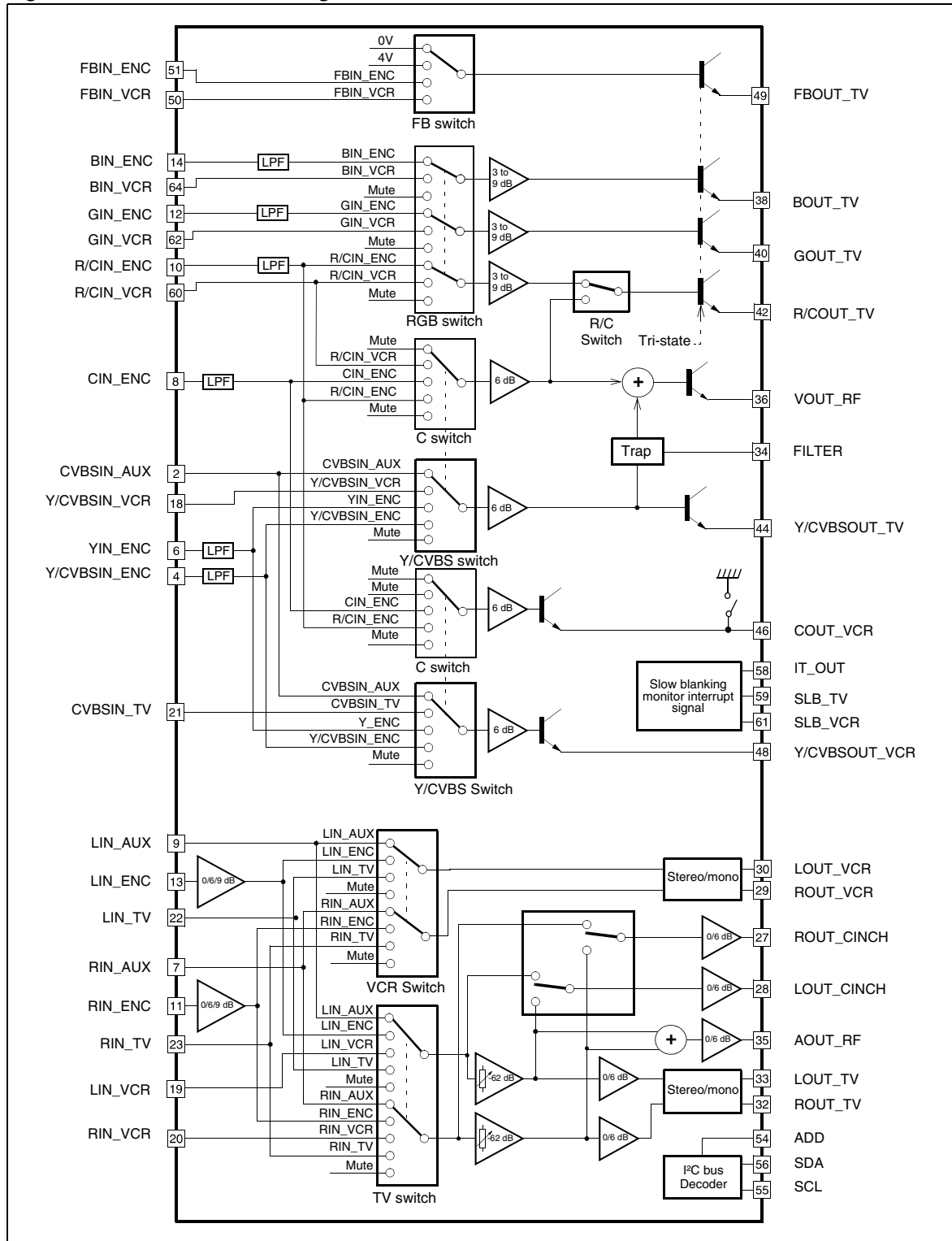
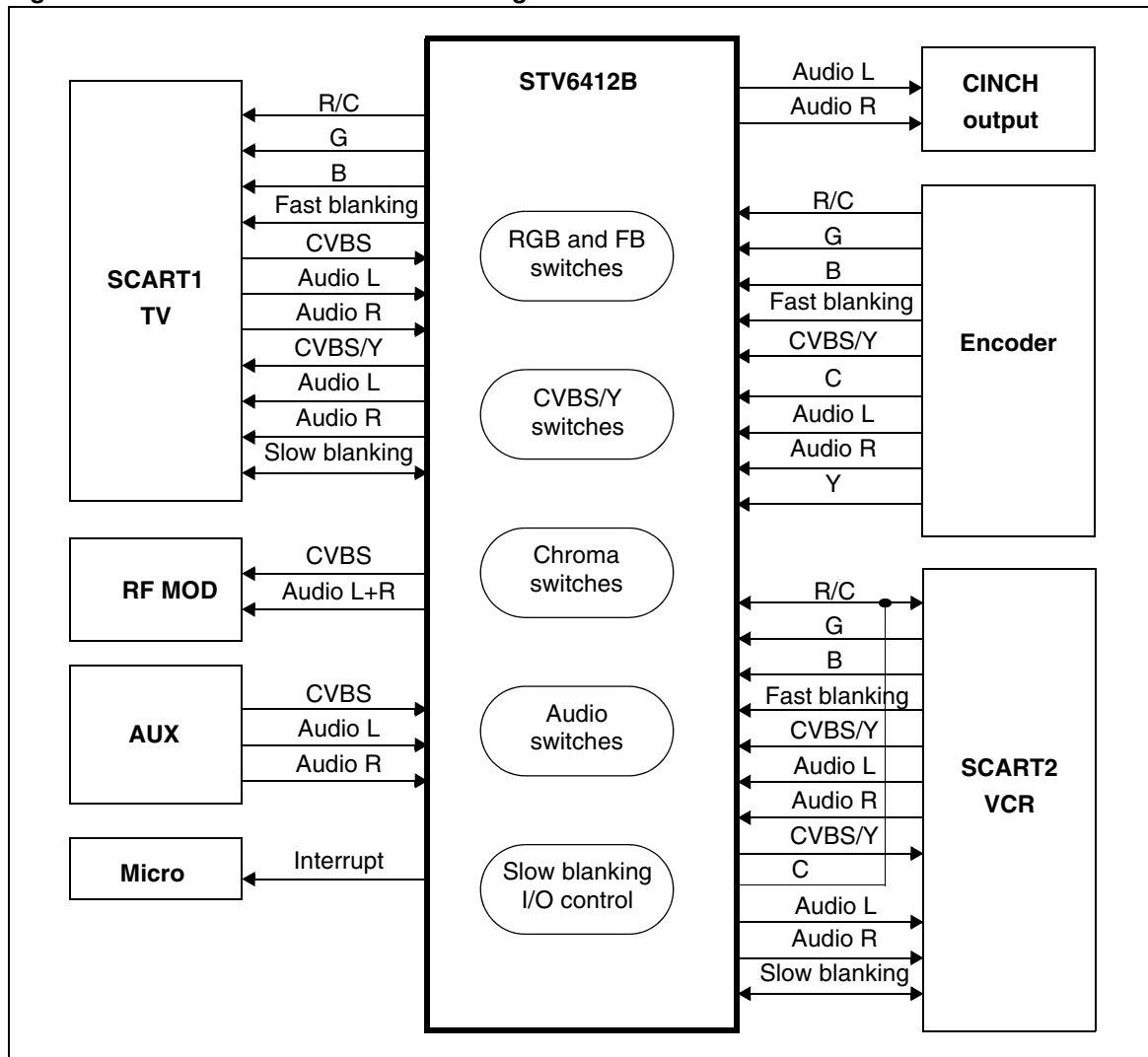


Figure 4. STV6412B functional block diagram



2 Electrical characteristics

Table 2: Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{CC12}	Supply voltage for slow blanking sections		13.2	V
V_{CCAO}	Supply voltage for audio drivers		13.2	V
V_{CCA}	Supply voltage for internal digital audio parts		10.0	V
V_{DD}	Supply voltage for digital parts		6.0	V
V_{CC}, V_{CCB1}	Supply voltage for video sections		6.0	V
V_{IN}	Input voltage at pin (in reference to GND)	Audio pins Video pins Bus pins Slow blanking pins	0, V_{CCA} 0, V_{CC} or V_{CCB1} 0, 5.5 0, V_{CC12}	V
V_{ESD}	Maximum ESD Voltage allowed (human body model: 100 pF capacitor discharged through 1.5 k Ω serial resistor)		± 4	kV

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Maximum junction-to-ambient thermal resistance	48	$^{\circ}\text{C}/\text{W}$
T_{STG}	Storage temperature	-20 to +150	$^{\circ}\text{C}$
T_{OPER}	Operating free air temperature range	0 to +70	$^{\circ}\text{C}$
T_j	Maximum junction temperature	150	$^{\circ}\text{C}$

2.1 Latch up

At an ambient temperature of 25 $^{\circ}\text{C}$, all pins meet the following specifications:

$I_{\text{trigger}} = 200 \text{ mA}$ or $I_{\text{trigger}} = -200 \text{ mA}$.

2.2 Recommended operating conditions

$T_{\text{AMB}} = 25 \text{ }^{\circ}\text{C}$, $V_{\text{CCAO}} = 12 \text{ V}$, $V_{\text{CC}} = 5 \text{ V}$, $V_{\text{CC12}} = 12 \text{ V}$, $V_{\text{DD}} = 5 \text{ V}$,
 $R_{\text{LOUTA}} = 10 \text{ k}\Omega$, $R_{\text{LOUTV}} = 150 \text{ }\Omega$, unless otherwise specified.

Table 4: Recommended operating conditions

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Supply voltages						
V_{DD}	Digital supply voltage		4.75	5	5.25	V
V_{CCAO}	Audio operating supply voltage	- Decoupling capacitor on V_{CCA} - Connected to V_{CCA}	11.2 8.5	12 9	12.8 9.5	V
V_{CC}	Video operating supply voltage		4.75	5	5.25	V

Table 4: Recommended operating conditions (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{CC12}	Slow blanking control supply voltage		11.2	12	12.8	V
Active mode (all channels ON)						
I_{DD}	Digital supply current	$V_{DD} = 5\text{ V}$		6	10	mA
I_{CCA}	Audio supply current	$V_{CCA0} = 12\text{ V}$, no load		8	15	mA
I_{CCV}	Total video supply current ($V_{CC} + V_{CCB1} + V_{CCB2} + V_{CCB3} + V_{CCB4} + V_{CCB5}$)	$V_{CC} = 5\text{ V}$, no load, LPF OFF $V_{CC} = 5\text{ V}$, no load, LPF ON $V_{CC} = 5\text{ V}$, with load, LPF OFF $V_{CC} = 5\text{ V}$, with load, LPF ON		35 50 48 63	45 65 62 80	mA
I_{CC12}	12 V supply current	$V_{CC12} = 12\text{ V}$ SLB input mode SLB output mode, no load		0 3	1 4	mA
Standby mode (all channels OFF + LPF OFF)						
I_{DD}	Digital supply current	$V_{DD} = 5\text{ V}$		6	10	mA
I_{CCAstd}	Audio supply current	$V_{CCA0} = 12\text{ V}$, no load		3		mA
I_{CCVstd}	Total video supply current	$V_{CC} = 5\text{ V}$		1		mA

2.3 Audio section characteristics

$T_{AMB} = 25^\circ\text{C}$, $V_{CCA0} = 12\text{ V}$, $V_{CC} = 5\text{ V}$, $V_{CC12} = 12\text{ V}$, $V_{DD} = 5\text{ V}$,
 $R_{GA} = 600\ \Omega$, $R_{LOUTA} = 10\text{ k}\Omega$, $R_{GV} = 50\ \Omega$, $R_{LOUTV} = 150\ \Omega$, unless otherwise specified.

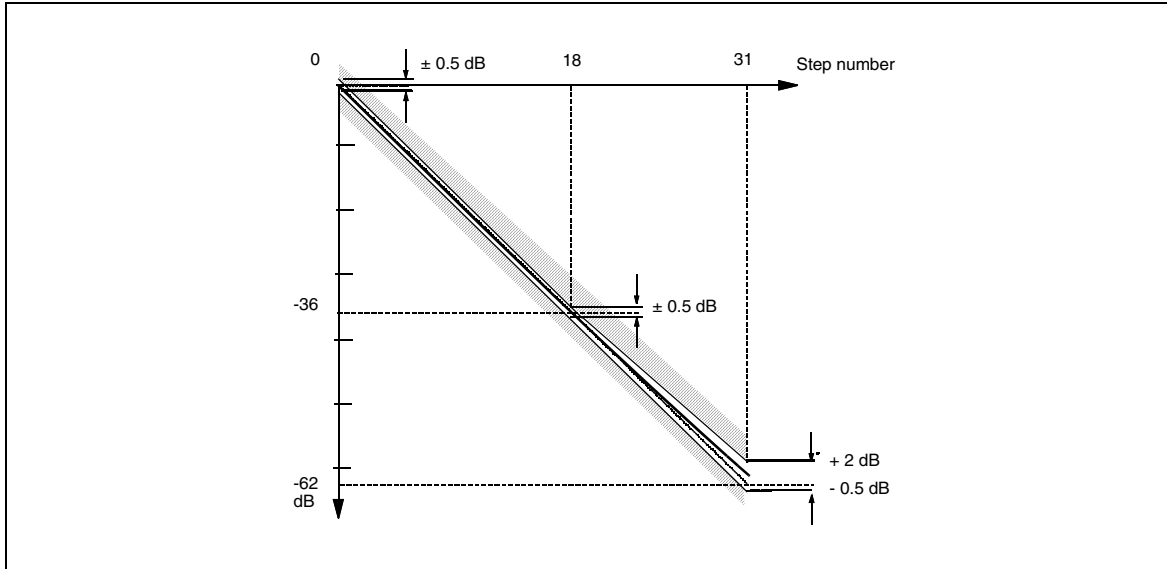
Table 5. Audio section characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
SVR100	Supply voltage rejection	$V_{RIPPLE} = 500\text{ mV}_{RMS}$ at 100 Hz, Gain = 0 dB, DECA filter cap = 47 μF DECA filter cap = 220 μF	60	70 80		dB
SVR1K	Supply voltage rejection	$V_{RIPPLE} = 500\text{ mV}_{RMS}$ at 1 kHz, Gain = 0 dB	70	80		dB
V_{INDC}	Input DC level	$V_{CCA} = 9\text{ V}$		3.2		V
V_{INAC}	Input signal amplitude				2	V_{RMS}
R_{IN}	Input resistance		30	50		$\text{k}\Omega$
$R_{INmatch}$	Input resistance matching			± 2	± 10	%
F_{RANGE}	Bandwidth	-3 dB, 0.5 V_{RMS} , $R_{LOAD} = 10\text{ k}\Omega$, Gain = 0 dB	50			kHz
Flatness	Spread of gain in audio band	-0.5 V_{RMS} , 20 Hz to 20 kHz, Gain = 0 dB			0.5	dB

Table 5. Audio section characteristics (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
CS	Channel separation, from audio inputs Between L & R of TV outputs	$V_{IN} = 0.5 V_{RMS}$ at 1 kHz, on 1 input, $R_{LOAD} = 10\text{ k}\Omega$, Gain = 0 dB	80 70	90 74		dB
Ci	Channel isolation from video inputs	$V_{IN} = 1 V_{pp}$ at 15 kHz, on one point		85		dB
V_{OUT}	Output DC level	$V_{CCA} = 9\text{ V}$		$V_{CCA}/2$		V
V_{OFF}	DC offset change	Switching between inputs		1	± 15	mV
R_{OUT}	Output resistance			60	120	Ω
PHD	Phase difference	$f = 1\text{ kHz}$, $1 V_{RMS}$ input on each input channel			3	$^{\circ}$ deg.
ASN	S/N ratio	$f = 1\text{ kHz}$, $1 V_{RMS}$ input (Gain = 0 dB) weighted CCIR 468-4 quasi peak	75	85		dB
eNI	Equivalent RMS input voltage noise	BW = 20 Hz to 20 kHz flat, Gain = 0 dB		5		μV
G0	0 dB gain	$0.5 V_{RMS}$, $R_{LOAD} = 10\text{ k}\Omega$, Gain = 0 dB	-0.5		+0.5	dB
G_{STEP}	Gain step	-62 dB to +6 dB (see Figure 5)		2		dB
G_{MATCH1}	Gain matching between different inputs of one output	$V_{IN} = 0.5 V_{RMS}$, 1 kHz, Gain = 0 dB	-0.5		0.5	dB
G_{MATCH2}	Gain matching between left/right outputs of one input channel	$V_{IN} = 0.5 V_{RMS}$, 1 kHz, Gain = 0 dB	-0.5		0.5	dB
THD0 THD6 THD9	Total harmonic distortion ENC Input at 0 dB ENC Input at 6 dB ENC Input at 9 dB	$V_{OUT} = 0.5 V_{RMS}$, 1 kHz, LPF @ 80 kHz		0.01 0.01 0.01	0.1 0.1 0.1	% % %
V_{CL}	Output clipping level	THD = 0.2%, 1 kHz	2.1	2.3		V_{RMS}
R_L	Output load resistance	$V_{IN} = 1 V_{RMS}$, THD = 0.3%, Gain = 0 dB	2	2.25		$\text{k}\Omega$
Mute	Mute suppression	$V_{IN} = 0.5 V_{RMS}$, on one point	-90			dB

Figure 5. Volume control characteristics



2.4 Video section characteristics

$T_{AMB} = 25\text{ }^{\circ}\text{C}$, $V_{CCAO} = 12\text{ V}$, $V_{CC} = 5\text{ V}$, $V_{CC12} = 12\text{ V}$, $V_{DD} = 5\text{ V}$

Table 6. Video section characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Units
V_{DCIN}	DC input level	Bottom sync pulse		2		V
I_{CLAMP}	Clamping current	at $V_{DCIN} - 400\text{ mV}$	1	2		mA
I_{LEAK}	Input leakage current	$V_{IN} = V_{DCIN} + 1\text{ V}$		1	10	μA
C_{IN}	Input capacitance			2		pF
V_{IN}	Max input signal	$V_{CC} = 5\text{ V}$			1.5	V_{PP}
DYN	Dynamic output signal	$V_{CC} = 5\text{ V}$			3	V_{PP}
BW	Bandwidth at -3 dB without LPF Y/CVBS RGB Y/C mixer (on VOUT-RF)	$V_{IN} = 1\text{ V}_{PP}$ $V_{IN} = 1\text{ V}_{PP}$ $V_{IN} = 1\text{ V}_{PP}$, $V_{INC} = \text{muted}$	10 10 8	15 15 10		MHz MHz MHz
Flatness	Spread of gain in video band (15 kHz to 5 MHz) Y/CVBS RGB Y/C Mixer (on VOUT-RF)	$V_{IN} = 1\text{ V}_{PP}$ $V_{IN} = 1\text{ V}_{PP}$ $V_{IN} = 1\text{ V}_{PP}$, $V_{INC} = \text{muted}$			± 0.5 ± 0.5 ± 1.5	dB dB dB
BW LPF	Low pass filter bandwidth at -3 dB	$V_{IN} = 1\text{ V}_{PP}$, $CL = 10\text{ pF}$		7.5		MHz
ATT	Low pass filter attenuation	27 MHz		-47	-36	dB
CTi	Crosstalk isolation between Input channel	$V_{IN} = 1\text{ V}_{PP}$ at $f = 4.43\text{ MHz}$, on one point		60		dB

Table 6. Video section characteristics (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Units
C _{To}	Crosstalk isolation between output channel	V _{IN} = 1 V _{PP} at f = 4.43 MHz, on one point, R _{LOAD} = 150 Ω		50		dB
R _{OUT}	Output resistance			5	10	Ω
G _{RGB}	Gain at RGB outputs	V _{IN} = 1 V _{PP} , Gain set to 6 dB	5.5	6	6.5	dB
G _{RGBM}	Gain matching between R, G, B	V _{IN} = 1 V _{PP} , Gain set to 6 dB	-0.3	0	0.3	dB
G _{RGBSTEP}	Step of gain	3 dB to 6 dB	0.75	1	1.25	dB
G _{YCVBS}	Gain on Y, CVBS channels	V _{IN} = 1 V _{PP}	5.5	6	6.5	dB
G _{YCVBSM}	Gain matching between Y, CVBS inputs	V _{IN} = 1 V _{PP}	-0.5	0	0.5	dB
DC _{OUT}	DC output voltage	Bottom sync pulse		0.6		V
DC _{OUT RF}	RF output voltage	Bottom sync pulse		1		V
DPHI	Differential phase	V _{IN} = 1 V _{PP} at f = 4.43 MHz		1	5	° deg.
DG	Differential gain	V _{IN} = 1 V _{PP} at f = 4.43 MHz		1	5	%
Mute	Mute suppression	V _{IN} = 1 V _{PP} at f = 5 MHz on one point	-55			dB
LNL	Luminance non-linearity			0.3	3	%
VSN	Video S/N ratio	Refer to Note 1	65			dB

Note: 1 $S/N = 20 \log (V_{OUT \text{ Black to White}} = 0.7 V_{PP} / V_{Noise} (mV_{RMS}) \text{ weighted CCIR 567})$.

2.5 Chroma section characteristics

T_{AMB} = 25 °C, V_{CCAO} = 12 V, V_{CC} = 5 V, V_{CC12} = 12 V, V_{DD} = 5 V
R_{GA} = 600 Ω, R_{LOUTA} = 10 kΩ, R_{GV} = 50 Ω, R_{LOUTV} = 150 Ω, unless otherwise specified.

Table 7. Chroma section characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Units
V _{DCIN}	DC input level			3		V
R _{IN}	Input resistance		30	50		kΩ
C _{IN}	Input capacitance			2		pF
V _{IN}	Max input signal				1.5	V _{PP}
DYN	Dynamic output signal				3	V _{PP}
DC _{OUT}	DC output VCR voltage			2.2		V
CBW	Chroma bandwidth	C _{IN} = 1 V _{PP} at -3 db	10	15		MHz
CTi	Crosstalk isolation between Input channel	V _{IN} = 1 V _{PP} at f = 4.43 MHz, on one input		55		dB

Table 7. Chroma section characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Units
C _{TO}	Crosstalk isolation between output channel	V _{IN} = 1 V _{PP} at f = 4.43 MHz, on one input, R _{LOAD} = 150 Ω		50		dB
R _{OUT}	Output resistance			5	10	Ω
G _{OUTC}	Gain at OUTC	V _{IN} = 1 V _{PP}	5.5	6	6.5	dB
G _{CM}	Gain matching between C inputs	V _{IN} = 1 V _{PP}	-0.5	0	0.5	dB
Mute	Mute suppression	V _{IN} = 1 V _{PP} at f = 4.43 MHz, on one input	-55			dB
C _{TOydel}	Chroma to luma delay, source Y/C	Pin other than VOUT_RF, V _{PP} @ 4.43 MHz,			20	ns
C _{TOydel}	Chroma to luma delay, source Y/C	Pin VOUT_RF			20	ns
Z _{COU_T_VCR}	Output impedance when switched to ground	2.7V applied to COU _T _VCR with series 75 Ω Resistor		2		Ω

2.6 Blanking section

T_{AMB} = 25 °C, V_{CCA0} = 12 V, V_{CC} = 5 V, V_{CC12} = 12 V, V_{DD} = 5 V,
R_{LOU_TA} = 10 kΩ, R_{LOU_TV} = 150 Ω, unless otherwise specified.

Table 8. Blanking section

Symbol	Parameter	Test conditions	Min	Typ	Max	Units
Input mode						
SLBlow	Input low level threshold		2.5	3.25	4	V
SLBhigh	Input high level threshold		7.5	8.25	9	V
I _{IN}	Input current			50	100	μA
Output mode						
SLBlow	Output low level (int. TV)		0	0.02	1.5	V
SLBmed	Output medium level (ext. 16/9)		5	5.75	6.5	V
SLBhigh	Output high level (ext. 4/3)		10	11	12	V

2.6.1 Fast blanking section

Table 9. Fast blanking section

Symbol	Parameter	Test conditions	Min	Typ	Max	Units
Input mode						
FBlow/high	Input low/high level threshold		0.4	0.7	0.9	V
I _{IN}	Input current			2	10	μA
Output mode						

Table 9. Fast blanking section (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Units
FB _{LOW}	Output low level	R _{LOAD} = 150 Ω			0.5	V
FB _{HIGH}	Output high level		3.0	3.4	3.8	V
FB _{DEL}	Fast blanking RGB delay	At 50% on digital RGB transients, at 2 V on FB rise transient, at 1 V on FB fall, C _{LOAD} = 10pF maximum		15		ns
FB _{TRANS}	FB transitions at FB output Rise Time Fall Time	C _{LOAD} = 10 pF maximum between 10% and 90% between 90% and 10%		10 10		ns ns

2.6.2 Interrupt output

Refer to [Note 1](#)

Table 10. Interrupt output

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Units
IT-Leak	High level leakage	External pull-up to 5 V			10	μA
IT-Low	Output low level (active)	I _{IN} = 0 mA I _{IN} = 1 mA			0.3 0.7	V V

2.6.3 Address selection input

Table 11. Address selection input

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Units
ADDsel_L	Address selection low level			0	0.2	V
ADDsel_H	Address selection high level		2.5		V _{DD}	V
I _{LEAK}	Leakage current				10	μA

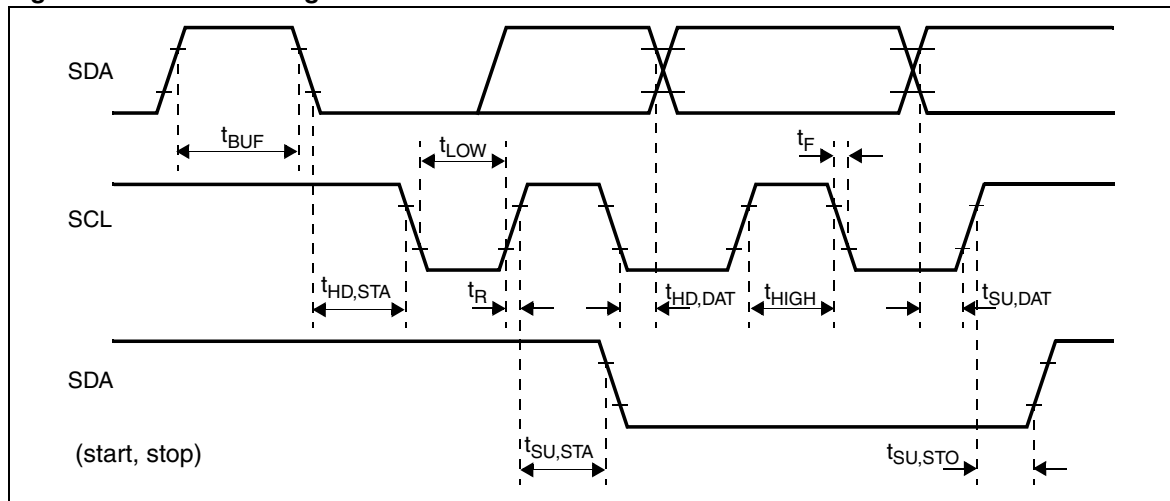
Note: 1 The interrupt is forced low when a change is detected on slow blanking inputs. It can be used in standby mode to wake up the microprocessor. It is released when the I²C bus register is read.

2.7 I²C bus characteristics

$T_{AMB} = 25^{\circ}\text{C}$, $V_{CCAO} = 12\text{ V}$, $V_{CC} = 5\text{ V}$, $V_{CC12} = 12\text{ V}$, $V_{DD} = 5\text{ V}$,
 $R_{LOUTA} = 10\text{ k}\Omega$, $R_{LOUTV} = 150\ \Omega$, unless otherwise specified.

Table 12. I²C bus characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Units
SCL						
V_{IL}	Low level input voltage		-0.3		1.5	V
V_{IH}	High level input voltage		2.3		5.5	V
I_{LI}	Input leakage current	$V_{IN} = 0\text{ to }5.5\text{ V}$	-10	0	10	μA
f_{SCL}	Clock frequency				400	kHz
t_R	Input rise time	1.5 V to 3 V			1	μs
t_F	Input fall time	1.5 V to 3 V			300	ns
C_I	Input capacitance				10	pF
SDA						
V_{IL}	Low level input voltage		-0.3		1.5	V
V_{IH}	High level input voltage		2.3		5.5	V
I_{LI}	Input leakage current	$V_{IN} = 0\text{ to }5.5\text{ V}$	-10	0	10	μA
C_I	Input capacitance				10	pF
t_R	Input rise time	1.5 V to 3 V			1	μs
t_F	Input fall time	3 V to 1.5 V			300	ns
V_{OL}	Low level output voltage	$I_{OL} = 3\text{ mA}$			0.4	V
t_F	Output fall time	3 V to 1.5 V			250	ns
C_L	Load capacitance				400	pF
Timing: SCL frequency = 400 kHz						
t_{LOW}	Clock low period		1.3			μs
t_{HIGH}	Clock high period		0.6			μs
$t_{SU,DAT}$	Data setup time		100			ns
$t_{HD,DAT}$	Data hold time		0		340	ns
$t_{SU,STO}$	Setup time from clock high to stop		0.6			μs
t_{BUF}	Start setup time following a stop		1.3			μs
$t_{HD,STA}$	Start hold time		0.6			μs
$t_{SU,STA}$	Start setup time following clock low to high transition		0.6			μs

Figure 6. I²C bus timing

3 I²C bus selection

Data transfers follow the usual I²C format; that is, after the start condition (S), a 7-bit slave address is sent, followed by an eighth bit (W) that determines whether the data direction is Read (W=1) or Write (W=0). An 8-bit sub-address is sent to select a register, followed by an 8-bit data word to be included in the register. The IC's I²C bus decoder enables the automatic incrementation mode in write mode.

The circuit operates at clock frequencies of up to 400 kHz.

Table 13. String format

Write only mode (S = Start condition, P = Stop condition, A = Acknowledge)

S	SLAVE ADDRESS	0	A	SUB-ADDRESS	A	DATA	A	P
---	---------------	---	---	-------------	---	------	---	---

Table 14. Read only mode

S	SLAVE ADDRESS	1	A	DATA	A	P
---	---------------	---	---	------	---	---

Table 15. Slave address

Address	A6	A5	A4	A3	A2	A1	A0
Value	1	0	0	1	0	1	X

Table 16. Auto increment mode

S	SLAVE ADDRESS	0	A	SUB-ADDRESS	A	DATA0	A	DATA1	A	...	DATA _n	A	P
				Sub-address	Sub-address +1		Sub-address + N						

3.1 I²C bus addresses

Write address: 1001 01X0, read address: 1001 01X1

Address selection pin grounded: X = 0, write address = 94(hex), read address = 95(hex)

Address selection pin to supply: X = 1, write address = 96(hex), read address = 97(hex)

Table 17. Input signal summary (write mode)

Reg Addr (Hex)	Data							
	d7	d6	d5	d4	d3	d2	d1	d0
Audio								
00h	TV stereo mono	TV 0/6 dB	TV volume-62 dB to 0 dB - 2 dB steps				Soft volume mode	
01h	VCR stereo mono	Not used (see Note 1)	VCR audio switch control		CINCH audio gain	TV/CINCH audio switch control		

Table 17. Input signal summary (write mode) (continued)

Reg Addr (Hex)	Data							
	d7	d6	d5	d4	d3	d2	d1	d0
Video								
02h	VCR chroma muted	VCR video and chroma switch control			TV chroma muted	TV video and chroma switch control		
03h	RGB and FB tri-state	RGB gain			RGB switch control		Fast blanking mode/input selection	
Miscellaneous								
04h	IT enable	SLB mode	Low pass filter control	VCR-C output control		RF trap filter control	RF adder control	TV R or C output selection
05h	VCR slow blanking		TV slow blanking		ENC audio input gain 0/6/9 dB		VCR R/C sub clamp	ENC R/C sub clamp
STB-BY								
06h	RF outputs	TV outputs	CINCH outputs	VCR outputs	AUX inputs	TV inputs	VCR inputs	ENC inputs

Note: 1 Unused data must be set to "0".

Table 18. TV audio output

Reg Addr (Hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
00h	Soft volume change	1	X X	X X	X X	X X	X X	X X	X X	0 1	Active Disabled
	Level adjustment	5	X X	X X	0 1	0 1	0 1	0 1	0 1	X X	0 dB -62 dB (-2 dB/step)
	6 dB extra gain	1	X X	0 1	X X	X X	X X	X X	X X	X X	0 dB +6 dB
	TV stereo or mono mode	1	0 1	X X	X X	X X	X X	X X	X X	X X	0 = Stereo 1 = Mono

Table 19: Audio selection and VCR audio output

Reg Addr (Hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
01h	TV & CINCH audio output selection	3	X	X	X	X	X	0	0	0	Muted
			X	X	X	X	X	0	0	1	Encoder L/R selected
			X	X	X	X	X	0	1	0	VCR L/R selected
			X	X	X	X	X	0	1	1	AUX L/R selected
			X	X	X	X	X	1	0	0	TV L/R selected
			X	X	X	X	X	1	0	1	Not allowed
			X	X	X	X	X	1	1	0	Not allowed
	CINCH audio gain	1	X	X	X	X	0	X	X	X	0 dB
			X	X	X	X	1	X	X	X	Follow TV gain
	VCR audio output selection	2	X	X	0	0	X	X	X	X	Muted
			X	X	0	1	X	X	X	X	Encoder L/R selected
			X	X	1	0	X	X	X	X	TV L/R selected
	VCR stereo or mono mode	1	0	X	X	X	X	X	X	X	0 = Stereo
1			X	X	X	X	X	X	X	1 = Mono	

Table 20: TV and VCR selection

Reg Addr (Hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
02h	TV video output selection	3	X	X	X	X	X	0	0	0	Y/CVBS muted & chroma muted
			X	X	X	X	X	0	0	1	Y/CVBS_ENC & R/C_ENC
			X	X	X	X	X	0	1	0	Y_ENC & C_ENC
			X	X	X	X	X	0	1	1	Y/CVBS_VCR & R/C_VCR
02h	TV chroma output control	1	X	X	X	X	0	X	X	X	Chroma defined by d2d1d0
			X	X	X	X	1	X	X	X	Chroma force to mute
			X	0	0	0	X	X	X	X	Y/CVBS muted & chroma muted
			X	0	0	1	X	X	X	X	Y/CVBS_ENC & R/C_ENC
02h	VCR video output selection	3	X	0	1	0	X	X	X	X	Y_ENC & C_ENC
			X	0	1	1	X	X	X	X	CVBS_TV & chroma muted
			X	1	0	0	X	X	X	X	CVBS_AUX & chroma muted
			X	1	0	1	X	X	X	X	muted
02h	VCR chroma output control	1	0	X	X	X	X	X	X	X	Chroma defined by d6d5d4
			1	X	X	X	X	X	X	X	Chroma force to mute
			X	1	1	0	X	X	X	X	Not allowed
			X	1	1	1	X	X	X	X	Not allowed

Table 21: RGB and fast blanking outputs

Reg Addr (Hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
03h	Fast blanking control	2	X	X	X	X	X	X	0	0	FB forced to low level
			X	X	X	X	X	X	0	1	FB forced to high level
			X	X	X	X	X	X	1	0	FB from encoder
			X	X	X	X	X	X	1	1	FB from VCR
	RGB selection	2	X	X	X	X	0	0	X	X	Muted
			X	X	X	X	0	1	X	X	RGB_ENC selected
			X	X	X	X	1	0	X	X	RGB_VCR selected
	RGB gain	2	X	X	0	0	X	X	X	X	+6 dB gain
			X	X	0	1	X	X	X	X	+5 dB gain
			X	X	1	0	X	X	X	X	+4 dB gain
X			X	1	1	X	X	X	X	+3 dB gain	
RGB and fast blanking control	1	X	0	X	X	X	X	X	X	+0 dB extra gain	
		X	1	X	X	X	X	X	X	+3 dB for weak input signals	
RGB and fast blanking control	1	0	X	X	X	X	X	X	X	RGB and FB outputs high impedance state	
		1	X	X	X	X	X	X	X	RGB and FB outputs active	

Table 22: RF and miscellaneous control

Reg Addr (Hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
04h	R/C TV output selection	1	X	X	X	X	X	X	X	0	Red signal selected
			X	X	X	X	X	X	X	1	Chroma signal selected
	RF output: adder control and chroma sub-carrier filter selection	1	X	X	X	X	X	X	0	X	CVBS to RF output
			X	X	X	X	X	X	1	X	Y + C to RF output
	C_VCR output control	2	X	X	X	0	0	X	X	X	Grounded
			X	X	X	0	1	X	X	X	Tri-state Mode (High Impedance)
	Low pass filter control	1	X	X	0	X	X	X	X	X	Active
			X	X	1	X	X	X	X	X	LPF Enabled
Slow blanking mode	1	X	0	X	X	X	X	X	X	LPF Disabled	
		X	1	X	X	X	X	X	X	Normal Mode	
IT enable	1	0	X	X	X	X	X	X	X	SLB TV is driven by SLB VCR	
		1	X	X	X	X	X	X	X	No interrupt flag	
IT enable	1	0	X	X	X	X	X	X	X	IT enable	
		1	X	X	X	X	X	X	X	IT enable	

Table 23: Slow blanking and inputs control

Reg Addr (Hex)	Description	Bits	Data								Comments	
			d7	d6	d5	d4	d3	d2	d1	d0		
05h	Encoder R/C sub clamp	1	X X	X X	X X	X X	X X	X X	X X	X X	0 1	Bottom level clamp Average level clamp
	VCR R/C sub clamp	1	X X	X X	X X	X X	X X	X X	0 1	X X	X X	Bottom level clamp Average level clamp
	Encoder input level adjustment	2	X X X	X X X	X X X	X X X	0 0 1	0 1 0	X X X	X X X	X X X	0 dB for normal audio inputs +6 dB for weak audio inputs +9 dB for weak audio inputs
	Slow blanking TV SCART	2	X X X X	X X X X	0 0 1 1	0 1 0 1	X X X X	X X X X	X X X X	X X X X	X X X X	Input mode only Output < 2 V Output 16/9 format Output 4/3 format
	Slow blanking VCR SCART	2	0 0 1 1	0 1 0 1	X X X X	X X X X	X X X X	X X X X	X X X X	X X X X	X X X X	Input mode only Output < 2 V Output 16/9 format Output 4/3 format

Table 24: Standby modes

Reg Addr (Hex)	Description	Bits	Data								Comments	
			d7	d6	d5	d4	d3	d2	d1	d0		
06h	ENC inputs	1	X X	X X	X X	X X	X X	X X	X X	X X	0 1	Inputs active Inputs disabled
	VCR inputs	1	X X	X X	X X	X X	X X	X X	0 1	X X	X X	Inputs active Inputs disabled
	TV inputs	1	X X	X X	X X	X X	X X	0 1	X X	X X	X X	Inputs active Inputs disabled
	AUX inputs	1	X X	X X	X X	X X	0 1	X X	X X	X X	X X	Inputs active Inputs disabled
	VCR outputs	1	X X	X X	X X	0 1	X X	X X	X X	X X	X X	Audio & video outputs ON Audio & video outputs OFF
	CINCH outputs	1	X X	X X	0 1	X X	X X	X X	X X	X X	X X	Audio & video outputs on audio & video outputs OFF
	TV outputs	1	X X	0 1	X X	X X	X X	X X	X X	X X	X X	Audio & video outputs ON Audio & video outputs OFF
	RFmod outputs	1	0 1	X X	X X	X X	X X	X X	X X	X X	X X	Audio & video outputs ON Audio & video outputs OFF
	Full stop		1	1	1	1	1	1	1	1	1	Only I ² C bus and slow blanking detection parts are supplied.

Table 25: Output signals (read mode)

Reg Addr (Hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
	Slow blanking TV SCART	2	X	X	X	X	X	X	0	1	Input < 2 V Input 16/9 format Input 4/3 format
			X	X	X	X	X	X	1	0	
			X	X	X	X	X	X	1	1	
	Slow blanking VCR SCART	2	X	X	X	X	0	1	X	X	Input < 2 V Input 16/9 format Input 4/3 format
			X	X	X	X	1	0	X	X	
			X	X	X	X	1	1	X	X	
	Interrupt flag	1	X	X	X	0	X	X	X	X	No change since read One change has been detected (refer to Note 1)
			X	X	X	1	X	X	X	X	

Note: 1 The interrupt flag will be cleared when this register is read. To prepare for a new interrupt, a "1" must be re-written in the IT Enable bit (Reg. 04h, d7).

4 Input/output groups

Figure 7. Bottom clamped video inputs (pins 2, 4, 6, 12, 14, 18, 21, 62, and 64)

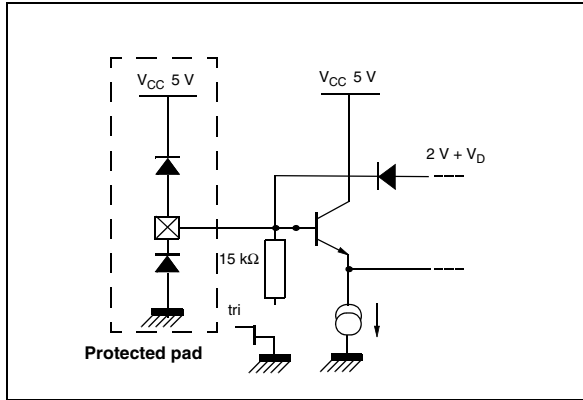
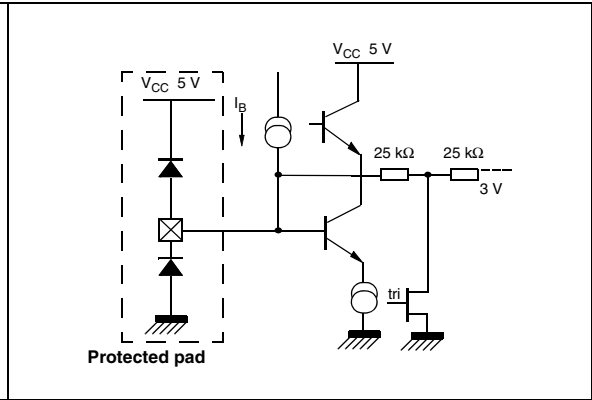


Figure 8. Average clamped video inputs (pin 8)



R/C clamped video inputs (pins 10 and 60)

R/C inputs may be configured either as a bottom clamped input or as an average clamped input. In either case, the simplified input schematic is very close to one of the graphics shown above

Figure 9. Fast blanking output (pin 49)

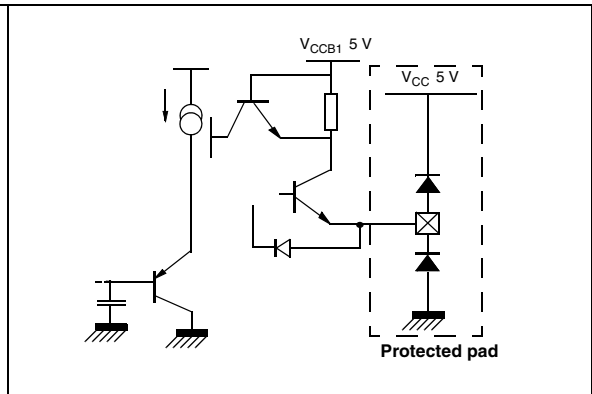


Figure 10. Fast blanking inputs (pins 50 and 51)

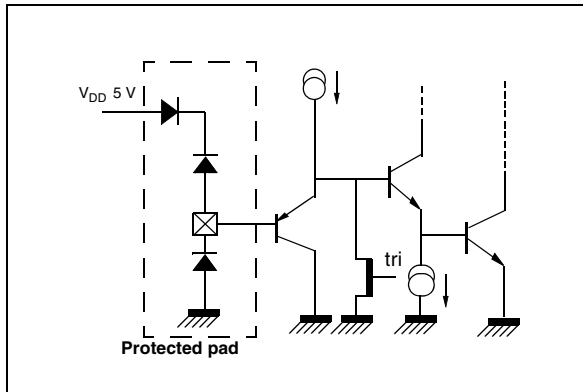


Figure 11. Video outputs (pins 38, 40, 42, 44, 46, and 48)

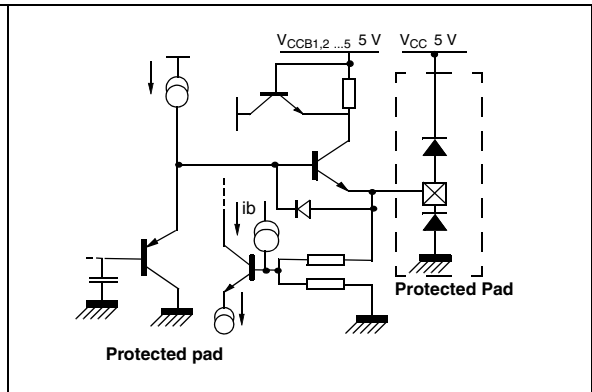


Figure 12. Audio inputs (pins 11, 13, 19, 20, 22, and 23)

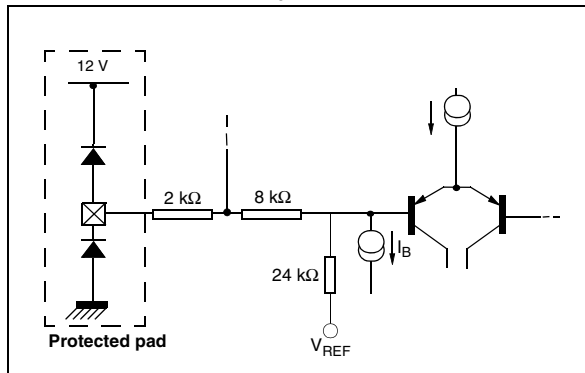


Figure 13. Audio outputs (pins 27, 28, 29, 30, 32 and 33)

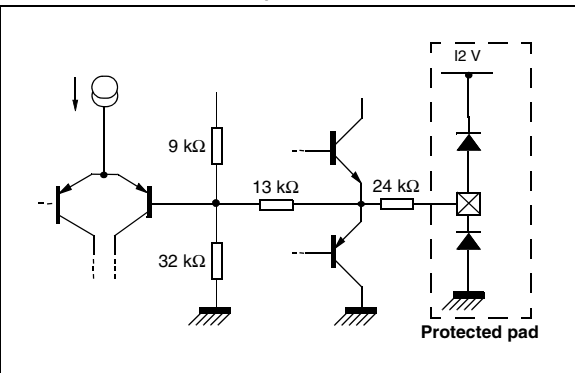


Figure 14. Slow blanking I/O (pins 59 and 61)

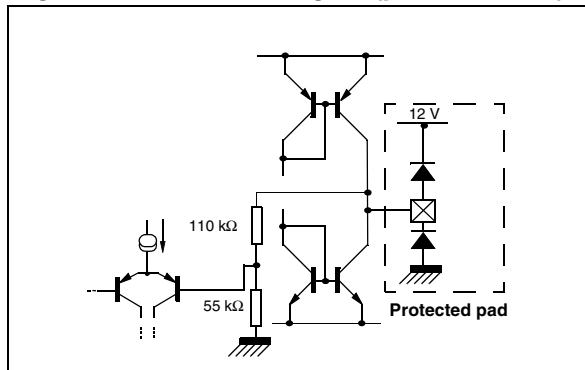


Figure 15. Interrupt output (pin 58)

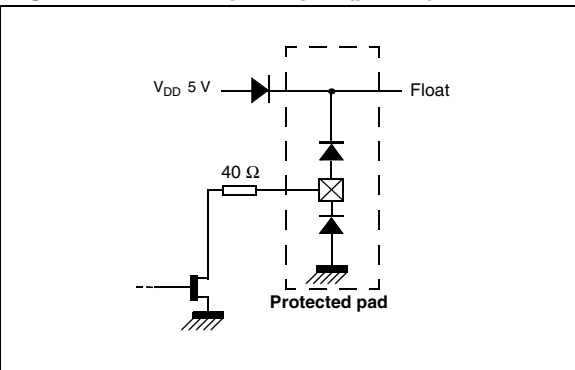


Figure 16. I²C bus (SDA) (pin 56)

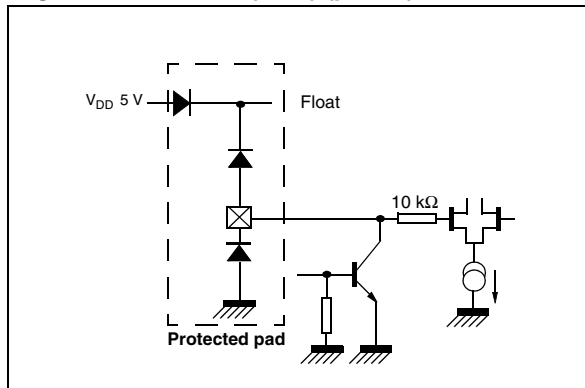


Figure 17. I²C bus (ADD) (pin 54)

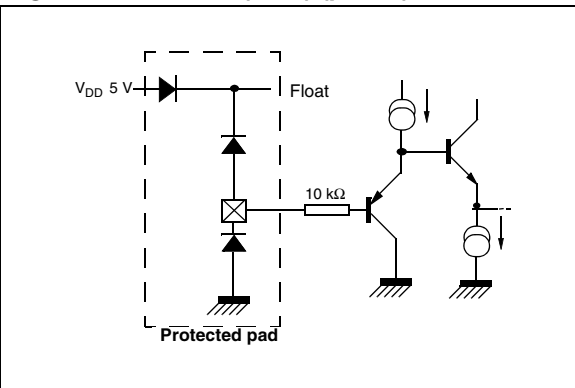


Figure 18. I²C bus (SCL) (pin 55)

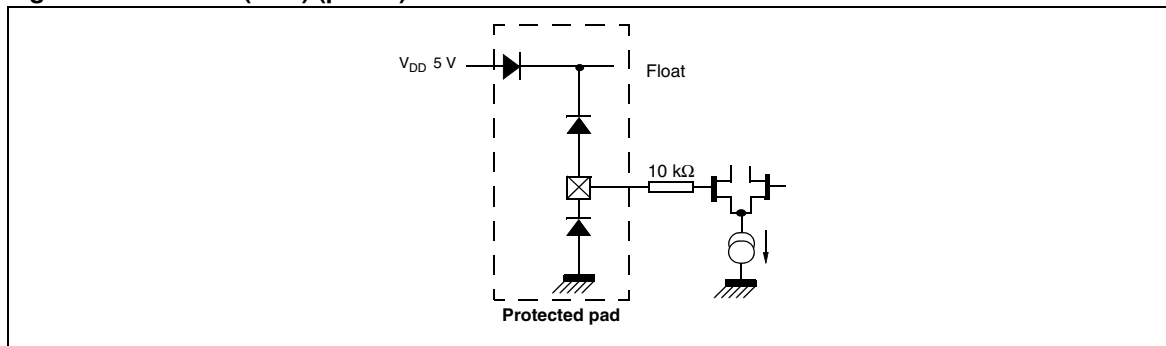
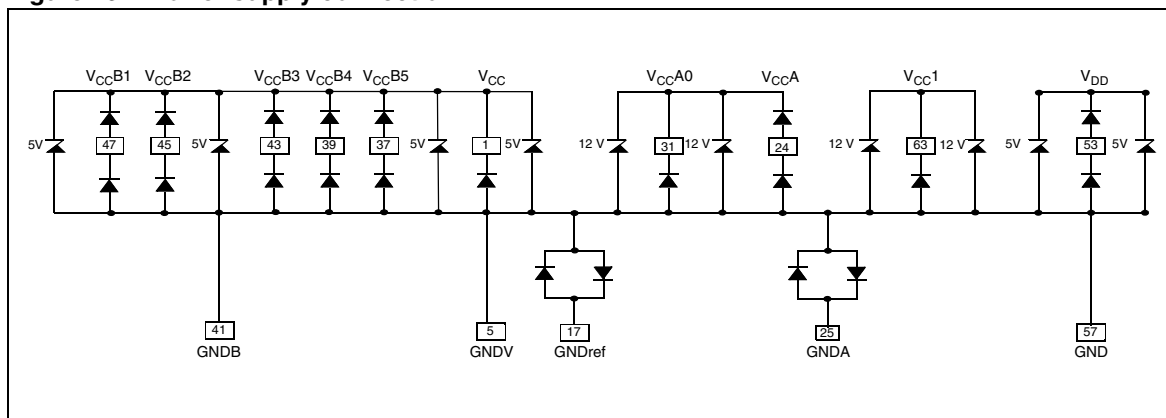


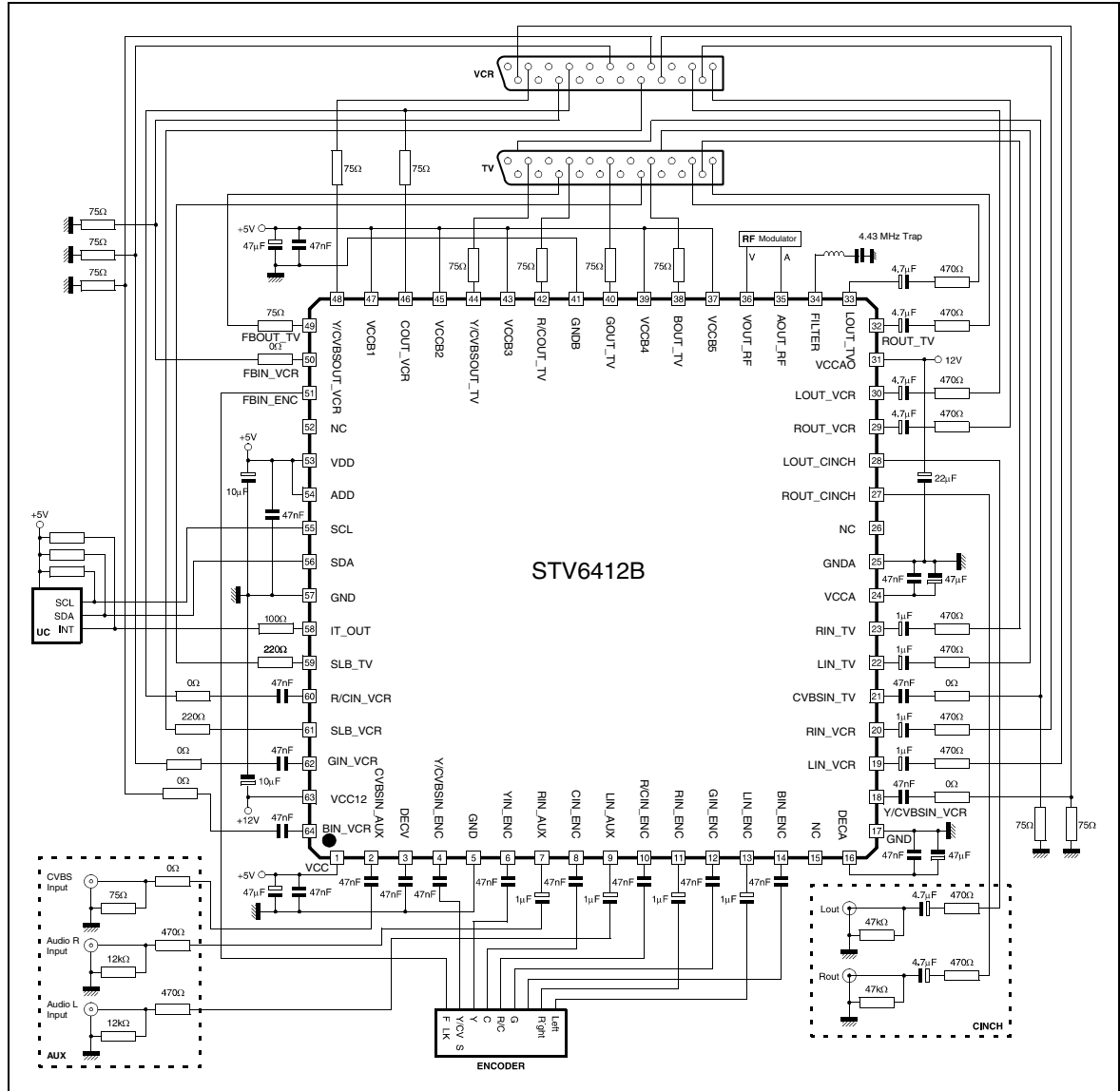
Figure 19. Power supply connection



5 Application diagram

Note: The application diagram presented here is an example only and is subject to change without notice. The real application diagram will depend on application conditions and constraints.

Figure 20. STV6412B application diagram



6 Package mechanical data

Figure 21. 64 pin, LQFP64 (low-profile quad flat package) 14 × 14 × 1.4 mm

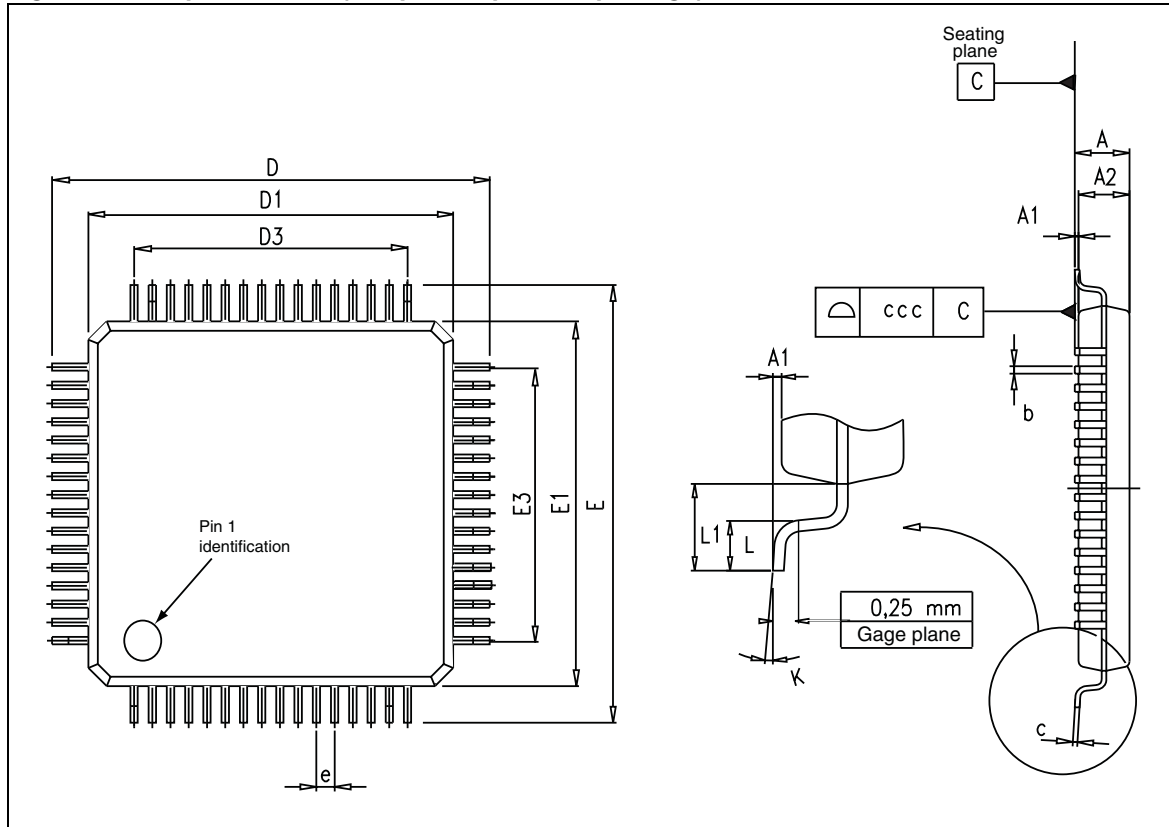


Table 26. LQFP64 package dimensions

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.30	0.37	0.45	0.0118	0.015	0.018
c	0.09		0.20	0.0035		0.0079
ccc			0.10			0.0039
D	15.80	16.00	16.20	0.622	0.630	0.638
D1	13.80	14.00	14.20	0.543	0.551	0.559
D3		12.00			0.472	
e		0.80			0.0315	
E	15.80	16.00	16.20	0.622	0.630	0.638

Table 26. LQFP64 package dimensions (continued)

E1	13.80	14.00	14.201	0.543	0.551	0.559
E3		12.00			0.472	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
Degrees						
k	0° minimum 3.5° typical 7° maximum					

6.1 Environment

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark.

ECOPACK specifications are available at www.st.com.

Revision history

Table 27. Document revision history

Date	Revision	Changes
28-Jul-2008	1	Initial Release.

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