

HD74LVC534

Octal D-type Flip Flops with 3-state Outputs

REJ03D0357-0400Z
 (Previous ADE-205-071B (Z))
 Rev.4.00
 Jul. 27, 2004

Description

The HD74LVC534 has eight edge trigger D type flip flops with three state outputs in a 20 pin package. Data at the D inputs meeting set up requirements are transferred to the Q outputs on positive going transitions of the clock input. When the latch enable goes low, data at the D inputs will be retained at the outputs until latch enable returns high again. When a high logic level is applied to the output control input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements. Low voltage and high-speed operation is suitable at the battery drive product (note type personal computer) and low power consumption extends the life of a battery for long time operation.

Features

- $V_{CC} = 2.0\text{ V to }5.5\text{ V}$
- All inputs $V_{IH}(\text{Max.}) = 5.5\text{ V} (@V_{CC} = 0\text{ V to }5.5\text{ V})$
- Typical V_{OL} ground bounce $< 0.8\text{ V} (@V_{CC} = 3.3\text{ V}, T_a = 25^\circ\text{C})$
- Typical V_{OH} undershoot $> 2.0\text{ V} (@V_{CC} = 3.3\text{ V}, T_a = 25^\circ\text{C})$
- High output current $\pm 24\text{ mA} (@V_{CC} = 3.0\text{ V to }5.5\text{ V})$
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LVC534FPEL	SOP-20 pin (JEITA)	FP-20DAV	FP	EL (2,000 pcs/reel)
HD74LVC534TELL	TSSOP-20 pin	TTP-20DAV	T	ELL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

Function Table

Inputs			Output \bar{Q}
\bar{G}	CK	D	
H	X	X	Z
L	↑	L	H
L	↑	H	L
L	L	X	Q_0

H: High level

L: Low level

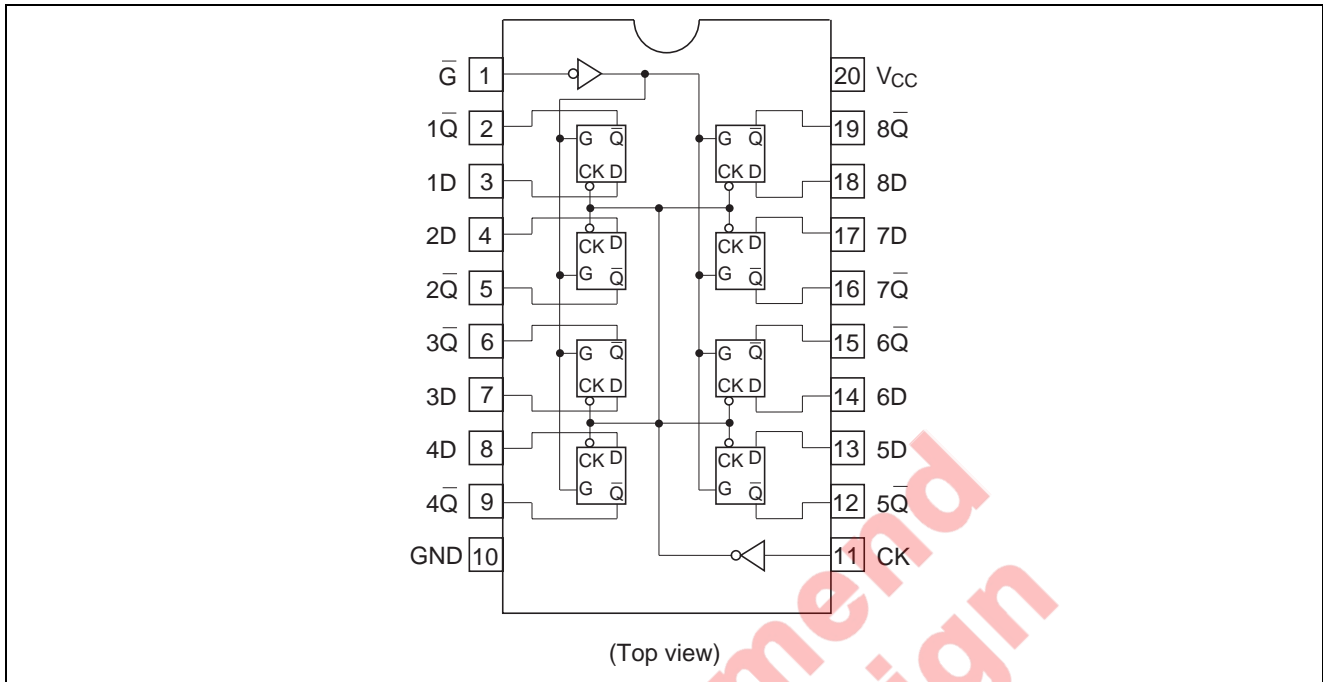
X: Immaterial

Z: High impedance

↑: Low to high transition

Q_0 : Level of \bar{Q} before the indicated steady input conditions were established.

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	-0.5 to 6.0	V	
Input diode current	I_{IK}	-50	mA	$V_I = -0.5$ V
Input voltage	V_I	-0.5 to 6.0	V	
Output diode current	I_{OK}	-50	mA	$V_O = -0.5$ V
		50		$V_O = V_{CC} + 0.5$ V
Output voltage	V_O	-0.5 to $V_{CC} + 0.5$	V	
Output current	I_O	± 50	mA	
V_{CC} , GND current / pin	I_{CC} or I_{GND}	100	mA	
Storage temperature	T_{stg}	-65 to +150	$^{\circ}$ C	

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	1.5 to 5.5	V	Data retention
		2.0 to 5.5		At operation
Input / output voltage	V_I	0 to 5.5	V	\bar{G} , CK, D
	V_O	0 to V_{CC}	V	\bar{Q}
Operating temperature	T_a	-40 to 85	°C	
Output current	I_{OH}	-12	mA	$V_{CC} = 2.7\text{ V}$
		-24 ^{*2}		$V_{CC} = 3.0\text{ V to }5.5\text{ V}$
	I_{OL}	12	mA	$V_{CC} = 2.7\text{ V}$
		24 ^{*2}		$V_{CC} = 3.0\text{ V to }5.5\text{ V}$
Input rise / fall time ^{*1}	t_r, t_f	10	ns/V	

- Notes: 1. This item guarantees maximum limit when one input switches.
 Waveform: Refer to test circuit of switching characteristics.
 2. Duty cycle ≤ 50%

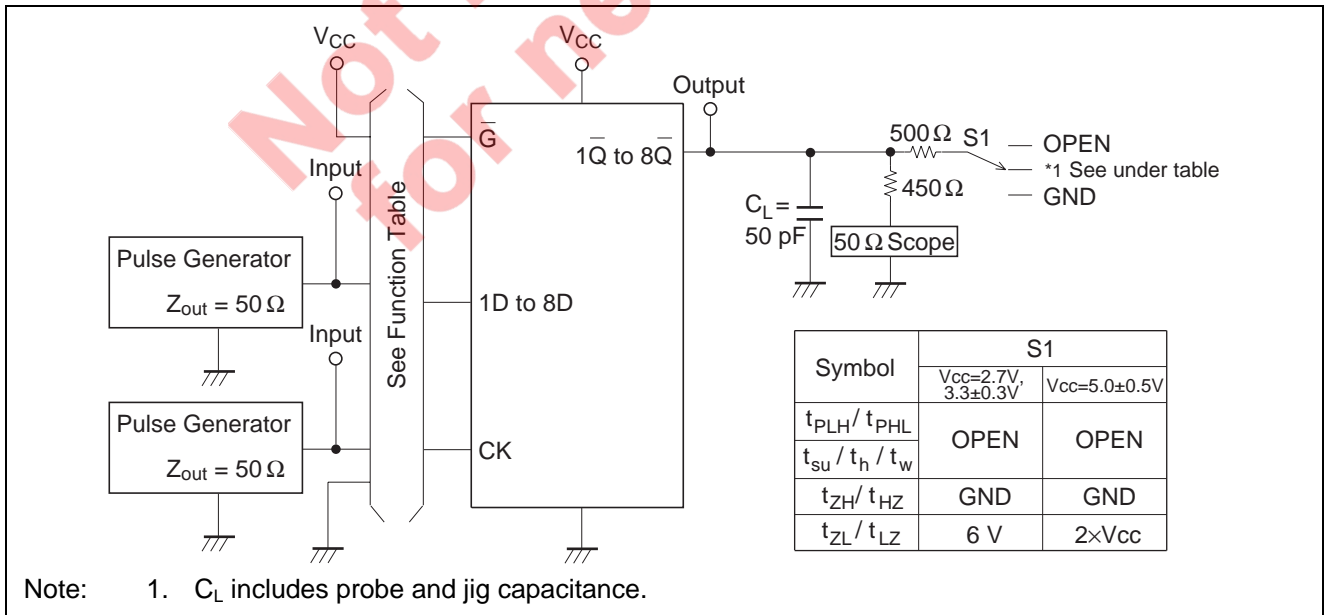
Electrical Characteristics

Item	Symbol	V_{CC} (V)	$T_a = -40\text{ to }85^\circ\text{C}$		Unit	Test Conditions
			Min	Max		
Input voltage	V_{IH}	2.7 to 3.6	2.0	—	V	
		4.5 to 5.5	$V_{CC} \times 0.7$	—		
	V_{IL}	2.7 to 3.6	—	0.8	V	
		4.5 to 5.5	—	$V_{CC} \times 0.3$		
Output voltage	V_{OH}	2.7 to 5.5	$V_{CC} - 0.2$	—	V	$I_{OH} = -100\ \mu\text{A}$
		2.7	2.2	—		$I_{OH} = -12\ \text{mA}$
		3.0	2.4	—		
		3.0	2.0	—		$I_{OH} = -24\ \text{mA}$
		4.5	3.8	—		
	V_{OL}	2.7 to 5.5	—	0.2	V	$I_{OL} = 100\ \mu\text{A}$
		2.7	—	0.4		$I_{OL} = 12\ \text{mA}$
		3.0	—	0.55		$I_{OL} = 24\ \text{mA}$
		4.5	—	0.55		
Input current	I_{IN}	0 to 5.5	—	±5.0	μA	$V_{IN} = 5.5\text{ V or GND}$
Off state output current	I_{OZ}	5.5	—	±10	μA	$V_{IN} = V_{CC}, \text{ GND}$ $V_{OUT} = V_{CC} \text{ or GND}$
Quiescent supply current	I_{CC}	5.5	—	20	μA	$V_{IN} = V_{CC} \text{ or GND}$
	ΔI_{CC}	3.0 to 3.6	—	500	μA	$V_{IN} = \text{one input at } (V_{CC} - 0.6)\text{V},$ other inputs at $V_{CC} \text{ or GND}$

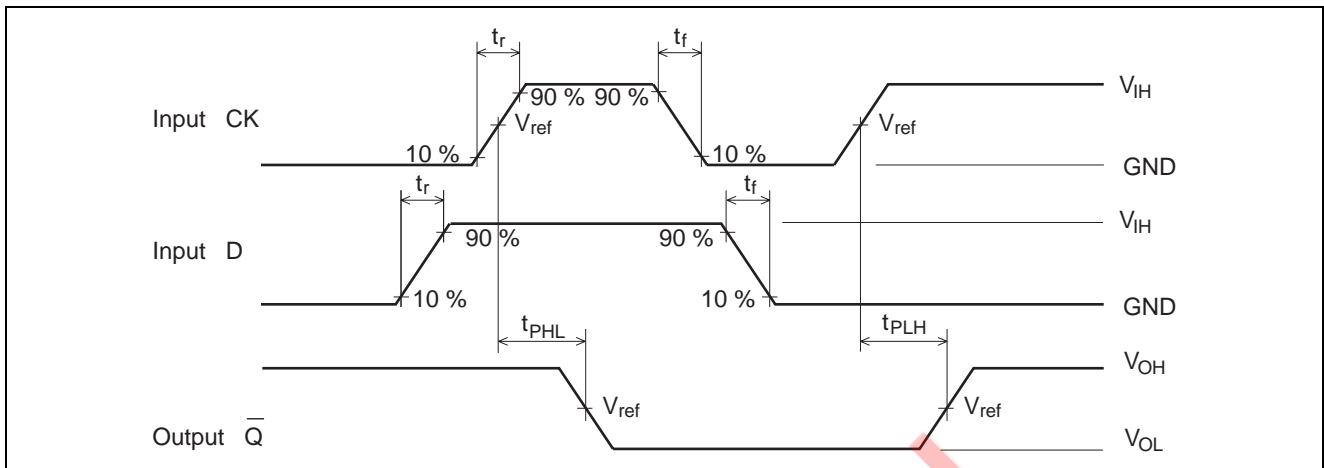
Switching Characteristics

Item	Symbol	V _{CC} (V)	Ta = -40 to 85°C			Unit	From (Input)	To (Output)
			Min	Typ	Max			
Maximum clock frequency	f _{max}	2.7	80.0	—	—	MHz		
		3.3±0.3	100.0	150.0	—			
		5.0±0.5	125.0	—	—			
Propagation delay time	t _{PLH} t _{PHL}	2.7	—	7.0	9.5	ns	CK	Q̄
		3.3±0.3	1.5	5.5	8.5			
		5.0±0.5	—	4.0	7.0			
Output enable time	t _{ZH} t _{ZL}	2.7	—	7.0	9.5	ns	Ḡ	Q̄
		3.3±0.3	1.5	5.5	8.5			
		5.0±0.5	—	4.0	7.0			
Output disable time	t _{HZ} t _{LZ}	2.7	—	5.0	8.5	ns	Ḡ	Q̄
		3.3±0.3	1.5	4.5	7.5			
		5.0±0.5	—	3.5	6.5			
Setup time	t _{su}	2.7	2.0	—	—	ns		
		3.3±0.3	2.0	—	—			
		5.0±0.5	2.0	—	—			
Hold time	t _h	2.7	1.5	—	—	ns		
		3.3±0.3	1.5	—	—			
		5.0±0.5	1.5	—	—			
Pulse width	t _w	2.7	4.0	—	—	ns		
		3.3±0.3	4.0	—	—			
		5.0±0.5	3.0	—	—			
Input capacitance	C _{IN}	2.7	—	3.0	—	pF		
Output capacitance	C _O	2.7	—	15.0	—	pF		

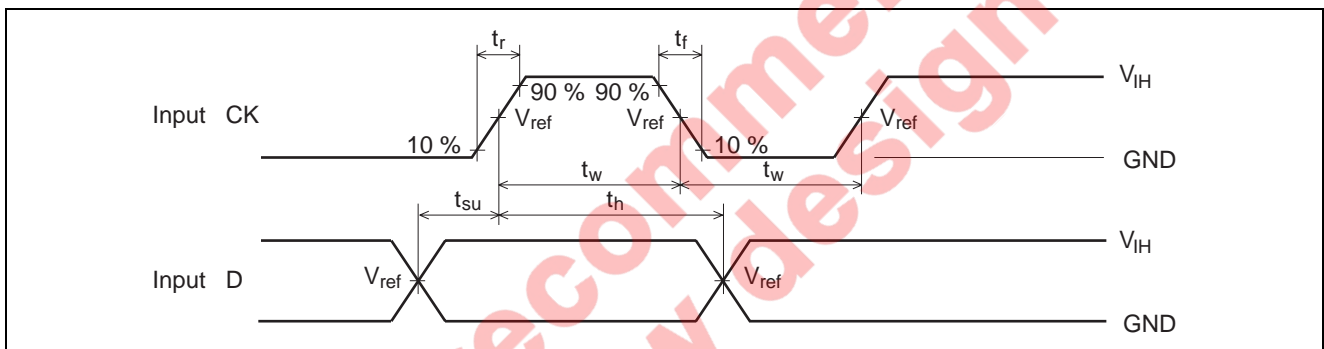
Test Circuit



Waveforms – 1

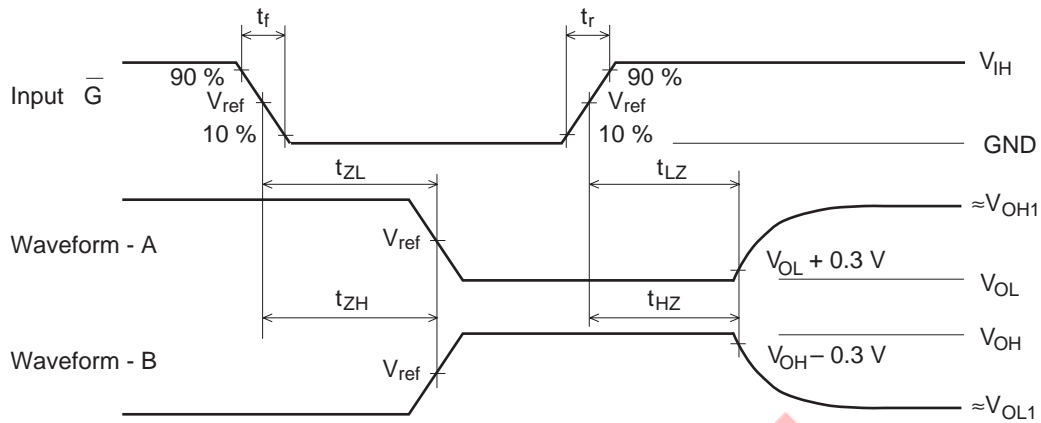


Waveforms – 2



Not recommended for new design

Waveforms – 3

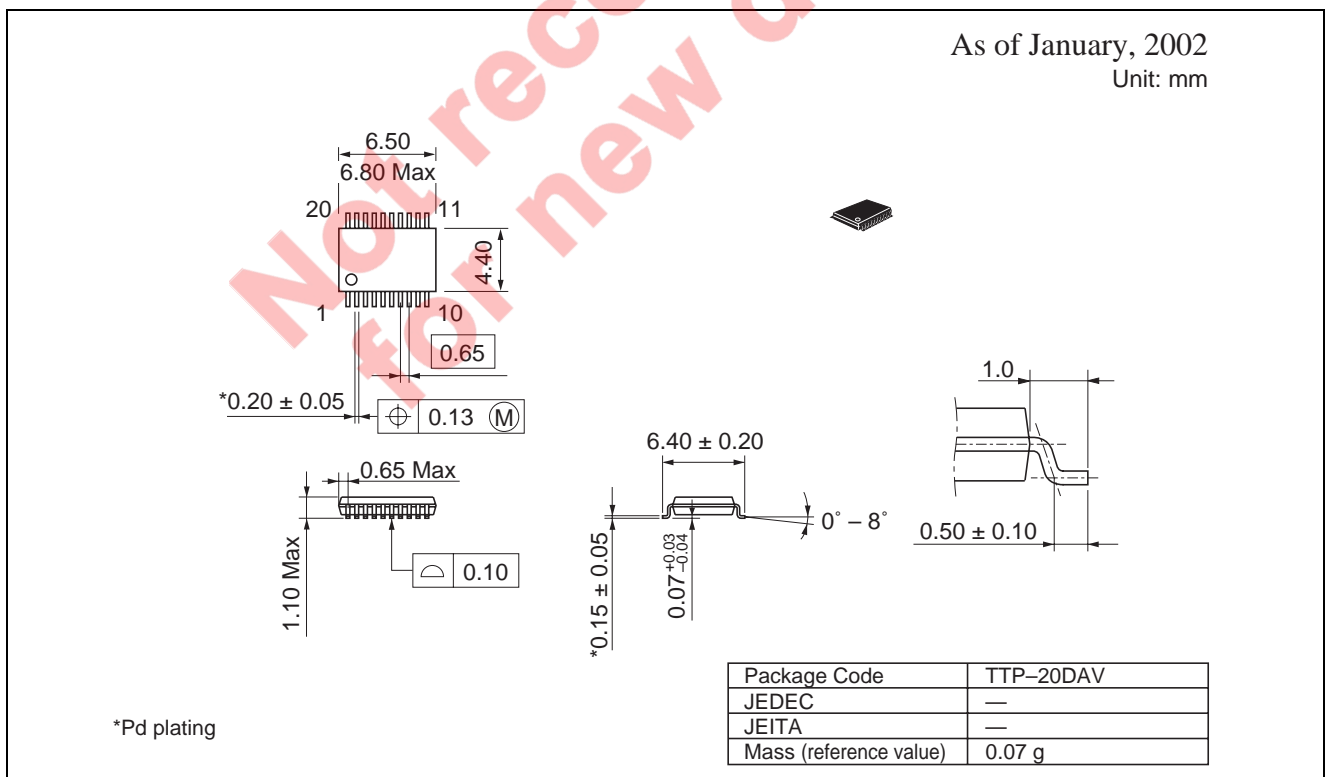
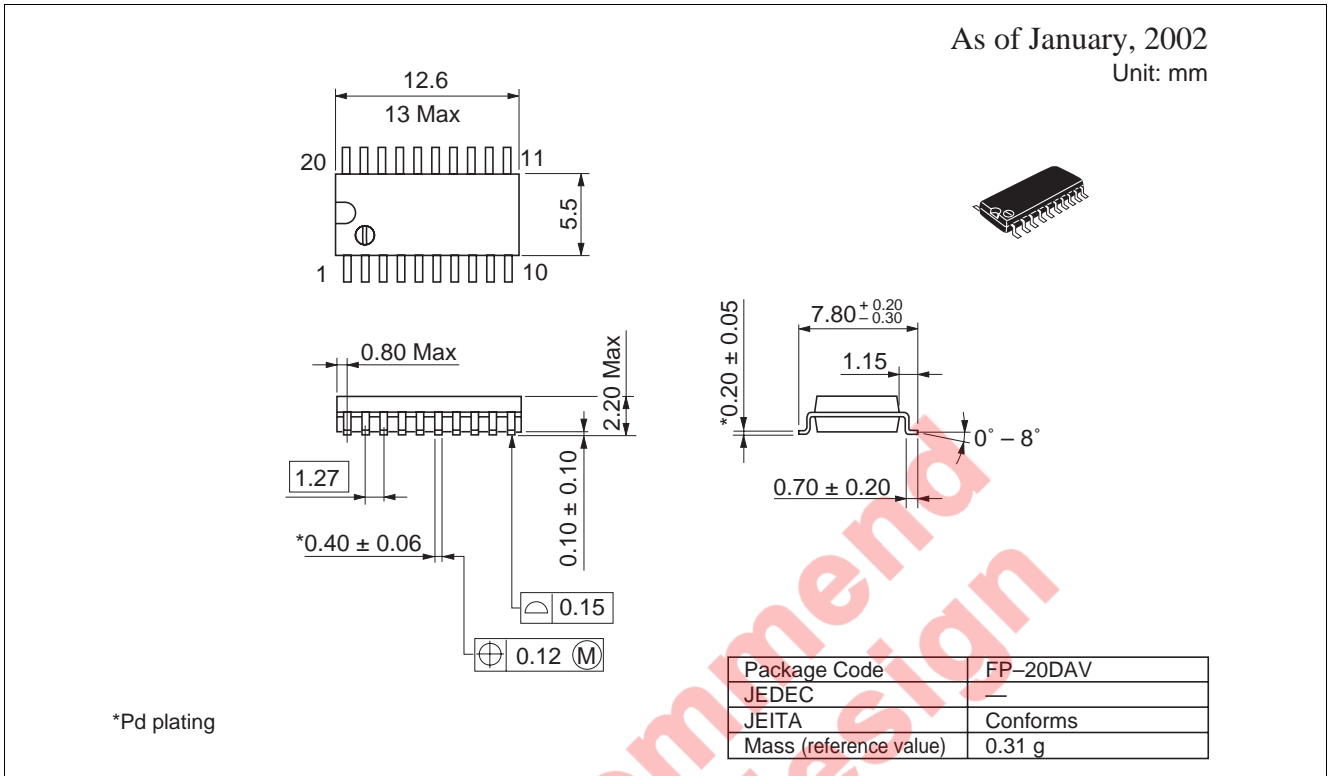


TEST	$V_{cc}=2.7V, 3.3\pm 0.3V$	$V_{cc}=5.0\pm 0.5V$
V_{IH}	2.7 V	V_{cc}
V_{ref}	1.5 V	50% V_{cc}
V_{OH1}	3 V	V_{cc}
V_{OL1}	GND	GND

- Notes:
1. $t_r = 2.5 \text{ ns}$, $t_f = 2.5 \text{ ns}$
 2. Input waveform : PRR = 10 MHz, duty cycle 50%
 3. Waveform – A shows input conditions such that the output is "L" level when enable by the output control.
 4. Waveform – B shows input conditions such that the output is "H" level when enable by the output control.

Not recommended for new design

Package Dimensions



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