The DLO4135/DLG4137 5 x 7 Dot Matrix Intelligent Display® Appnote 28

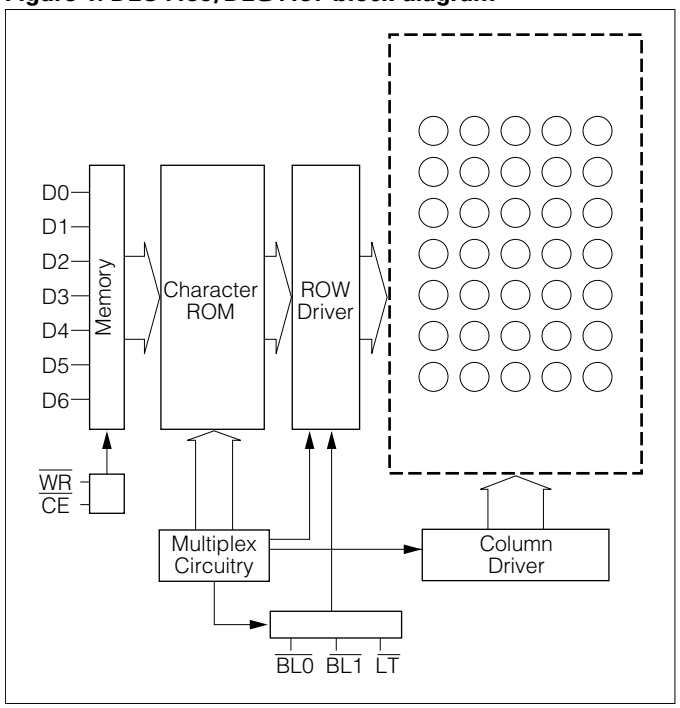
This application note is intended to serve as a design and application guide for users of the DLO4135 and DLG4137 OSRAM Intelligent Displays. This appnote covers device electrical description, operation, general circuit design considerations, and interfacing to microprocessors.

Electrical Description

The DLO4135/DLG4137 Intelligent Alphanumeric 5x7 Dot Matrix Display contains memory, character generator, multiplexing circuits, and drivers built into a single package.

Figure 1 is a block diagram of DLO4135/DLG4137. The unit consists of 35 LED die arranged in a 5x7 pattern and a single CMOS integrated circuit chip. The IC chip contains the column drivers, row drivers, 128 character generator ROM, memory, multiplex and blanking circuitry.

Figure 1. DLO4135/DLG4137 block diagram



Thirty-five dots form a 0.30 x 0.43 inch overall character size in a.500 x 1.00 inch dual-in-line package. The ±50 degree wide viewing angle complements the display and is the ideal display for industrial control applications. Display construction is filled reflector type with the integrated circuit in the back also filled with IC-grade epoxy. This results in a very rugged part which is resistant to moisture, shock and vibration.

Figure 2. Physical dimensions in inches (mm)

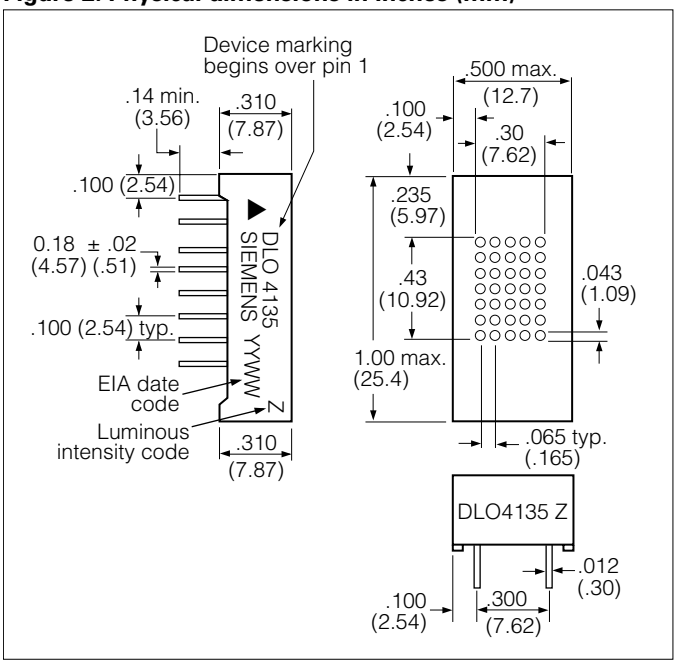


Table 1. DLO4135/DLG4137 pin functions

Pin	Function	Pin	Function
1	$\overline{LT}$ Lamp Test	9	D0 data LSB
2	$\overline{WR}$ Write	10	D1 data
3	$\overline{BL1}$ Brightness	11	D2 data
4	$\overline{BL0}$ Brightness	12	D3 data
5	No Pin	13	D4 data
6	No Pin	14	D5 data
7	$\overline{CE}$ Chip Enable	15	D6 data MSB
8	GND	16	$+V_{CC}$

Table 2. Pin description

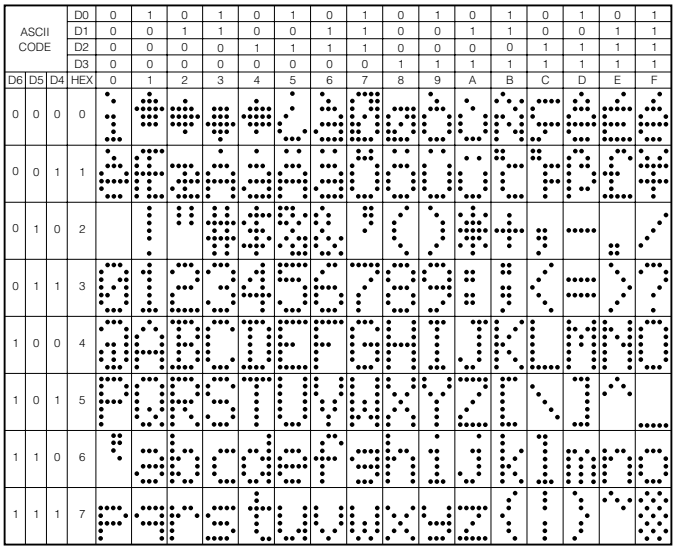
V_{CC}	Positive Supply +5 volts
GND	Ground
D0-D6	Data Lines, see Figure 3 (Character set)
$\overline{CE}$	Chip Enable (active low) This determines which device in an array will accept data
$\overline{WR}$	Write (active low) Data and chip enable must be present and stable before and after the write pulse (see data sheet for timing)
$\overline{BL0}$, $\overline{BL1}$	Blanking Control Input (active low) Used to control the level of display brightness
$\overline{LT}$	Lamp Test (active low) Causes all dots to light at 1⁄2 brightness

Operation

In a dot matrix display system, it is advantageous to use a multiplexed approach with 12 drivers (5 digit plus 7 segments) rather than 35 segment drivers. This obviously reduces the number of drivers and interconnections required. A multiplexed system must be a synchronous system, or the digits or elements may have different on (lit) times and therefore varying brightness.

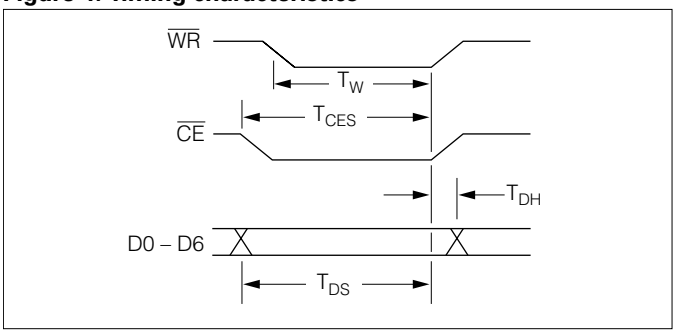
The DLO4135/DLG4137 is an internally multiplexed display, but the data entry is asynchronous. Loading data is similar to writing into a RAM. Present the data, select the chip, and give a write signal. For a multi digit system, each digit has its own unique address location and will display its contents until replaced by another code. The waveforms of Figure 4 shows the relationship of the signals required to generate a write cycle. Check the data sheet for minimum values required for each signal.

Figure 3. Character set



1. High=1 level. 2. Low=0 level.

Figure 4. Timing characteristics



Display Blanking and Dimming

The DLO4135/DLG4137 Intelligent Display has the capability of three levels of brightness plus blank. Figure 5 shows the combination of $\overline{BL0}$ and $\overline{BL1}$ for the different levels of brightness. The $\overline{BL0}$ and $\overline{BL1}$ inputs are independent of write and chip enable and does not affect the contents of the internal memory. A flashing display can be achieved by pulsing the blanking pins at a 1–2 hertz rate. Either $\overline{BL0}$ or $\overline{BL1}$ should be held high to light up the display.

Table 3. Dimming and blanking control

Brightness Level	**$\overline{BL1}$**	**$\overline{BL0}$**
Blank	0	0
1/7 brightness	0	1
1/2 brightness	1	0
full brightness	1	1

Lamp Test

The lamp test when activated causes all dots on the display to be illuminated at 1/7 brightness. It does not destroy any previously stored characters. The lamp test function is independent of chip enable, write, and the settings of the blanking inputs.

This convenient test gives a visual indication that all dots are functioning properly. The lamp test can be used as a cursor or pointer in a line of displays because it does not affect the display memory.

General Design Considerations

When using the DLO4135/DLG4137 on a separate display board having more than 6 inches of cable length, it may be necessary to buffer all of the input lines. A non-inverting 74LS244 buffer can be used. The object is to prevent current transient into the DLO4135/DLG4137 protection diodes. The buffers should be located on the display board and as close to the displays as possible.

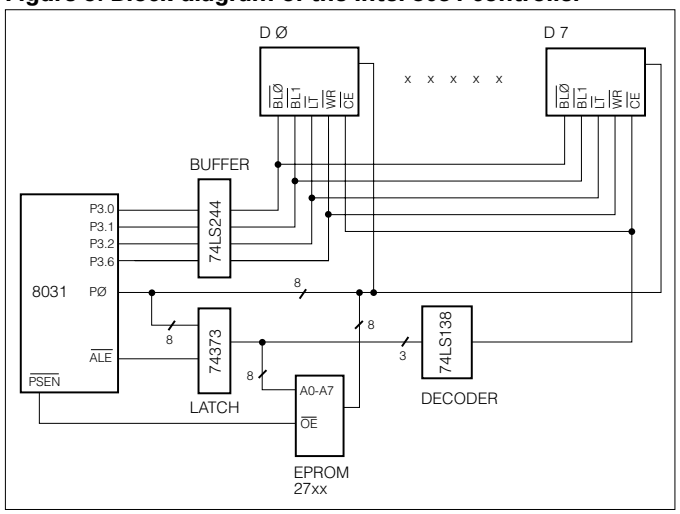
Because of high switching currents caused by the multiplexing, local power supply by-pass-capacitors are also needed in many cases. These should be 10 volt, tantalum type having 10 uf capacitance. The capacitors may only be required every 2 displays depending on the line regulation and other noise generators.

Decoupling capacitors should also be used across V_{CC} and ground of each display. Typical value of these capacitors is 0.01 mF/10 V.

If small wire cables are used, good engineering practice is to calculate the wire resistance of the ground and the +5 volt wires. More than 0.2 volt drop (at 100 ma per digit) should be avoided, since this loss is in addition to any inaccuracies or load regulation of the power supply.

The 5 volt power supply for the DLO4135/DLG4137 should be the same one supplying the V_{CC} to all logic devices. If a separate power supply must be used, then local buffers should be used on all the inputs. These buffers should be powered from the display power supply. This precaution is to avoid line transients or any logic signals to be higher than V_{CC} during power up.

Figure 5. Block diagram of the Intel 8031 controller



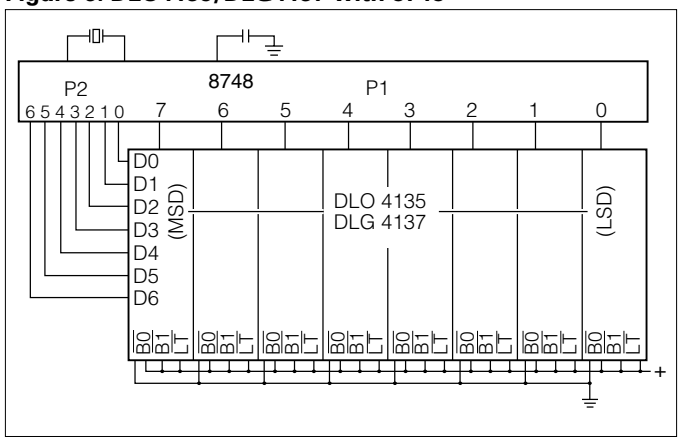
Interfacing

For an eight digit display using the DLO4135/DLG4137, interfacing to a single chip microprocessor such as the 8748, is easy and straight forward. One approach may be to dedicate one port for the seven data signals and another 8-bit port for the write signals. The schematic is shown in Figure 6.

I/O or Memory Mapped System

For a memory mapped system using a processor such as the 8080 or 8085, the interfacing is also straight-forward. Each display is treated as a memory location with its own address, like another I/O or RAM location. See Figure 7.

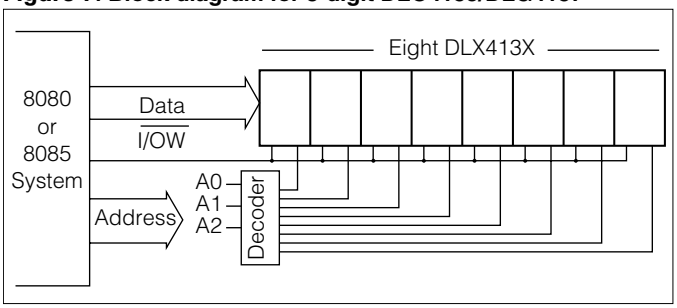
Figure 6. DLO4135/DLG4137 with 8748



Subroutine to Load an 8-digit Display using the DLO4135/DLG4137

```
                        ; DATA IN RAM 10H-17H
                          (MSD-LSD)
INIT    ORL   P1,#0FFH  ; PORT 1 ALL HIGH (WRITE)
        ORL   P2,#00H   ; PORT 2 ALL LOW (DATA)
        MOV   R1,#OFH   ; RAM ADDRESS—1
        MOV   R2,#0FEH  ; WRITE PULSE
        MOV   R3,#08H   ; COUNTER
START:  INC   R1        ; INCREMENT RAM POINTER
DATA:   MOV   A,@R1     ; FETCH DATA FROM RAM
        OUTL  P2,A      ; LOAD PORT 2
        MOV   A,R2      ; RECALL WRITE
        RR    A         ; SHIFT A TO NEXT WRITE
        MOV   R2,A      ; SAVE WRITE
WRITE:  OUTL  P1,A      ; SEND WRITE PULSE
        MOV   A,#OFFH   ; WAIT
        OUTL  P1,A      ; RESET WRITE PULSE
        DJNZ  R3,START  ; LOAD COMPLETE?
        RET             ; RETURN TO MAIN PROGRAM
```

Figure 7. Block diagram for 8-digit DLO4135/DLG4137



Routine for an 8-Digit Display using the DLO4135/DLG4137 and 8085 or 8080 Microprocessor

```
                        ; DATA TO BE DISPLAYED IS IN
                        ; A0 (LSD) THRU A7 (MSD)
                        ;
                        ; DISPLAY ADDRESS C00X
                        ; LSD IS RIGHT MOST DIGIT
                        ;
                        ; DOES NOT SAVE REG A,B,H,L,D,E
                        ;
DADD    EQU   0A000H    ; DATA ADDRESS LOCATION
DPAD    EQU   0C000H    ; DISPLAY ADDRESS
                          LOCATION
LEN     EQU   08H       ; DISPLAY LENGTH
                        ;
ORG     100H            ;
DISP:   LXI   H,DADD    ; LOAD DATA ADDRESS
        LXI   D,DPAD    ; LOAD DISPLAY ADDRESS
        MVI   B,LEN     ; LOAD DISPLAY LENGTH
DISP1:  MOV   A,M       ; GET DATA
        XCHG            ; XCHG H/L & D/E
        MOV   M,A       ; LOAD DISPLAY FROM REG A
        XCHG            ; RESTORE H/L & D/E
        INX   D         ; INCREMENT DISPLAY ADDRESS
        INX   H         ; INCREMENT DATA ADDRESS
        DCR   B         ; DECREMENT LENGTH COUNTER
        JNZ   DISP1     ; END OF DISPLAY?
        RET             ; RETURN TO MAIN PROGRAM
```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Conclusion

Note that although other manufacturers' products are used in the examples, this application note does not imply specific endorsement, or warranty of other manufacturer's products by OSRAM. The interface schemes shown demonstrate the simplicity of using the DLO4135/DLG4137 dot matrix Intelligent Display. Slight timing differences may be encountered for various microprocessors, but can be resolved using similar methods as those used when using interfacing microprocessors with various RAMs. The techniques used in the examples were shown for their generality. The user will undoubtedly invent other schemes to optimize his particular system to its requirements.

Program Listing

```
1                                       ; BY DAN WATSON
2                                       ; TO DO LAMP TEST,  SET 100% BRIGHTNESS
3                                       ; AND WRITE 'SIEMENS*'
4
5                                       ; P3.0 = BLO\
6                                       ; P3.1 = BL1\
7                                       ; P3.2 = LT\
8                                       ; P3.6 = WR\
9
10                                      ; RO = DIGIT ADDRESS ( CHIP ENABLES – CE\ )
11                                      ; R1 = DIGIT COUNTER
12                                      ; R7 = R6 = R5 = WAIT REGISTERS
13
14      0000                            .ORG 00H
15      0000    02  00  03                  INIT:JMP BEGIN
16      0003    12  00  24                  BEGIN:CALL WAIT1        ; DELAY FOR uC TO STABILIZE
17      0006    75  B0  00                      MOV P3,#00H         ; LAMP TEST
18      0009    12  00  24                      CALL WAIT1          ; DISPLAY LT\ FOR A WHILE
19      000C    75  B0  07                      MOV P3,#07H         ; SET ALL 8 DISPLAYS TO 100% BRT
20      000F    00                              NOP
21      0010    00                              NOP
22      0011    78  00                          MOV R0,#00H         ; DIGIT 7 ADDRESS
23      0013    79  08                          MOV R1,#08H         ; 8 DIGIT COUNTER
24      0015    74  00                          MOV A,#00H          ; CLEAR ACC.
25      0017    90  00  37                      MOV DPTR,#TEXT      ; ADDRESS OF THE MESSAGE
26      001A    93                          WRT:MOVC A,@A+DPTR      ; LOAD FIRST CHAR. INTO THE ACC.
27      001B    F2                              MOVX @R0,A          ; DIGIT ADDRESS AND DATA WRITE
28      001C    A3                              INC DPTR            ; NEXT CHARACTER ADDRESS
29      001D    08                              INC R0              ; NEXT DIGIT (6) ADDRESS
30      001E    E4                              CLR A
31      001F    D9  F9                          DJNZ R1,WRT         ; WRITE ALL 8 CHAR.
32      0021    00                          GO:NOP
33      0022    01  21                          JMP GO              ; MESSAGE ALWAYS ON
34      0024
35      0024
36      0024    7F  88                      WAIT1:MOV R7,#88H       ; DELAY LOOPS
37      0026    00                              NOP
38      0027    7E  FF                      WAIT2:MOV R6,#FFH
39      0029    00                              NOP
40      002A    7D  FF                      WAIT3:MOV R5,#FFH
41      002C    00                              NOP
42      002D    DD FE                           DJNZ R5,$
43      002F    00                              NOP
44      0030    DE  F8                          DJNZ R6,WAIT3
45      0032    00                              NOP
46      0033    DF  F2                          DJNZ R7,WAIT2
47      0035    00                              NOP
48      0036    22                              RET
49
50      0037    53  49  45  4D  45          TEXT:DB 'SIEMENS*'
        003C    4E  53  2A
51      003F
52      003F                            .END
```