6-18GHz Amplifier

GaAs Monolithic Microwave IC

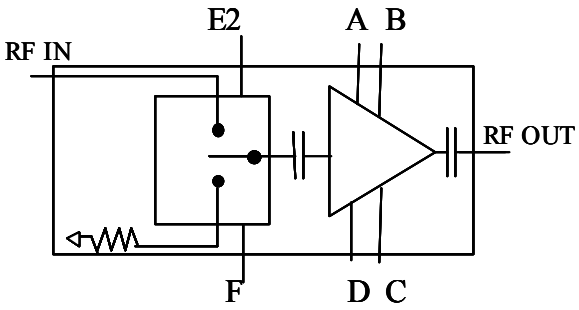
preliminary

Description

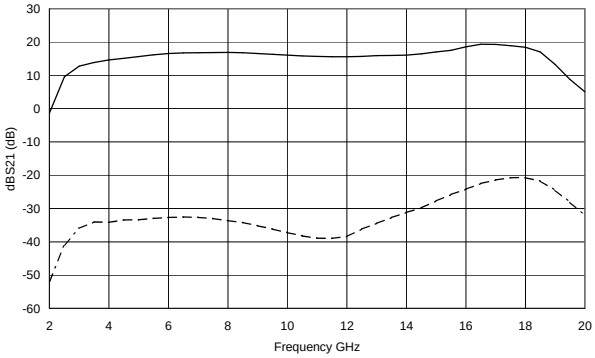
The CHA3511 is composed of a Single Pole Single Through (SPST) switch followed by a double stage travelling wave amplifier. It is designed for defence, naval, or avionic applications. The backside of the chip is both RF and DC grounded. This helps to simplify the assembly process.

The circuit is manufactured with a Power-HEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is available in chip form.



Typical on wafer Measurements
Gain versus switch states



Main Features

■Wide Band: 6-18GHz
■16dB gain
■39dB isolation
■22 dBm saturated output power
■DC power consumption, 190mA@ 4.5V
■Chip size: 3.55 x 2.30 x 0.1 mm

Main Characteristics

Tamb. = 25℃

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	6		18	GHz
G	Small signal gain @ Switch on	15	16		dB
ISO	Delta Gain (1)	35	39		dB
Psat	Saturated Output power @Switch on	20	22		dBm

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions!

United Monolithic Semiconductors S.A.S.
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Electrical Characteristics on wafer

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Tamb = +25℃
Vd (Pads D & B)= 4.5V, Vg (Pads A & C) tuned for Id= 190mA
Configuration Gain:E2=-5V; F=0V
Configuration isolation: E2=0V; F=-5V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range (1)	6		18	GHz
G	Small signal gain @ Config Gain		16		dB
ISO	Delta Gain between config Gain & config. Isolation	35	39		dB
P1dB	Output power at 1dB compression @ Config. Gain	18	20		dBm
Psat	Saturated Output power @ config. gain	20	22		dBm
NF	Noise figure @ Config. Gain 6-12 GHz 12-18 GHz		 6 8	 8 10	 dB dB
VSWRin	Input VSWR @Config gain		2.3:1		
VSWRout	Output VSWR @Config. gain		2.0:1		
Vd	Drain bias DC voltage (Pads D,B)		4.5		V
Id	Bias current @ small signal		190	250	mA
Vc	Control voltage for Attenuator bits		-5/0		V

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Absolute Maximum Ratings

Tamb. = 25℃ (1)

Symbol	Parameter	Values	Unit
Vd	Maximum Drain bias voltage (Pads B,D)	+5	V
Id	Drain bias current with Vd=4.5V	300	mA
Vg	Gate bias voltage (Pads A, C)	-2 to +0.4	V
Vc	Fet switch gate voltage (2) SPST switch control voltage	-7 to +0.6	V
Pin	Maximum input power overdrive (3)	+20	dBm
Tch	Maximum channel temperature	+175	℃
Ta	Operating temperature range	-40 to +70	℃
Tstg	Storage temperature range	-55 to +125	℃

(1)Operation of this device above anyone of these parameters may cause permanent damage.

(2)The switch is ON in the following condition : Pad F=0V & Pad E2=-5V; the switch is OFF when pad F=-5V & PAD E2=0V

(2) Duration < 1s.

Circuit Biasing Conditions

Drain Voltage on B and D pads=4.5V
Gate voltage adjusted on A and C pads for a drain current =190mA

SPST Control		Configuration selected
E2	**F**	
-5V	0V	1: Gain
0V	-5V	2: Isolation

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Typical chip on wafer Sij parameters for reference state

Tamb 25℃,Bias conditions:Vd(Pads B&D)=4.5V, Vg(Pad s A & C) tuned for Id=190mA
Configuration Gain:Pad E2=-5V / pad F=0V

Freq (GHz)	S11(dB)	PhS11(°)	S12(dB)	PhS12(°)	S21(dB)	PhS2 1(°)	S22(dB)	PhS22(°)
4.0	-9.5	154.9	-66.3	146.8	15.2	-67.3	-10.7	174.1
5.0	-12.0	129.9	-69.6	123.3	16.3	-129.1	-13.3	157.1
6.0	-14.3	107.7	-62.6	21.1	17.1	173.2	-15.0	140.2
7.0	-15.7	81.9	-59.2	-14.4	17.4	118.0	-16.9	122.9
8.0	-16.0	48.4	-56.1	-85.3	17.4	64.6	-17.8	103.3
9.0	-14.4	5.8	-54.0	-109.4	16.9	12.9	-18.3	69.8
10.0	-12.2	-34.4	-52.6	-157.0	16.4	-35.8	-18.6	29.4
11.0	-10.5	-68.9	-51.6	163.8	15.8	-81.7	-18.1	-18.3
12.0	-9.2	-99.1	-49.8	150.9	15.8	-125.7	-17.3	-70.0
13.0	-8.7	-126.1	-49.8	126.6	16.1	-170.8	-16.3	-125.6
14.0	-9.2	-154.5	-43.5	103.0	16.5	139.9	-17.2	163.7
15.0	-11.0	-175.5	-43.8	37.7	17.1	91.8	-19.4	78.6
16.0	-14.0	170.8	-45.2	-31.4	18.7	39.0	-17.0	-14.5
17.0	-15.9	-172.9	-45.7	-156.6	20.3	-30.3	-17.4	-87.5
18.0	-14.1	170.8	-40.8	110.8	19.3	-110.4	-14.6	-78.7
20.0	-10.5	102.1	-44.2	-9.5	6.6	94.2	-9.7	159.7

Typical on wafer Measurements @ 25℃

Bias conditions:Vd(Pads B&D)=4.5V, Vg(Pads A & C) tuned for Id=190mA
Configuration Isolation:Pad E2=0V / pad F=-5V

Freq (GHz)	S11(dB)	PhS11(°)	S12(dB)	PhS12(°)	S21(dB)	PhS21(°)	S22(dB)	PhS22(°)
4.0	-1.2	149.2	-71.2	128.5	-33.8	176.0	-10.7	174.1
5.0	-1.3	142.1	-72.9	-158.1	-32.0	118.9	-13.2	156.8
6.0	-1.4	134.8	-75.1	-69.3	-31.7	64.8	-15.0	139.7
7.0	-1.5	127.3	-77.2	68.3	-31.8	17.7	-16.9	122.8
8.0	-1.6	119.7	-66.2	-152.4	-33.2	-30.2	-17.8	103.0
9.0	-1.7	112.0	-70.9	-152.7	-36.2	-83.2	-18.6	69.1
10.0	-1.8	104.0	-65.9	153.0	-36.6	-135.5	-18.9	30.0
11.0	-1.9	95.9	-57.7	163.6	-37.9	159.1	-18.8	-18.0
12.0	-2.0	87.6	-54.0	164.6	-38.5	97.6	-18.0	-67.5
13.0	-2.0	78.5	-50.2	132.6	-36.6	40.5	-17.5	-119.7
14.0	-2.1	69.3	-45.3	85.4	-33.8	-22.5	-18.1	-178.3
15.0	-2.2	59.6	-48.2	39.2	-30.4	-79.1	-19.7	101.3
16.0	-2.3	49.7	-49.3	9.4	-26.3	-136.8	-17.9	7.2
17.0	-2.3	39.4	-53.6	9.2	-23.0	158.2	-16.0	-65.9
18.0	-2.4	29.2	-50.9	10.9	-20.3	76.0	-14.2	-85.3
19.0	-2.5	19.0	-52.7	-40.9	-24.1	-17.5	-8.4	-143.6
20.0	-2.5	8.8	-58.2	-10.3	-34.6	-86.3	-9.6	159.3

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Typical on wafer Measurements @ 25°C

Bias conditions:Vd(Pads B&D)=4.5V, Vg(Pads A & C) tuned for Id=190mA

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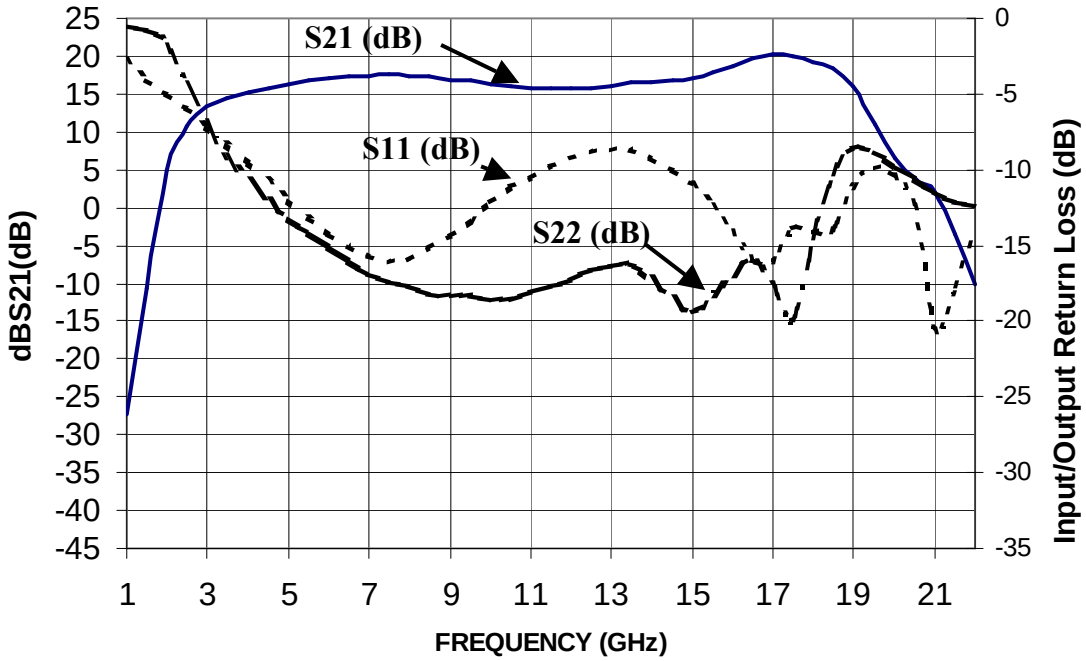
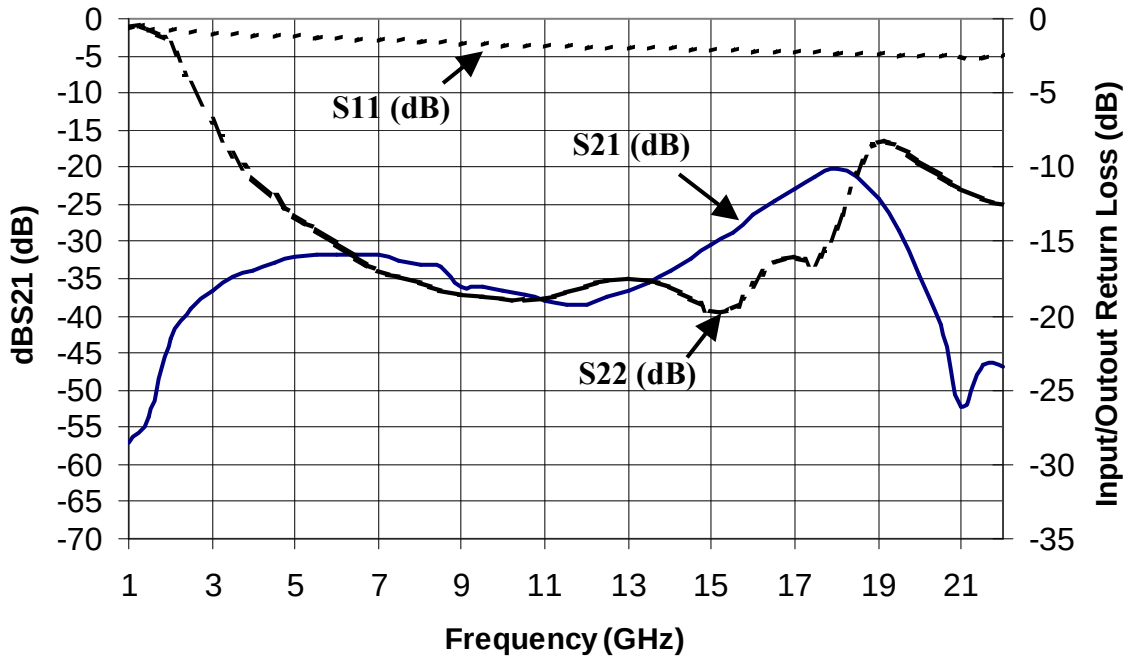
Configuration Gain (Pad E2=-5V/ Pad F=0V)
Gain/ input & output Return Loss



Configuration Isolation (Pad E2=-0V/ Pad F=-5V)
Isolation/ input & output Return Loss



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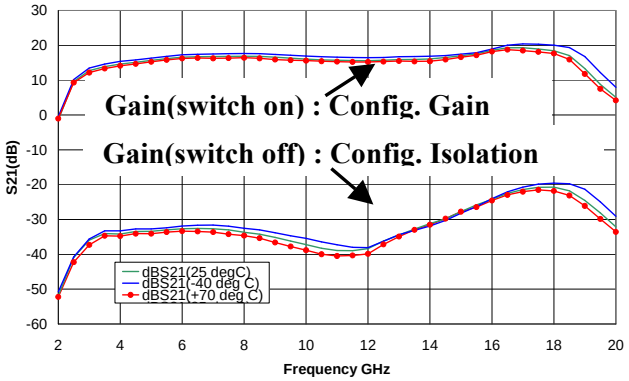
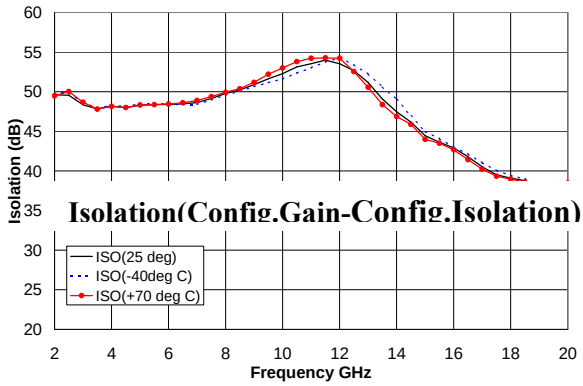
Typical test fixture Measurements

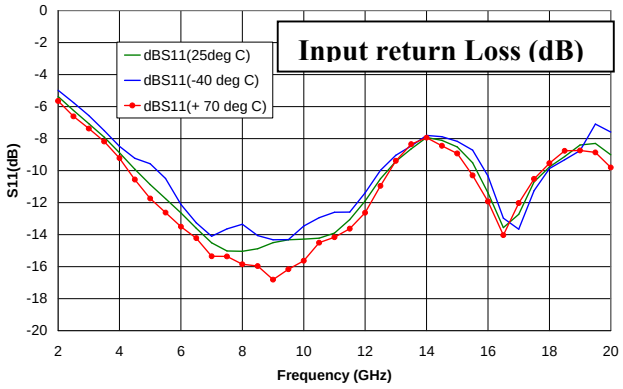
Bias conditions: Vd (Pads B & D)=4.5V, Vg(Pads A & C) tuned for Id = 190mA
Configuration Gain: Pad=E2=-5V/Pad F=0V

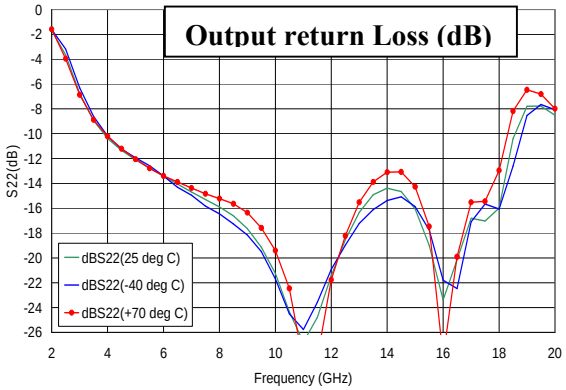
S Parameters: test fixture measurements

Measurements versus temperature



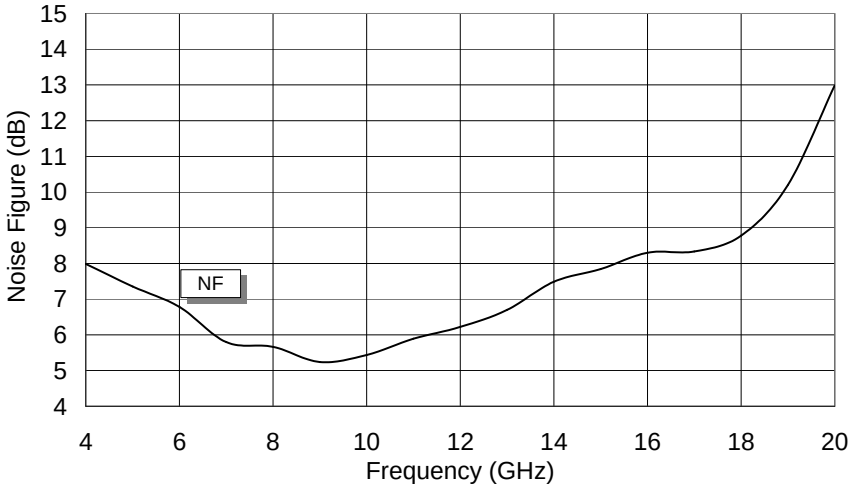






Tamb=+25℃

Noise Figure: test fixture measurements



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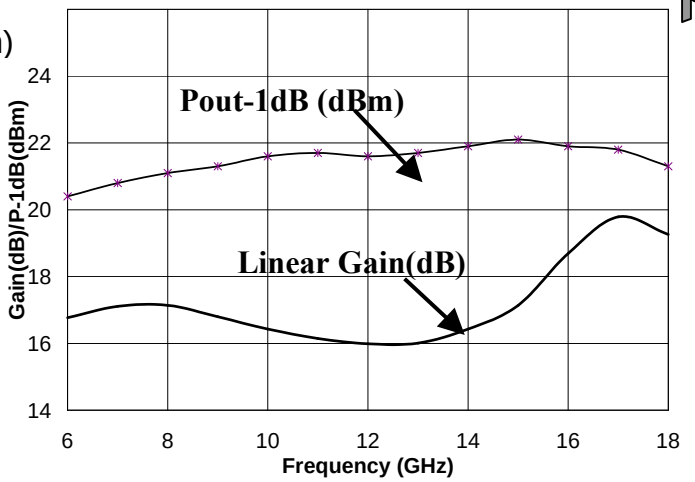
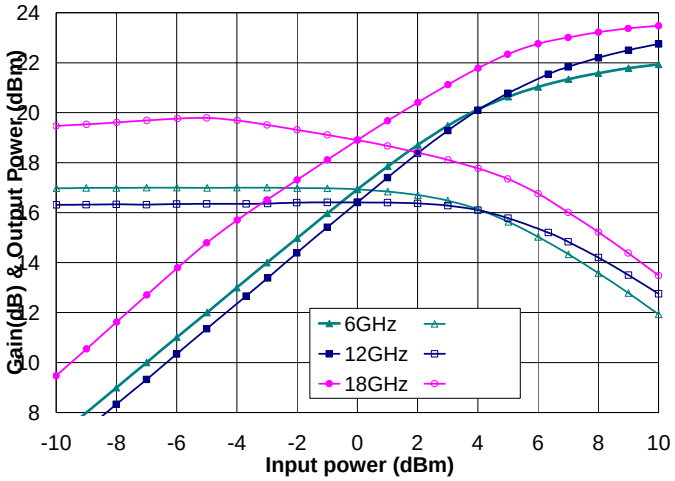
Linear Gain & Output Power for 1 dB compression
Versus frequency
Test fixture measurement

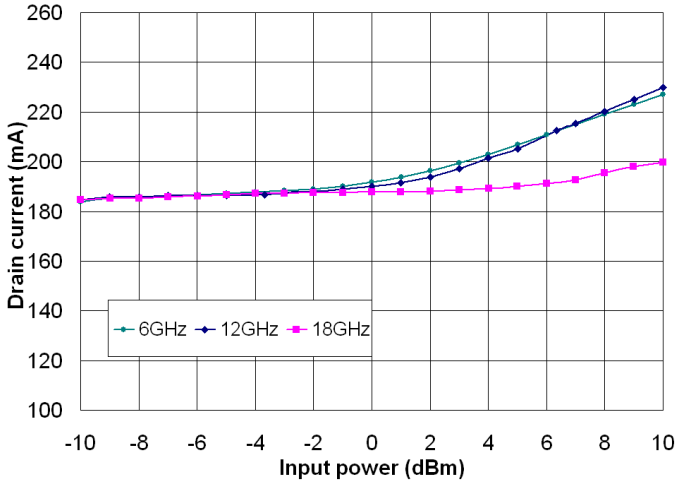
Tamb=+25°C
(configuration Gain)



Gain and Output power
Versus input power & Frequency
Test fixture measurement



Consumption versus Input power & frequency
Test fixture measurement



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Chip Assembly and Mechanical Data

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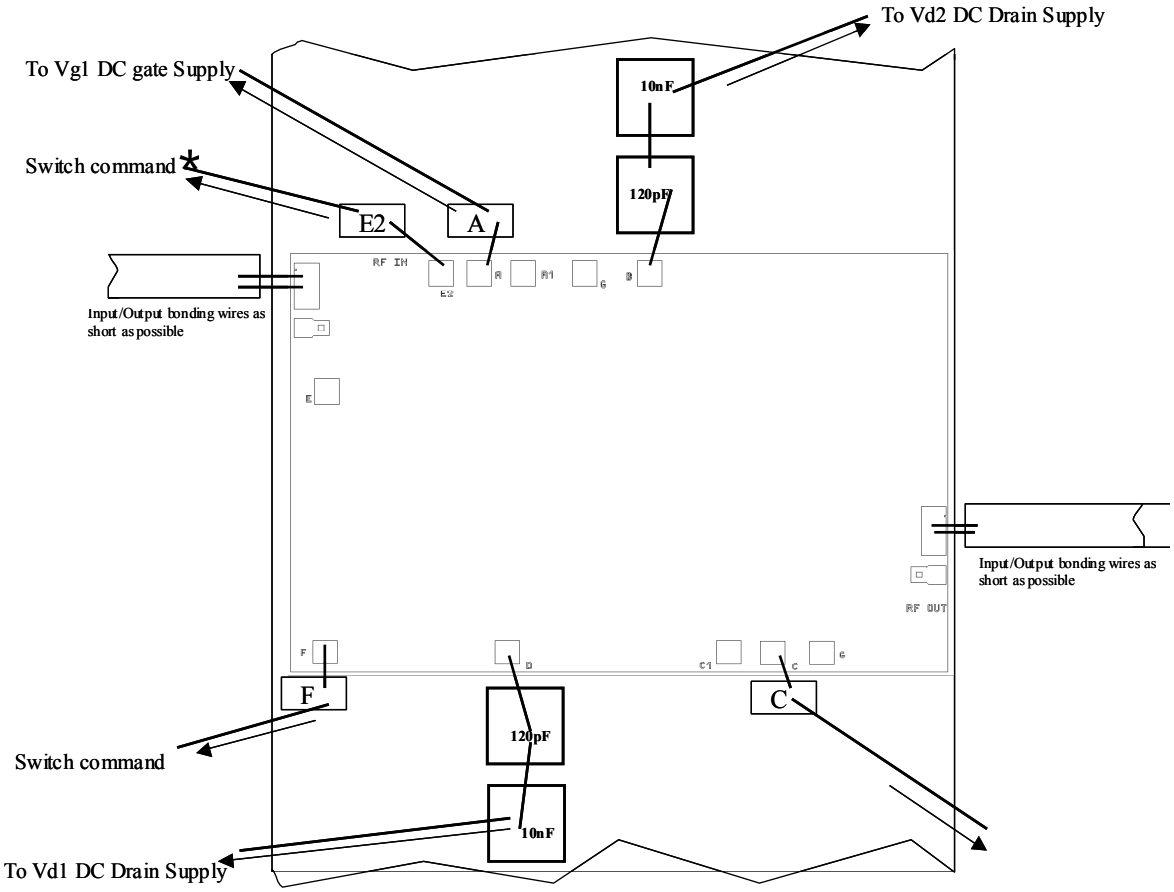

* The Pad E can be used in place of the Pad E2

Note : Supply feed should be capacitively bypassed. 25µm diameter gold wire is to be prefered.

Recommended circuit bonding table

Label	Type	Decoupling	Comment
B	Vd	120pF / 10nF	Drain Supply
D	Vd	120pF / 10nF	Drain Supply
A	Vg	*Not required*	Gate Supply
C	Vg	*Not required*	Gate Supply
E2	Vc	*Not required*	Switch control
F	Vc	*Not required*	Switch control

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Bonding pad positions

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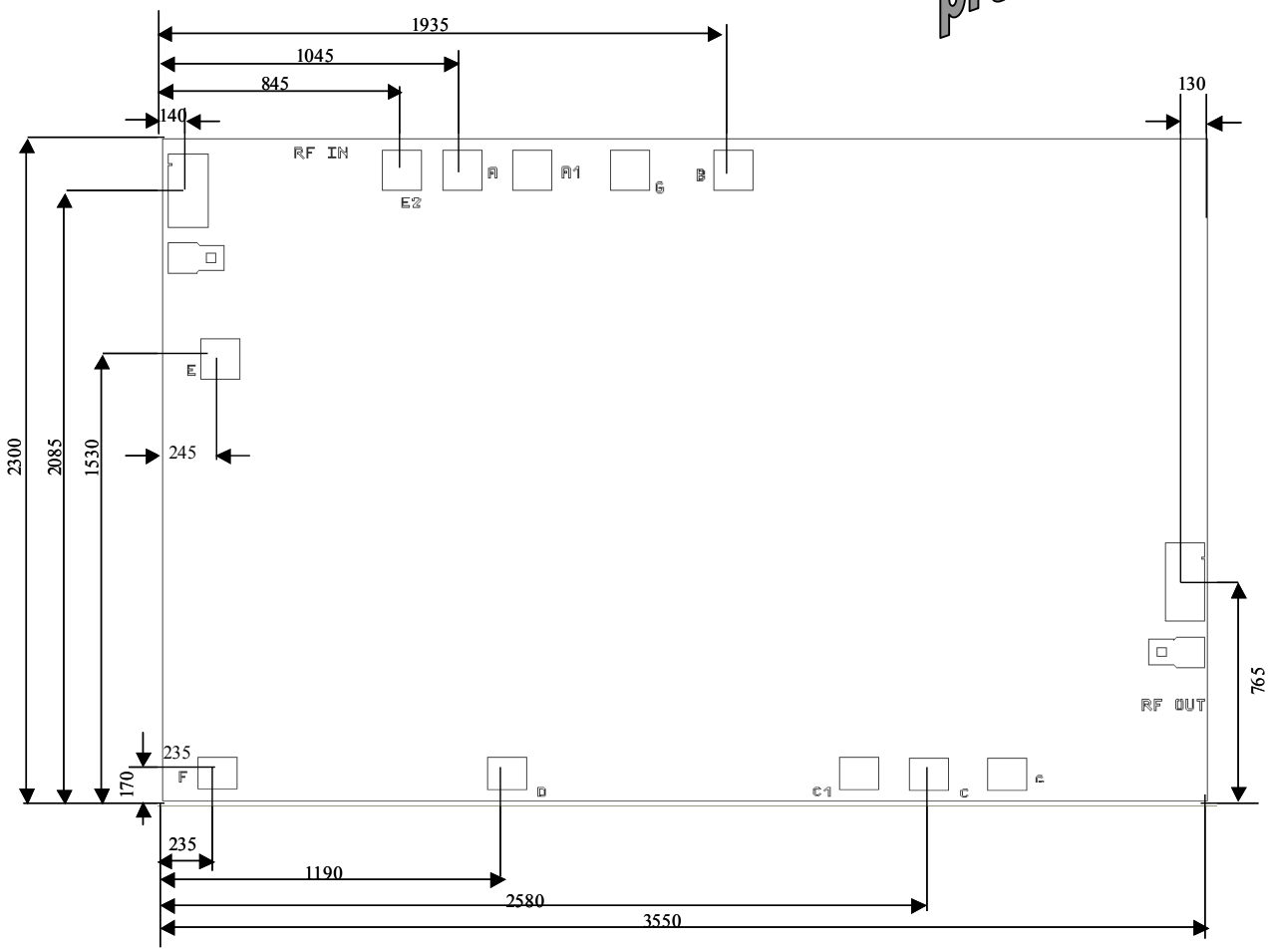

TOL :±35µm

(Chip thickness : 100µm ; All dimensions are in micrometers)

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Ordering Information

Chip form : CHA3511-99F/00

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