MC33272A, MC33274A, NCV33274A

Single Supply, High Slew Rate, Low Input Offset Voltage Operational Amplifiers

The MC33272/74 series of monolithic operational amplifiers are quality fabricated with innovative Bipolar design concepts. This dual and quad operational amplifier series incorporates Bipolar inputs along with a patented Zip−R−Trim element for input offset voltage reduction. The MC33272/74 series of operational amplifiers exhibits low input offset voltage and high gain bandwidth product. Dual−doublet frequency compensation is used to increase the slew rate while maintaining low input noise characteristics. Its all NPN output stage exhibits no deadband crossover distortion, large output voltage swing, and an excellent phase and gain margin. It also provides a low open loop high frequency output impedance with symmetrical source and sink AC frequency performance.

The MC33272/74 series is specified over −40° to +85°C and are available in plastic DIP and SOIC surface mount packages.

Features

- Pb−Free Packages are Available
- Input Offset Voltage Trimmed to 100 μV (Typ)
- Low Input Bias Current: 300 nA
- Low Input Offset Current: 3.0 nA
- High Input Resistance: 16 MΩ
- Low Noise: 18 nV/ $\sqrt{\text{Hz}}$ @ 1.0 kHz
- High Gain Bandwidth Product: 24 MHz @ 100 kHz
- High Slew Rate: 10 V/μs
- Power Bandwidth: 160 kHz
- Excellent Frequency Stability
- Unity Gain Stable: w/Capacitance Loads to 500 pF
- Large Output Voltage Swing: +14.1 V/ −14.6 V
- Low Total Harmonic Distortion: 0.003%
- Power Supply Drain Current: 2.15 mA per Amplifier
- Single or Split Supply Operation: +3.0 V to +36 V or ±1.5 V to ±18 V
- ESD Diodes Provide Added Protection to the Inputs
- NCV Prefix for Automotive and Other Applications Requiring Site and Control Changes

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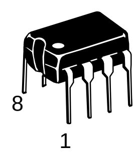
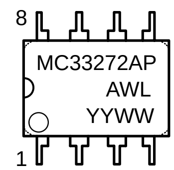
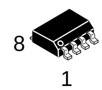
MARKING DIAGRAMS

DUAL

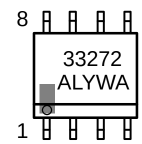


PDIP−8
P SUFFIX
CASE 626

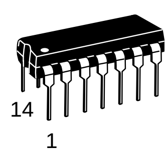




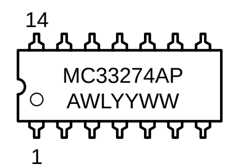
SOIC−8
D SUFFIX
CASE 751

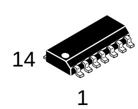


QUAD

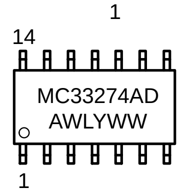


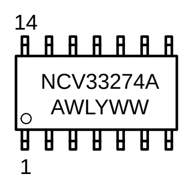
PDIP−14
P SUFFIX
CASE 646





SOIC−14
D SUFFIX
CASE 751A





A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

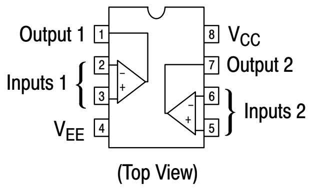
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

PIN CONNECTIONS

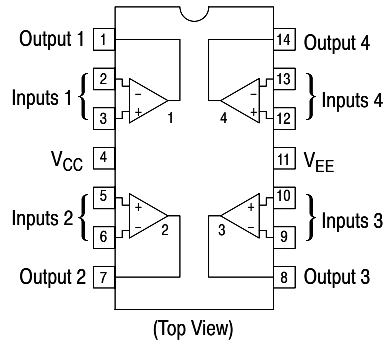
DUAL

CASE 626/751



QUAD

CASE 646/751A



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC} to V_{EE}	+36	V
Input Differential Voltage Range	V_{IDR}	Note 1	V
Input Voltage Range	V_{IR}	Note 1	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	−60 to +150	°C
ESD Protection at Any Pin − Human Body Model − Machine Model	V_{esd}	 2000 200	V
Maximum Power Dissipation	P_D	Note 2	mW
Operating Temperature Range MC33272A, MC33274A NCV33274A	T_A	−40 to +85 −40 to +125	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Either or both input voltages should not exceed V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see Figure 2).

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V)	3	$\|V_{IO}\|$				mV
(V_{CC} = +15 V, V_{EE} = −15 V)						
T_A = +25°C			−	0.1	1.0	
T_A = −40° to +85°C			−	−	1.8	
T_A = −40° to +125°C (NCV33274A)			−	−	3.5	
(V_{CC} = 5.0 V, V_{EE} = 0)						
T_A = +25°C			−	−	2.0	
Average Temperature Coefficient of Input Offset Voltage R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V, T_A = −40° to +125°C	3	$\Delta V_{IO}/\Delta T$	−	2.0	−	μV/°C
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	4, 5	I_{IB}				nA
T_A = +25°C			−	300	650	
T_A = T_{low} to T_{high}			−	−	800	
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)		$\|I_{IO}\|$				nA
T_A = +25°C			−	3.0	65	
T_A = T_{low} to T_{high}			−	−	80	
Common Mode Input Voltage Range (ΔV_{IO} = 5.0 mV, V_O = 0 V) T_A = +25°C	6	V_{ICR}	V_{EE} to (V_{CC} −1.8)			V
Large Signal Voltage Gain (V_O = 0 V to 10 V, R_L = 2.0 kΩ)	7	A_{VOL}				dB
T_A = +25°C			90	100	−	
T_A = T_{low} to T_{high}			86	−	−	
Output Voltage Swing (V_{ID} = ±1.0 V)	8, 9, 12					V
(V_{CC} = +15 V, V_{EE} = −15 V)						
R_L = 2.0 kΩ		V_O+	13.4	13.9	−	
R_L = 2.0 kΩ		V_O-	−	−13.9	−13.5	
R_L = 10 kΩ		V_O+	13.4	14	−	
R_L = 10 kΩ		V_O-	−	−14.7	−14.1	
(V_{CC} = 5.0 V, V_{EE} = 0 V)	10, 11					
R_L = 2.0 kΩ		V_{OL}	−	−	0.2	
R_L = 2.0 kΩ		V_{OH}	3.7	−	5.0	
Common Mode Rejection (V_{in} = +13.2 V to −15 V)	13	CMR	80	100	−	dB
Power Supply Rejection V_{CC}/V_{EE} = +15 V/ −15 V, +5.0 V/ −15 V, +15 V/ −5.0 V	14, 15	PSR	80	105	−	dB
Output Short Circuit Current (V_{ID} = 1.0 V, Output to Ground)	16	I_{SC}				mA
Source			+25	+37	−	
Sink			−25	−37	−	
Power Supply Current Per Amplifier (V_O = 0 V)	17	I_{CC}				mA
(V_{CC} = +15 V, V_{EE} = −15 V)						
T_A = +25°C			−	2.15	2.75	
T_A = T_{low} to T_{high}			−	−	3.0	
(V_{CC} = 5.0 V, V_{EE} = 0 V)						
T_A = +25°C			−	−	2.75	

3. MC33272A, MC33274A T_{low} = −40°C T_{high} = +85°C
NCV33274A T_{low} = −40°C T_{high} = +125°C

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 2.0 kΩ, C_L = 100 pF, A_V = +1.0 V)	18, 33	SR	8.0	10	−	V/μs
Gain Bandwidth Product (f = 100 kHz)	19	GBW	17	24	−	MHz
AC Voltage Gain (R_L = 2.0 kΩ, V_O = 0 V, f = 20 kHz)	20, 21, 22	A_{VO}	−	65	−	dB
Unity Gain Bandwidth (Open Loop)		BW	−	5.5	−	MHz
Gain Margin (R_L = 2.0 kΩ, C_L = 0 pF)	23, 24, 26	A_m	−	12	−	dB
Phase Margin (R_L = 2.0 kΩ, C_L = 0 pF)	23, 25, 26	ϕ_m	−	55	−	Deg
Channel Separation (f = 20 Hz to 20 kHz)	27	CS	−	−120	−	dB
Power Bandwidth (V_O = 20 V_{pp}, R_L = 2.0 kΩ, THD ≤ 1.0%)		BW_P	−	160	−	kHz
Total Harmonic Distortion (R_L = 2.0 kΩ, f = 20 Hz to 20 kHz, V_O = 3.0 V_{rms}, A_V = +1.0)	28	THD	−	0.003	−	%
Open Loop Output Impedance (V_O = 0 V, f = 6.0 MHz)	29	$\lvert Z_O \rvert$	−	35	−	Ω
Differential Input Resistance (V_{CM} = 0 V)		R_{in}	−	16	−	MΩ
Differential Input Capacitance (V_{CM} = 0 V)		C_{in}	−	3.0	−	pF
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1.0 kHz)	30	e_n	−	18	−	$nV/\sqrt{Hz}$
Equivalent Input Noise Current (f = 1.0 kHz)	31	i_n	−	0.5	−	$pA/\sqrt{Hz}$

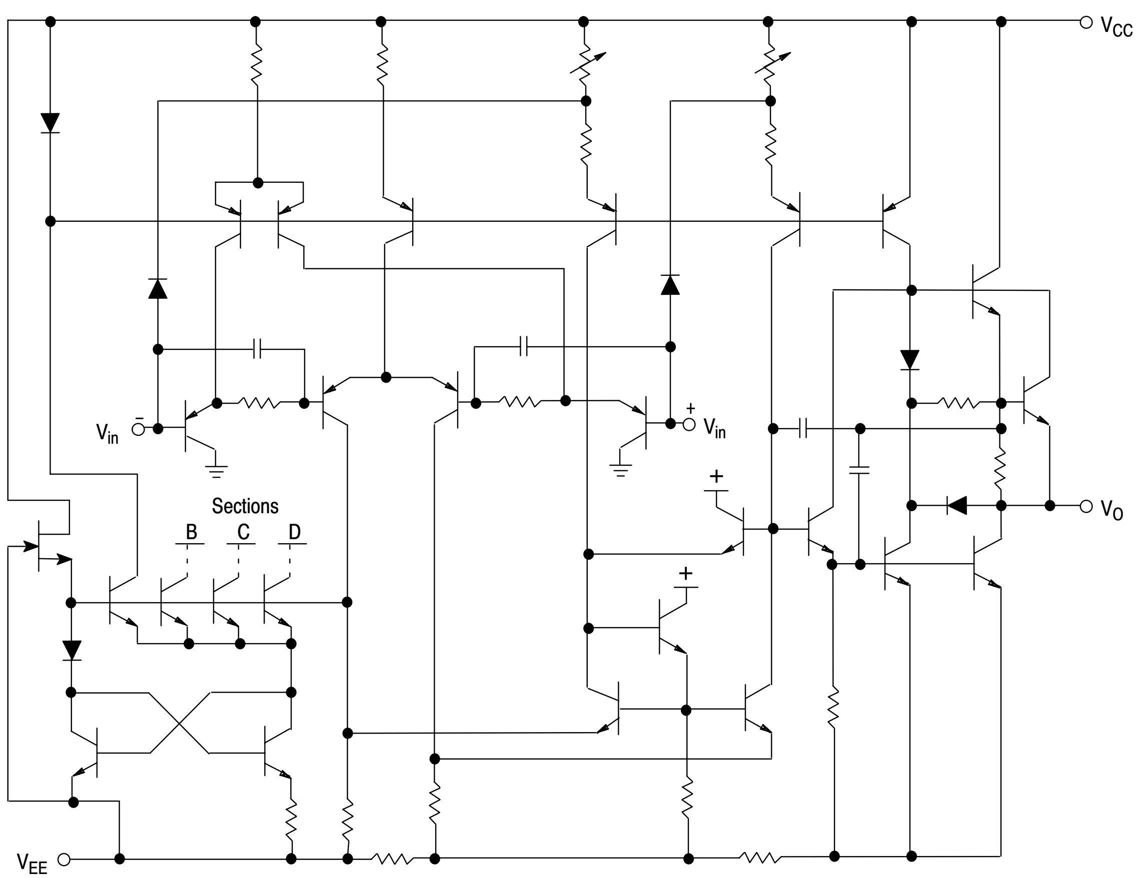


Figure 1. Equivalent Circuit Schematic
(Each Amplifier)

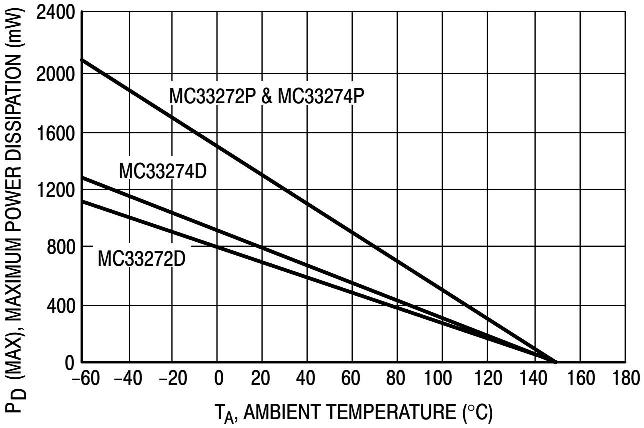


Figure 2. Maximum Power Dissipation versus Temperature

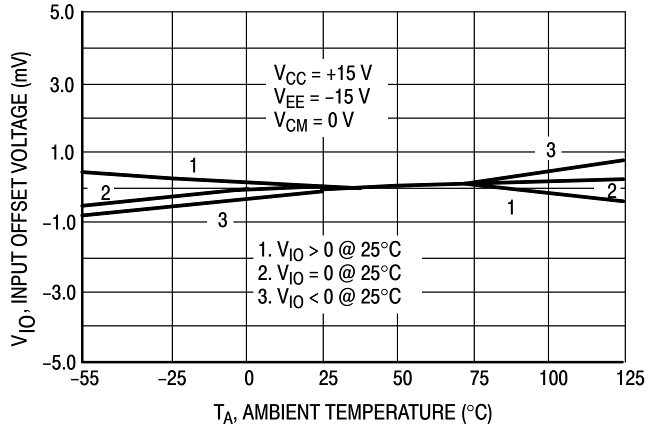


Figure 3. Input Offset Voltage versus Temperature for Typical Units

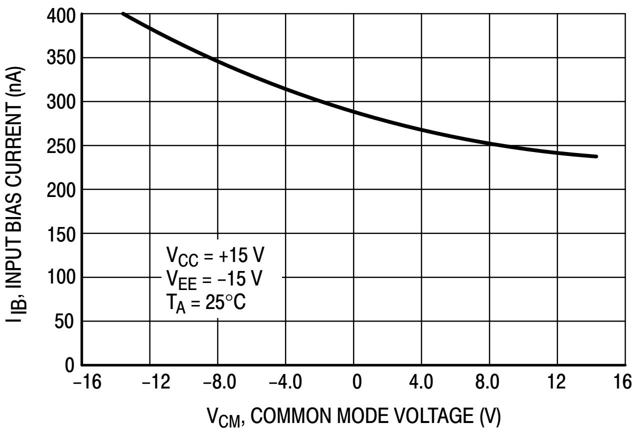


Figure 4. Input Bias Current versus Common Mode Voltage

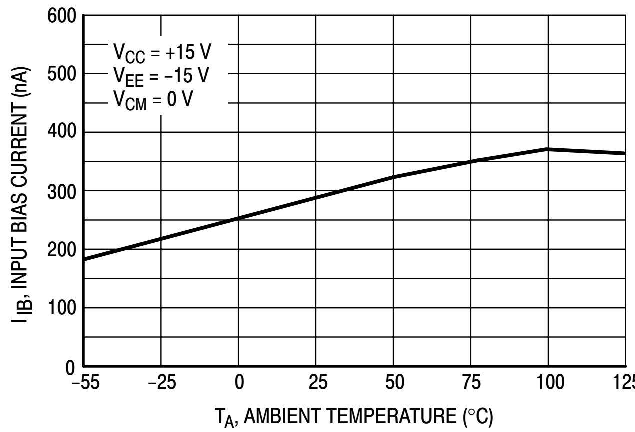


Figure 5. Input Bias Current versus Temperature

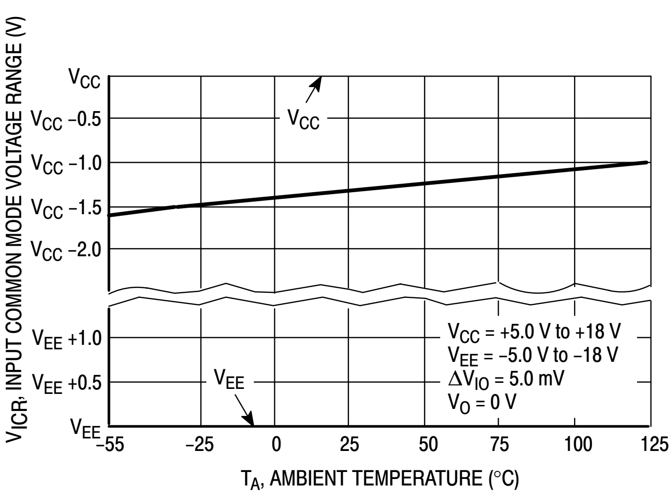


Figure 6. Input Common Mode Voltage Range versus Temperature

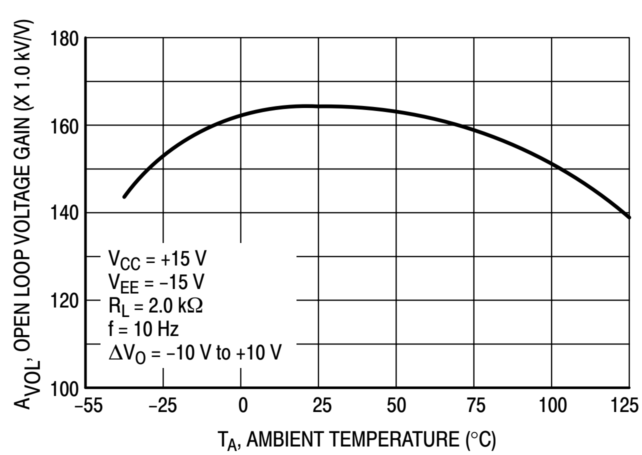


Figure 7. Open Loop Voltage Gain versus Temperature

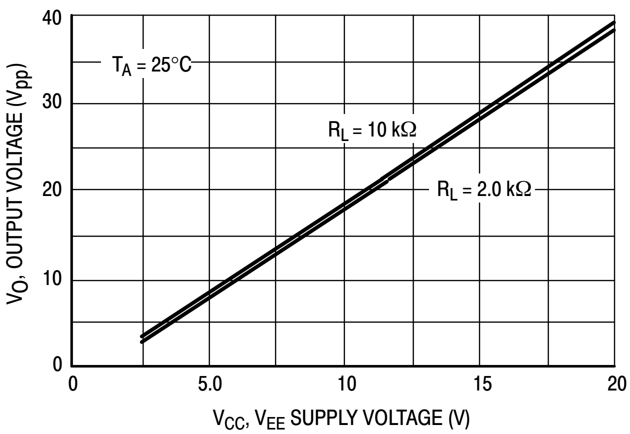


Figure 8. Split Supply Output Voltage Swing versus Supply Voltage

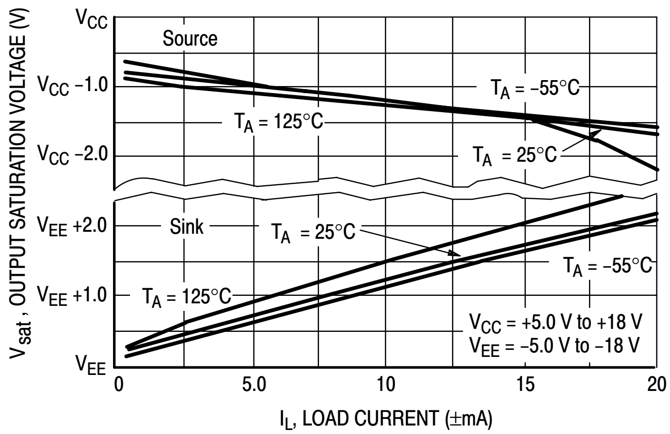


Figure 9. Split Supply Output Saturation Voltage versus Load Current

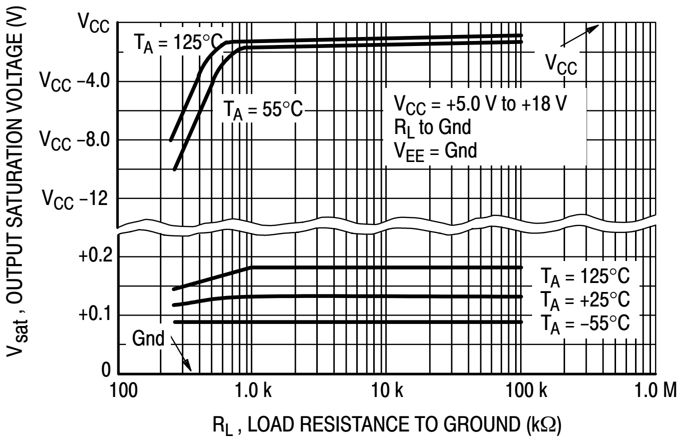


Figure 10. Single Supply Output Saturation Voltage versus Load Resistance to Ground

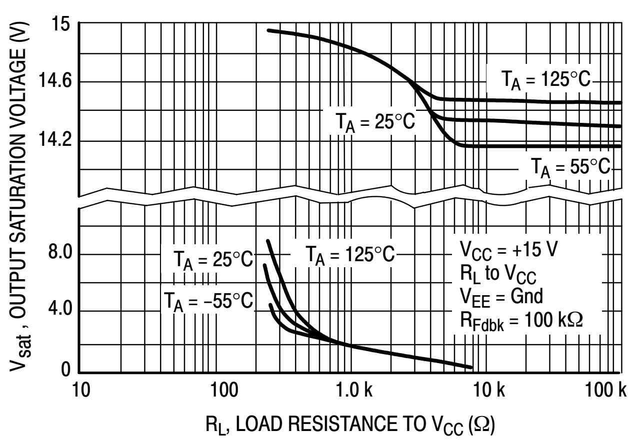


Figure 11. Single Supply Output Saturation Voltage versus Load Resistance to V_{CC}

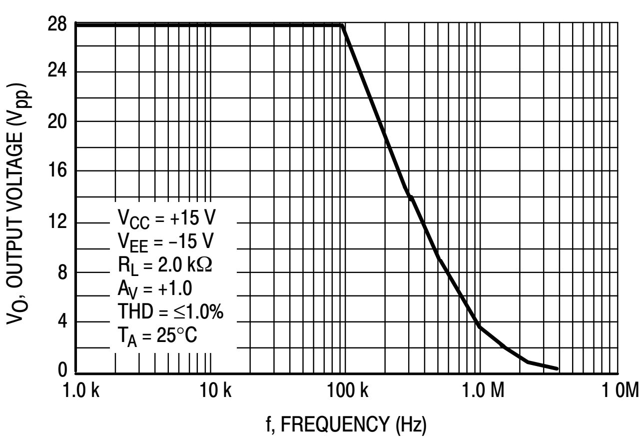


Figure 12. Output Voltage versus Frequency

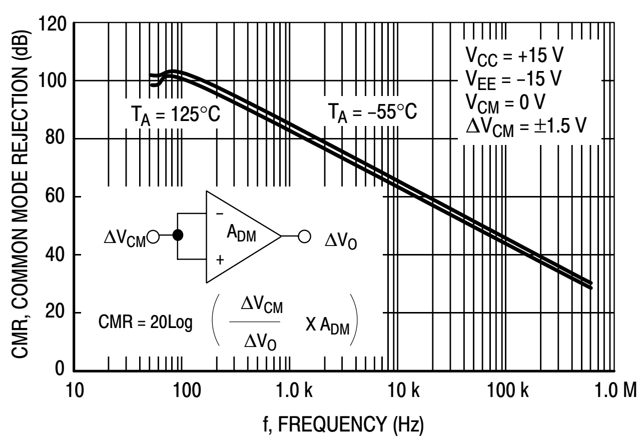


Figure 13. Common Mode Rejection versus Frequency

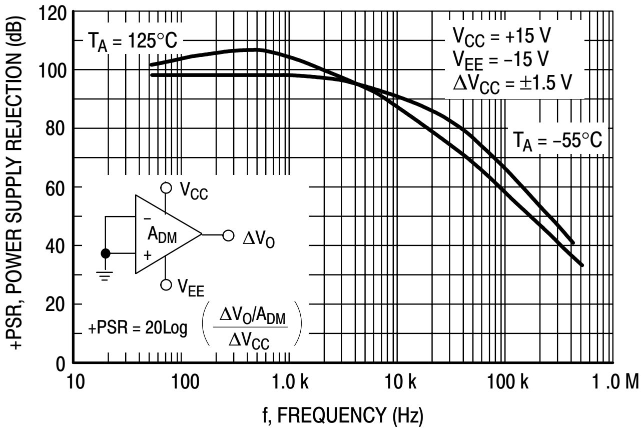


Figure 14. Positive Power Supply Rejection versus Frequency

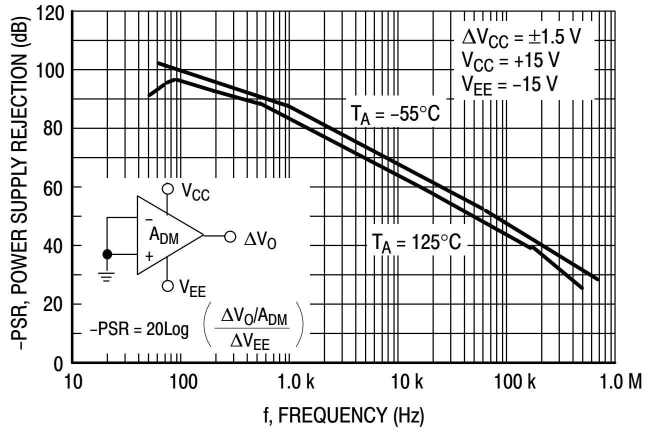


Figure 15. Negative Power Supply Rejection versus Frequency

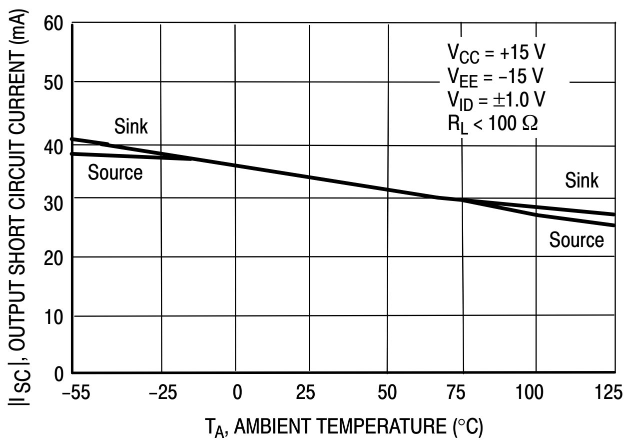


Figure 16. Output Short Circuit Current versus Temperature

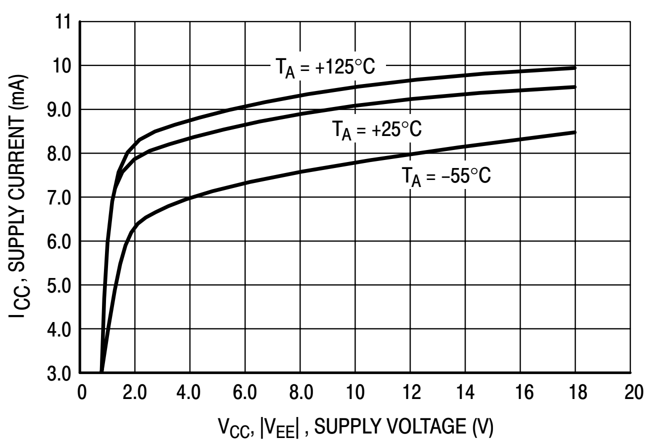


Figure 17. Supply Current versus Supply Voltage

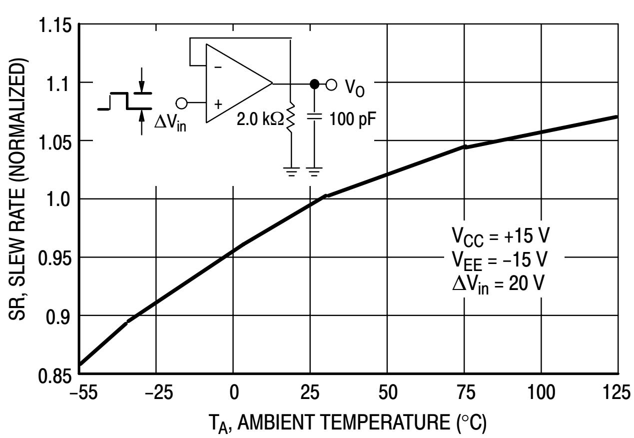


Figure 18. Normalized Slew Rate versus Temperature

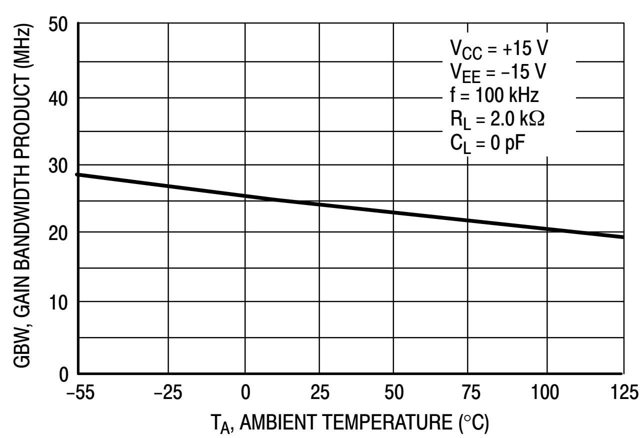


Figure 19. Gain Bandwidth Product versus Temperature

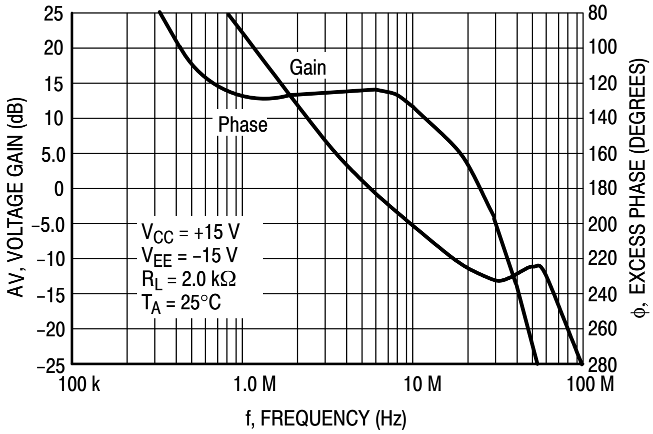


Figure 20. Voltage Gain and Phase versus Frequency

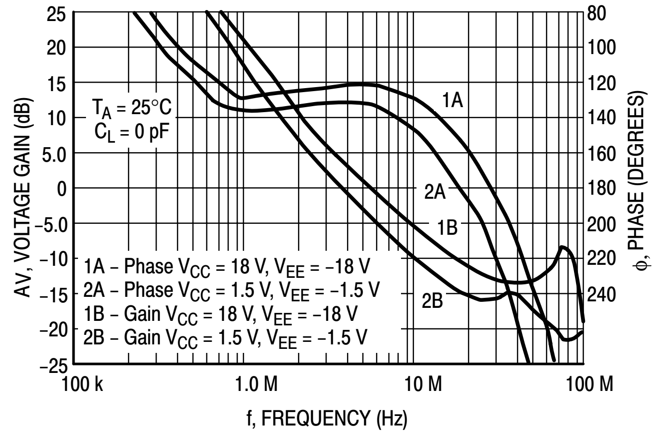


Figure 21. Gain and Phase versus Frequency

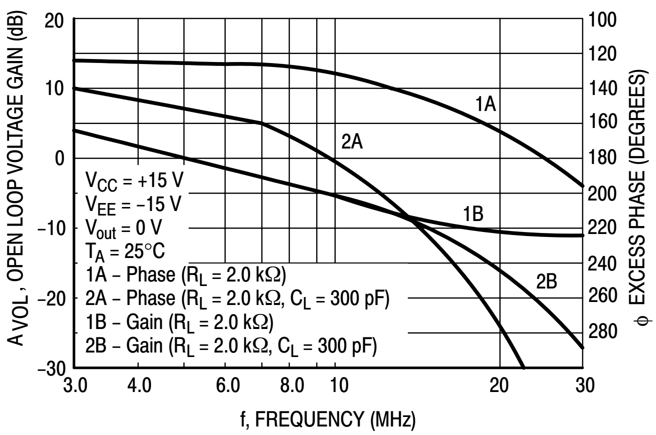


Figure 22. Open Loop Voltage Gain and Phase versus Frequency

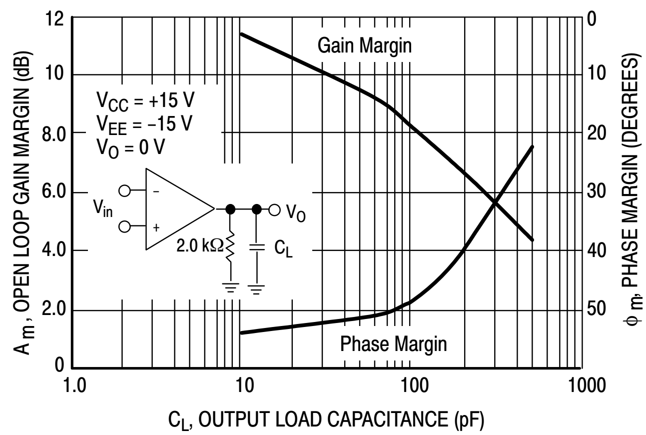


Figure 23. Open Loop Gain Margin and Phase Margin versus Output Load Capacitance

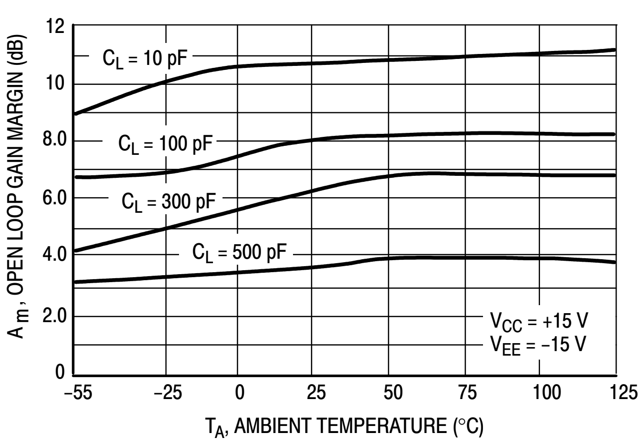


Figure 24. Open Loop Gain Margin versus Temperature

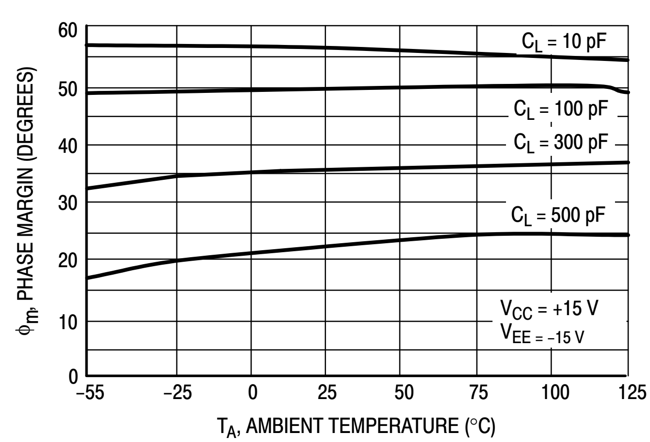


Figure 25. Phase Margin versus Temperature

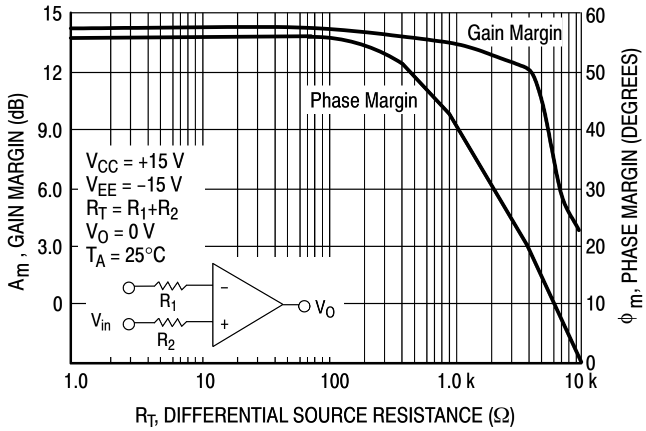


Figure 26. Phase Margin and Gain Margin versus Differential Source Resistance

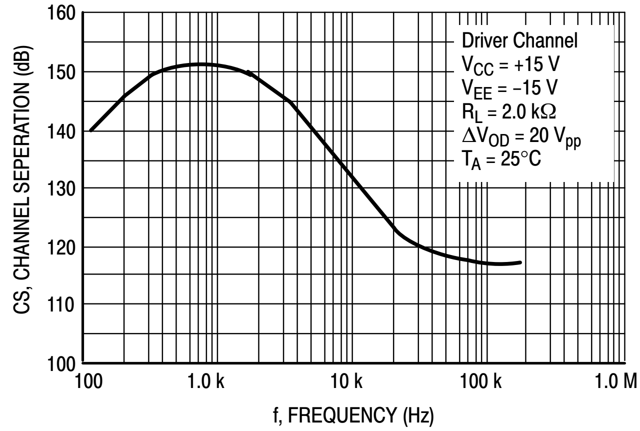


Figure 27. Channel Separation versus Frequency

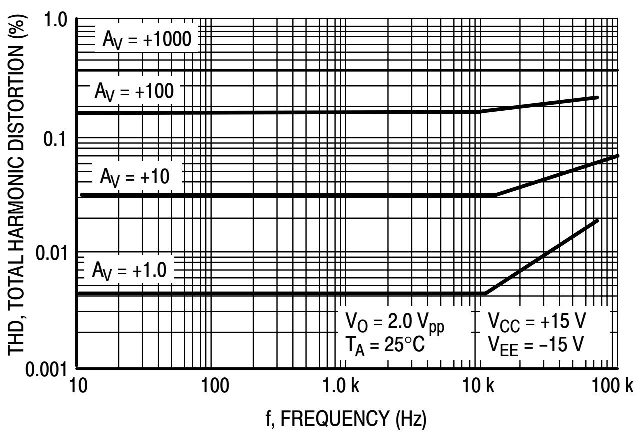


Figure 28. Total Harmonic Distortion versus Frequency

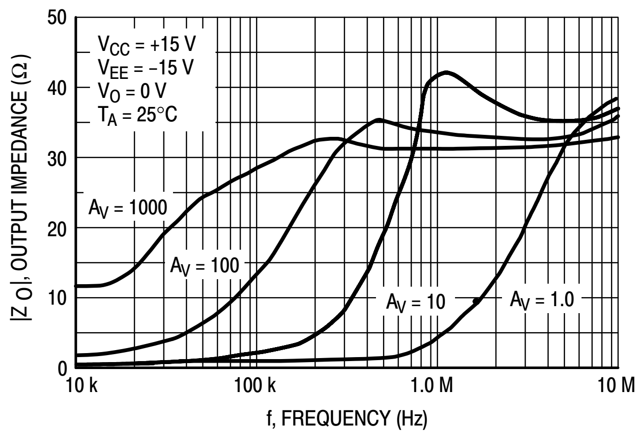


Figure 29. Output Impedance versus Frequency

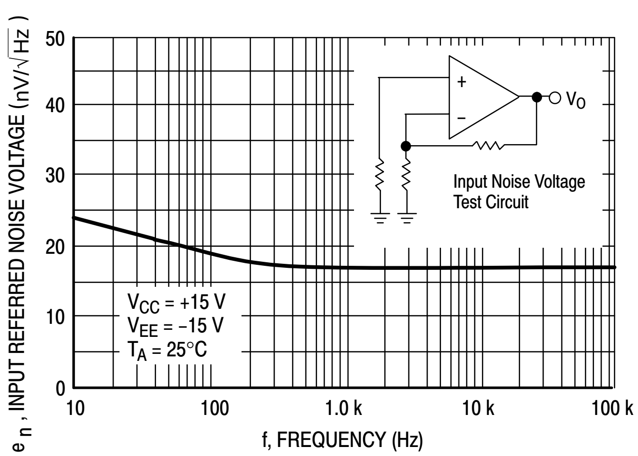


Figure 30. Input Referred Noise Voltage versus Frequency

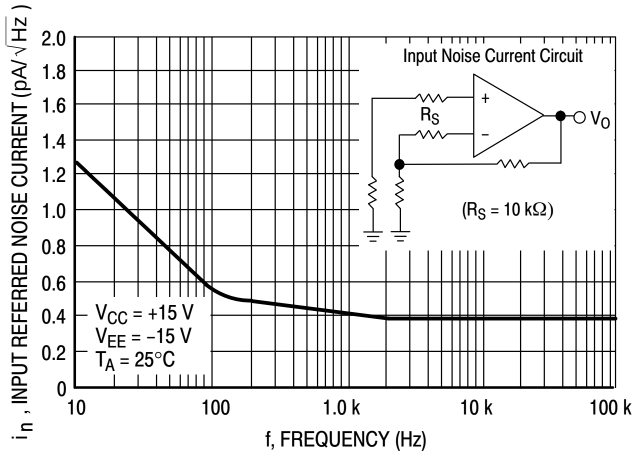


Figure 31. Input Referred Noise Current versus Frequency

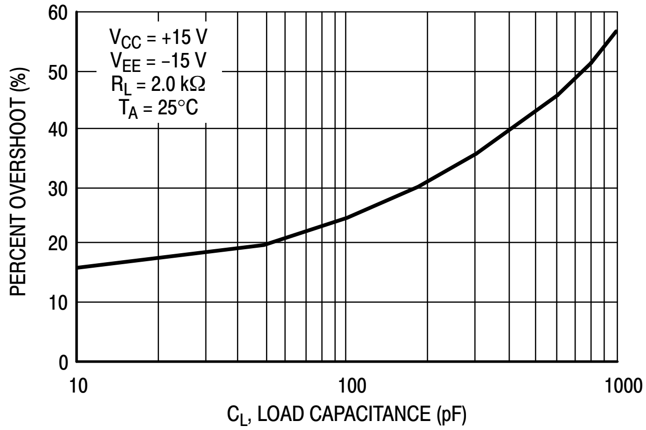


Figure 32. Percent Overshoot versus Load Capacitance

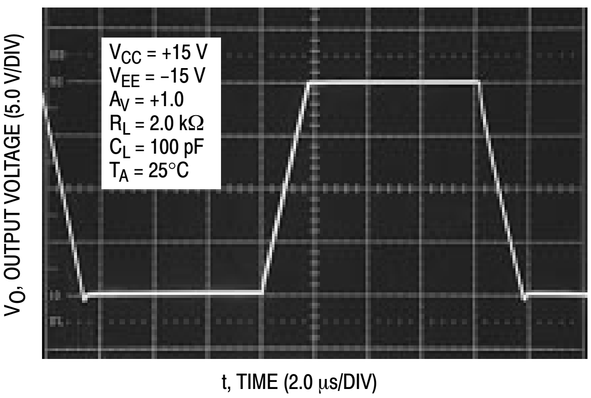


Figure 33. Non−inverting Amplifier Slew Rate for the MC33274

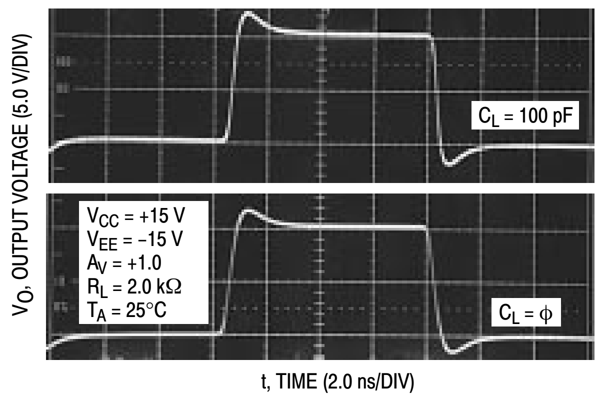


Figure 34. Non−inverting Amplifier Overshoot for the MC33274

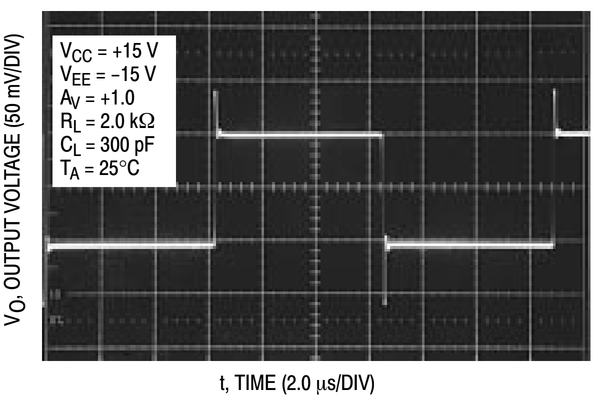


Figure 35. Small Signal Transient Response for MC33274

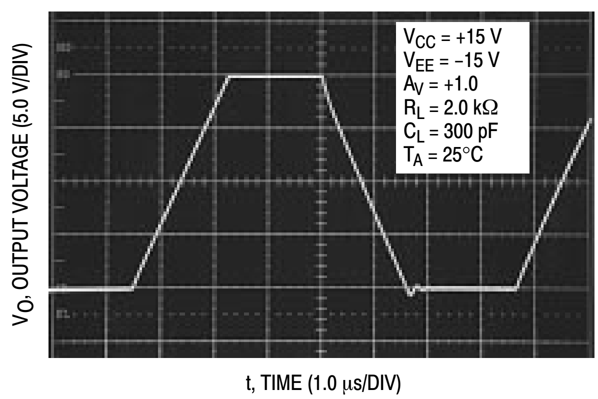


Figure 36. Large Signal Transient Response for MC33274

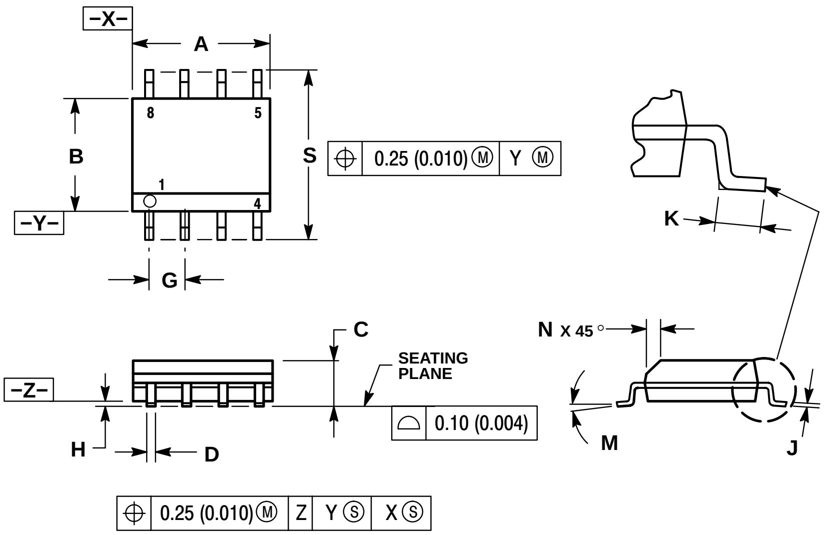
ORDERING INFORMATION

Device	Package	Shipping†
MC33272AD	SOIC−8	98 Units / Rail
MC33272ADG	SOIC−8 (Pb−Free)	98 Units / Rail
MC33272ADR2	SOIC−8	2500 Tape & Reel
MC33272ADR2G	SOIC−8 (Pb−Free)	2500 Tape & Reel
MC33272AP	PDIP−8	50 Units / Rail
MC33272APG	PDIP−8 (Pb−Free)	50 Units / Rail
MC33274AD	SOIC−14	55 Units / Rail
MC33274AD	SOIC−14	55 Units / Rail
MC33274ADR2	SOIC−14	2500 Tape & Reel
MC33274ADR2G	SOIC−14 (Pb−Free)	2500 Tape & Reel
MC33274AP	PDIP−14	25 Units / Rail
NCV33274ADG*	SOIC−14 (Pb−Free)	2500 Tape & Reel
NCV33274ADR2*	SOIC−14	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NCV devices are automotive qualified.

PACKAGE DIMENSIONS

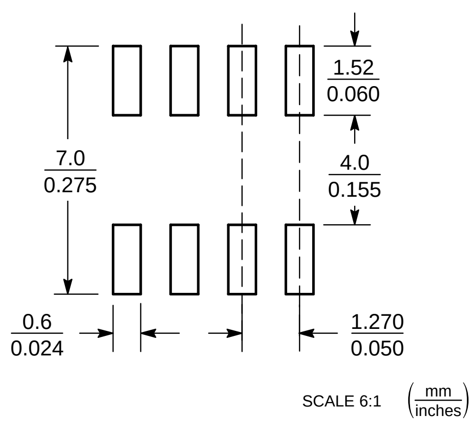
SOIC−8
D SUFFIX
CASE 751−07
ISSUE AD



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

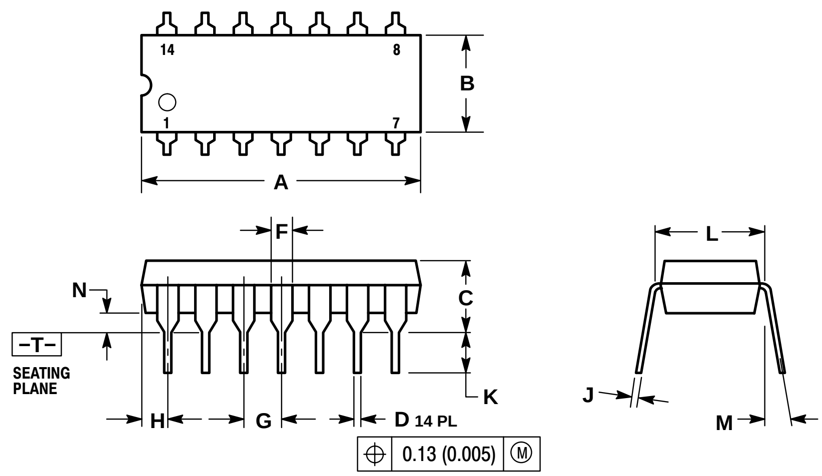
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

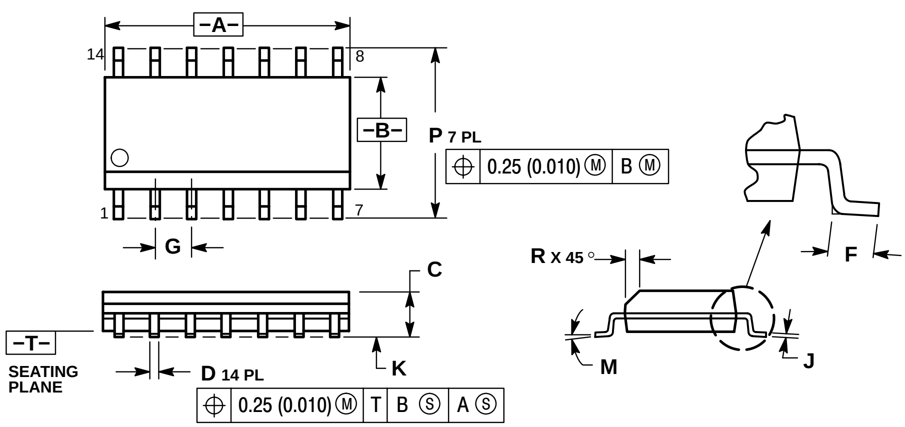
PDIP−14
P SUFFIX
CASE 646−06
ISSUE M



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	18.80
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---	10°	---	10°
N	0.015	0.039	0.38	1.01

SOIC−14
D SUFFIX
CASE 751A−03
ISSUE G

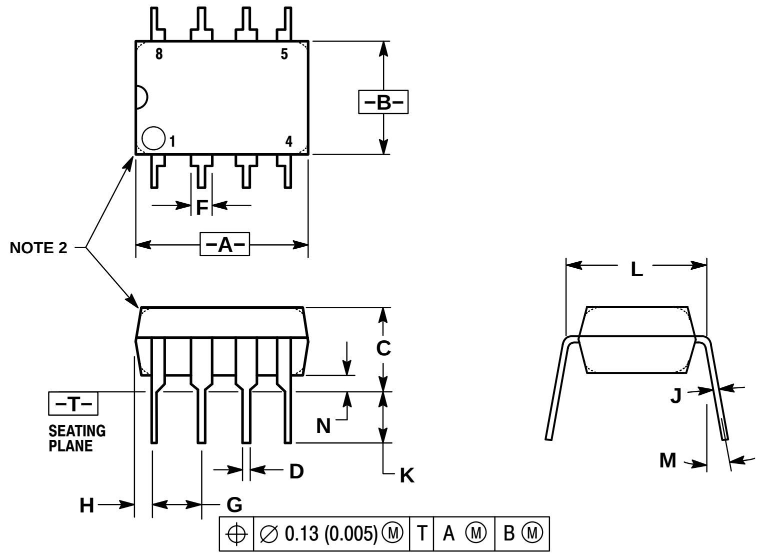


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

PACKAGE DIMENSIONS

PDIP−8
P SUFFIX
CASE 626−05
ISSUE L



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

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