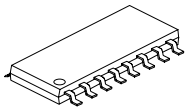
L2572

LINEAR INTEGRATED CIRCUIT

WIDEBAND PLL FM DEMODULATOR



SOP-16

*Pb-free plating product number: L2572L

■ DESCRIPTION

As a wideband PLL FM demodulator, the UTC L2572 is intended for application in satellite tuners primarily.

The device includes all the necessary elements, with external oscillator sustaining network and the exception of loop feedback components, to form a PLL system operating at frequencies up to 800MHz completely.

An AFC with window adjust (whose output signal can be used to correct for any frequency drift at the head end local oscillator) is provided.

■ FEATURES

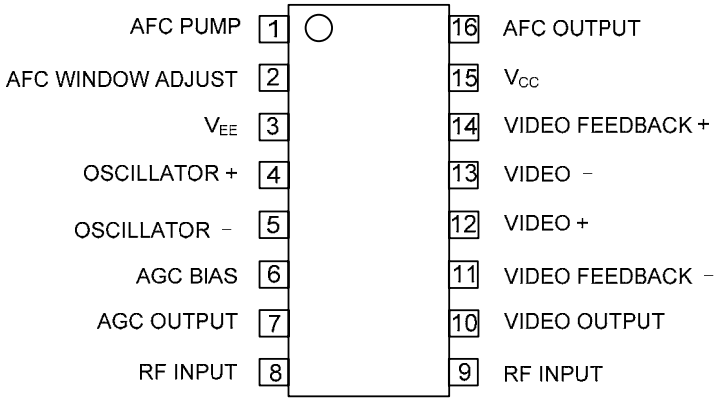
* Constant voltage and constant current control
* Single chip PLL system for wideband FM demodulation
* Simple low component count application
* Allows for application of threshold extension
* Fully balanced low radiation design
* High operating input sensivity
* Improved VCO stability with variations in supply or temperature
* AGC detect and bias adjust
* 75Ω video output drive with low distortion levels
* Dynamic self biasing analog AFC
* Full ESD Protection

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Normal	Lead Free Plating		
L2572-S16-R	L2572L-S16-R	SOP-16	Tape Reel
L2572-S16-T	L2572L-S16-T	SOP-16	Tube

L2572L-S16-R (1)Packing Type (2)Package Type (3)Lead Plating	(1) R: Tape Reel, T: Tube (2) S16: SOP-16 (3) L: Lead Free Plating, Blank: Pb/Sn

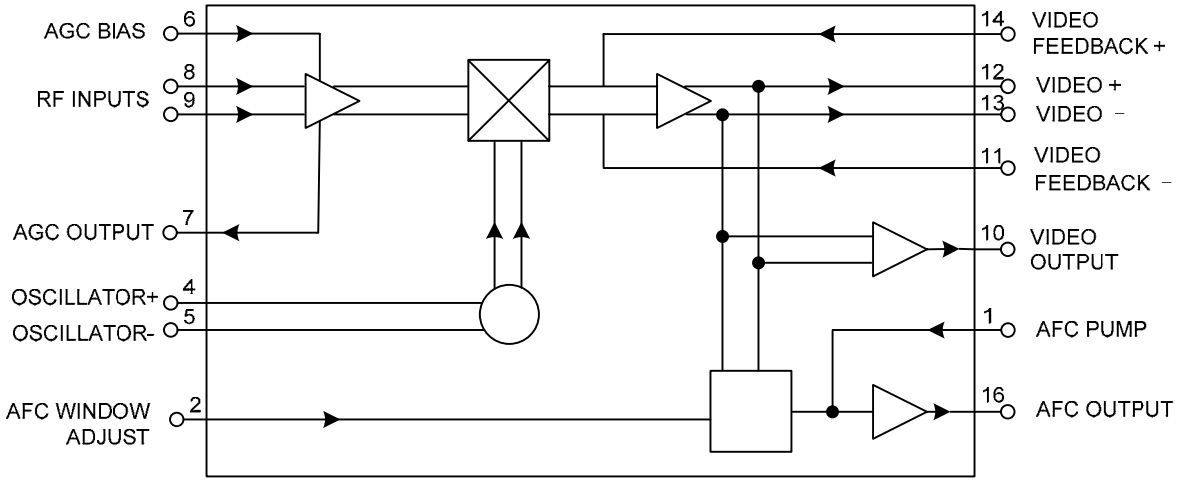
■ PIN CONFIGURATION



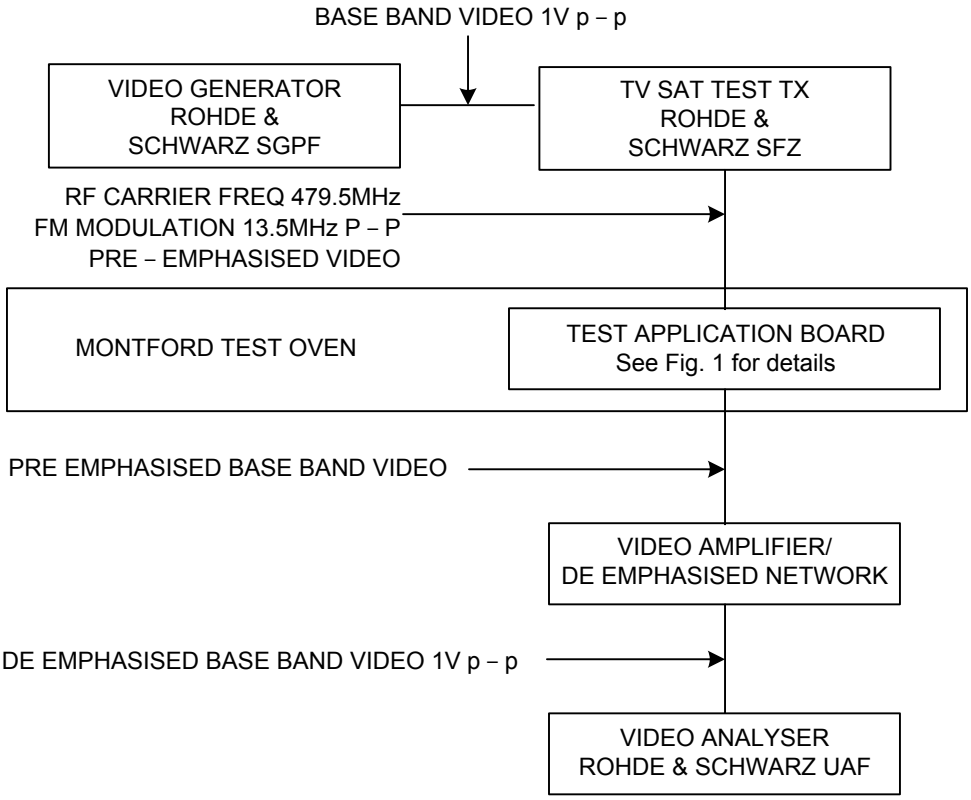
■ PIN DESCRIPTION

PIN NO.	PIN NAME	I/O	DESCRIPTION
1	AFC PUMP	I	Current pump, integrating the signal pulses into a DC voltage
2	AFC WINDOW ADJUST	I	Set the AFC deadband voltages corresponding the frequency
3	V_{EE}		GND
4	OSCILLATOR+	I	Oscillator positive signal
5	OSCILLATOR-	I	Oscillator negative signal
6	AGC BIAS	I	Set the AGC bias
7	AGC OUTPUT	O	Output AGC DC voltage
8	RF INPUT	I	Input signal
9	RF INPUT	I	Input signal
10	VIDEO OUTPUT	O	Output video signal
11	VIDEO FEEDBACK-	I	Feedback the video negative signal
12	VIDEO+	O	Video positive signal
13	VIDEO-	O	Video negative signal
14	VIDEO FEEDBACK+	I	Feedback the video positive signal
15	V_{CC}		Input V_{CC}
16	AFC OUTPUT	O	Output AFC DC voltage

■ BLOCK DIAGRAM



TEST CONFIGURATION



Using the above test configuration the video drive characteristics measurements were made. In the Electrical Characteristics Table the maximum figures recorded coincide with extremes of supply voltage and high temperatures. There's no adjustment to the recorded figures has been made to compensate for the effects of temperature on the external components of the application test board, in the varactor diodes particularly. Attention to temperature compensation of the external circuitry will result in performance figures closer to the stated typical figures if operation of the device at high ambient temperatures is envisaged.

■ ABSOLUTE MAXIMUM RATINGS (V_{EE}=0V)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.3~7	V
RF Input Voltage	$V_{IN(RF)}$	2.5	V_{P-P}
RF Input DC Offset	$V_{IN\ RF(OFF)}$	-0.3~V_{CC}+0.3	V
Oscillator ± DC Offset	$V_{OSC(OFF)}$	-0.3~V_{CC}+0.3	V
Video ± DC Offset	$V_{VDO(OFF)}$	-0.3~V_{CC}+0.3	V
Video Feedback ± DC Offset		-0.3~V_{CC}+0.3	V
Video Output DC Offset		-0.3~V_{CC}+0.3	V
AFC Pump DC Offset	$V_{AFC(OFF)}$	-0.3~V_{CC}+0.3	V
AFC Disable DC Offset		-0.3~V_{CC}+0.3	V
AFC Deadband DC Offset		-0.3~V_{CC}+0.3	V
AGC Bias DC Offset	$V_{AGC(OFF)}$	-0.3~V_{CC}+0.3	V
AGC Output DC Offset		-0.3~V_{CC}+0.3	V
Power Dissipation (at 5.5V)	P_D	250	mW
ESD Protection - Pin 1 to 15	ESD	2	kV
ESD Protection - Pin 16		1.7	kV
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	-55~125	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

Parameter	SYMBOL	RATINGS	Unit
Junction to Ambient	Θ_{JA}	111	°C/W
Junction to Case	Θ_{JC}	41	°C/W

■ ELECTRICAL CHARACTERISTICS

(Ta = -20°C~+80°C, V_{CC} = +4.5V ~ +5.5V. Either design or production test guarantee the electrical characteristics. Unless otherwise stated they apply within the specified ambient temperature and supply voltage.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current	V_{CC}			36	40	mA
Operating Frequency	F_{OPR}		300		800	MHz
Input Sensitivity		Preamp limiting		-40		dBm
Input Overload			0			dBm
VCO Sensitivity (dF/dV)		Refer to Fig. 1	25	32	39	MHz/V
VCO linearity		Refer to Fig. 1 with13.5MHz p-p deviation		25		%
VCO Supply Stability		See note 5		2.0		MHz/V
VCO Temperature Stability		See note 5		20		KHz/°C
Phase Detector Gain		Differential loop filter Single ended loop filter		0.5 0.25		V/rad
Loop Amplifier Input Impedance	R_{IN}		450	570	700	Ω
Loop Amplifier Output Impedance	$R_{OUT(LOOP)}$			25		Ω
Loop Amplifier Open Loop Gain				38		dB
Loop Amplifier Gain Bandwidth Product	B_W			240		MHz
Loop Amplifier Output Swing					1.2	Vp-p
Video Drive Output Impedance	$R_{OUT(VIDEO)}$		55	75	95	Ω

■ ELECTRICAL CHARACTERISTICS(Cont.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
VIDEO DRIVE						
Luminance Nonlinearity		1KΩ load, See note 3 and 4		1.9	5	%
Differential Gain		75KΩ load, See note 3 and 4		0.5	2.5	%
Differential Phase		75KΩ load, See note 3 and 4		1.0	3	Degree
Intermodulation		See notes 1, 3 and 4			-40	dB
Signal/noise		1KΩ load, See note 2 and 4	66	72		dB
Tilt		1KΩ load, See note 3 and 4		0.3	3	%
Baseline Distortion		1KΩ load, See note 3 and 4		0.4	2	%
AGC Output Current	I_{OUT}	Maximum load voltage drop 2V	10		400	μA
AGC Bias Current	I_{BIAS}		0		250	μA
AFC Window Current		400μA gives 1.5V deadband window	0		400	μA
AFC Charge Pump Current				50		μA
AFC Leakage Current	I_{LEAK}	With charge pump disabled			10	μA
AFC Output Saturation Voltage	$V_{O(SAT)}$	AFC output enabled			0.4	V

Note 1. Input modulation's product f 1 at 4.43MHz, 13.5MHz p–p deviation and f 2 at 6MHz p–p deviation, (PAL chroma and sound subcarriers).

2. To output rms noise in 6MHz bandwidth with no input modulation, ratio of output video signal with input modulation at 1MHz, 13.5MHz p–p deviation.
3. Output voltage is 600mV pk–pk and input test signal pre–emphasised video 13.5MHz p–p deviation.
4. See page 4
5. Assuming ambient temperature of +20°C and operating frequency of 479.5MHz set with V_{CC} @ 5.0V. Only applies to application shown in Fig. 1 also refer to Fig. 4.

■ APPLICATION CIRCUIT

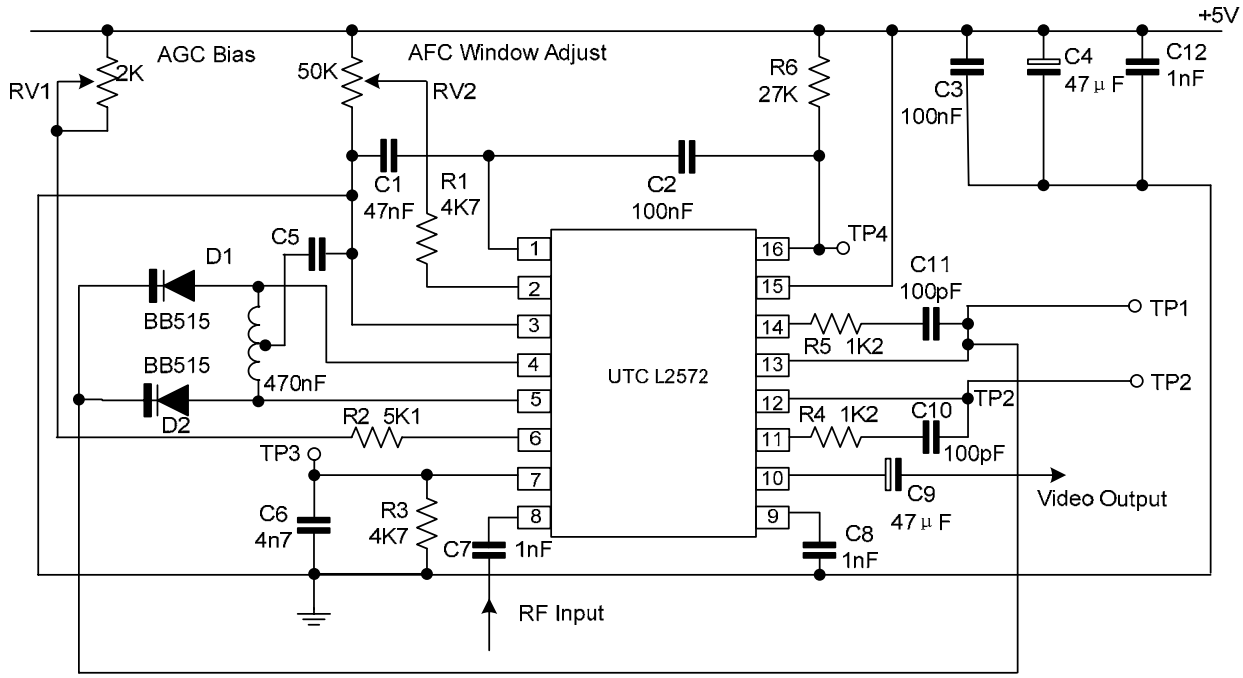


Fig. 1 Application Circuit

■ FUNCTIONAL DESCRIPTION

The UTC L2572 as optimized for application in satellite receiver systems and requiring a minimum external component count is a wideband PLL FM demodulator. It includes all the elements required to construct a phase locked loop circuit, with the exception of an AFC detector circuit for generation of error signal to correct for any frequency drift in the outdoor unit local oscillator, and tuning components for the local oscillator contains a block diagram and Fig. 1 contains the typical application.

Fig. 2-1 contains the internal pin connections

In applications the second satellite IF frequency of typically 479.5 or 402MHz is fed to the RF preamplifier normally, which depending on application and layout has a working sensitivity of typically -40 dBm. An RF level detect circuit, which generates an AGC signal that can be used for controlling the gain of the IF amplifier stages is contained in the preamplifier, so it can be maintaining a fixed level to the RF input of the UTC L2572, for optimum threshold performance. The AGC circuit's bias point can be adjusted to cater for device input power and variation in AGC line voltage requirement. Fig. 5 shows the typical AGC curves are shown in. That the device is recommended that be operated with an input signal between -30 and -35dBm. That can ensure optimum linearity and threshold performance, and when over the typical sensitivity of -40dBm can give a good safety margin.

The preamplifier's output is fed to the mixer section which is of balanced design for low radiation. In this stage the RF signal is mixed with which is generated by an on–board oscillator, the local oscillator frequency. The oscillator block is optimized for high linearity over the normal deviation range and uses an external varactor tuned sustaining network. Fig. 3 contains a typical frequency versus voltage characteristic for the oscillator. Fig.4 shows the typical stability that he loop output is designed to compensate for first order temperature variation effects.

The mixer's output is then fed to the loop amplifier around which feedback is applied to effect loop transfer characteristic. Feedback could be applied either in single ended or differential mode; both modes should give the same loop response if the appropriate phase detector gains are assumed in calculating loop filters.

The loop amplifier drives a 75Ω output impedance buffer amplifier, which could be connected to a 75Ω load and used to drive a high input impedance stage giving greater linearity and approximately 6dB higher demodulated signal output level too.

■ INTERNAL CIRCUITS

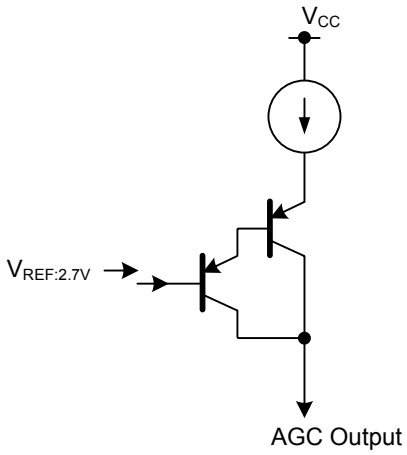


Fig. 2-1 AGC Output

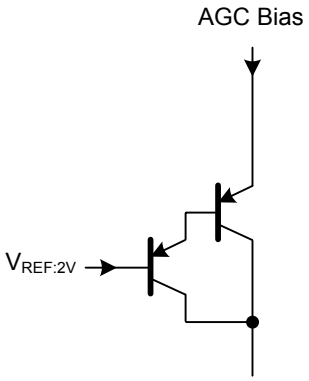


Fig. 2-2 AGC Bias Adjust

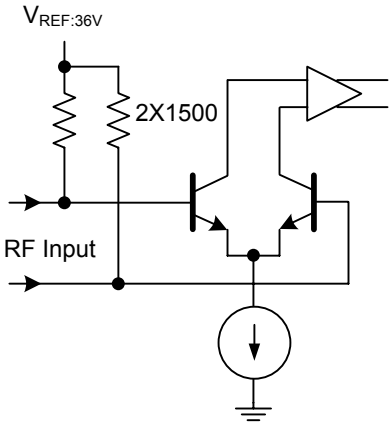


Fig. 2-3 RF Input

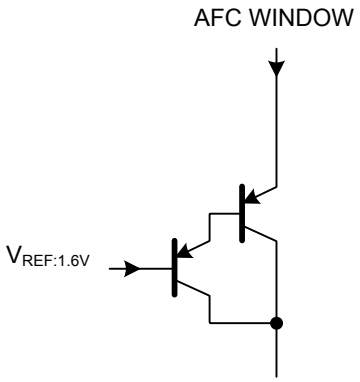


Fig. 2-4 AFC Window Adjust

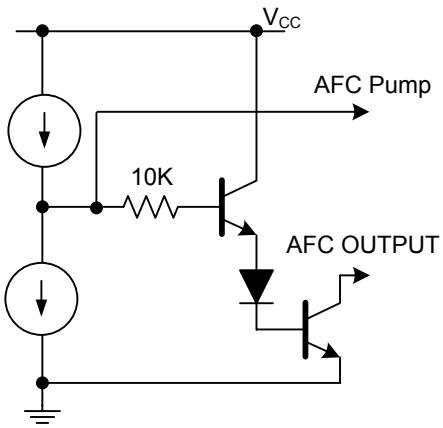


Fig. 2-5 AFC Output Stage

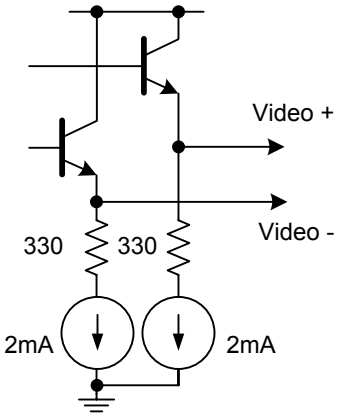


Fig. 2-6 Video Amp Output

■ INTERNAL CIRCUITS(Cont.)

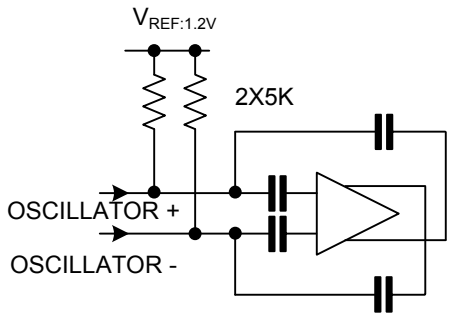


Fig. 2-7 Local Oscillator

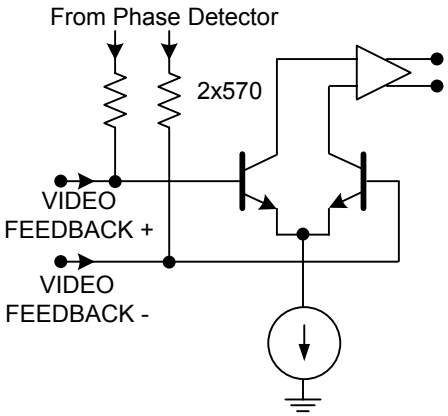


Fig. 2-8 Video amp feedback inputs

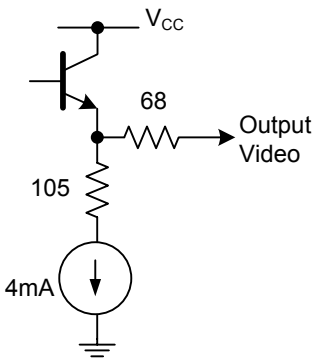


Fig. 2-9 Video Output Drive

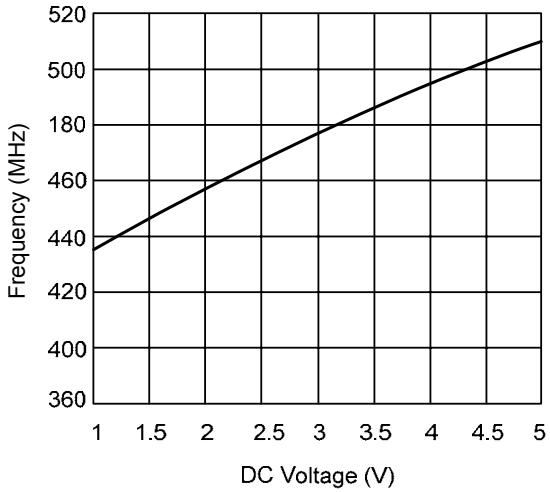


Fig. 3 Typical VCO Frequency vs. DC Control Voltage

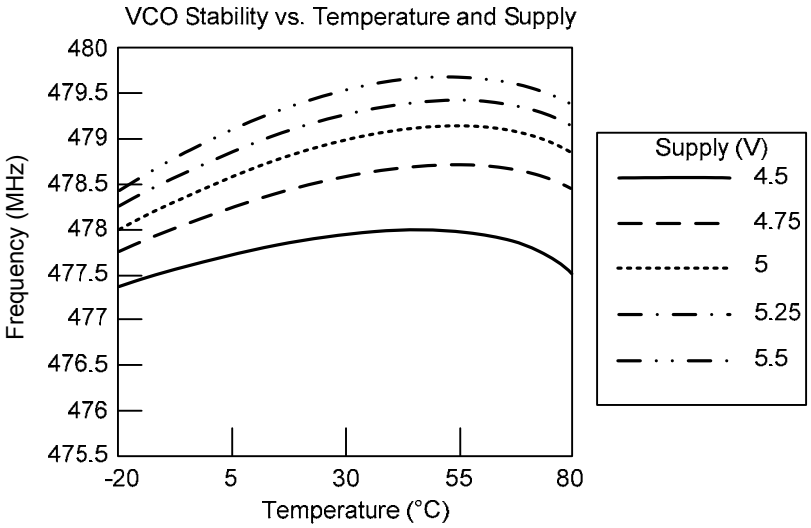


Fig. 4 VCO Centre Frequency Uncompensated Temperature Stability

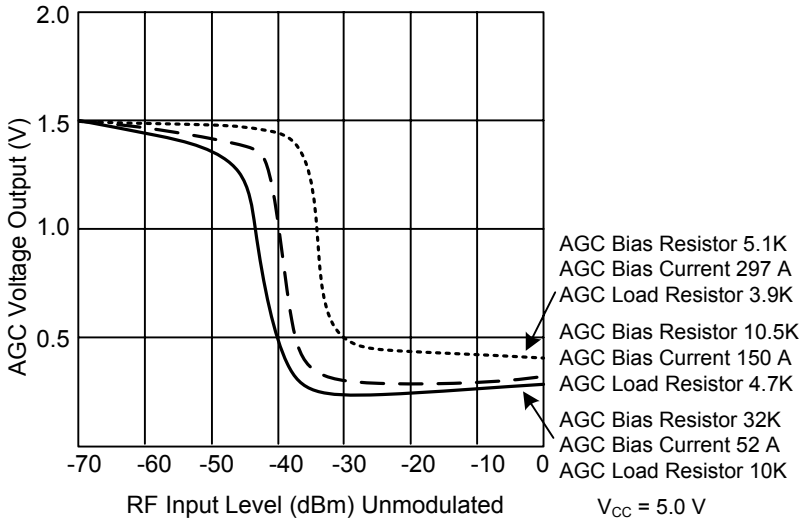
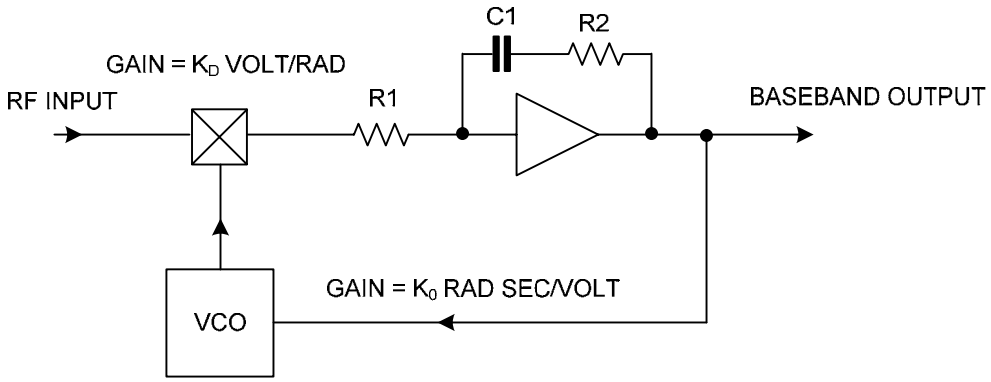


Fig.5 AGC Output Voltage for Differing Values of AGC Bias Resistor

■ DESIGN OF PLL LOOP PARAMETERS



The UTC L2572 is normally used as a type 1 second order loop and can be represented by the above diagram. For such a system the following parameters apply;

τ_1 = C1.R1
τ_2 = C1.R2
and

$$\tau_1 = \frac{K_0 K_D}{\omega_n^2}$$

$$\tau_2 = \frac{2\zeta}{\omega_n}$$

where:
K_0 is the VCO gain in radian seconds per volt
K_D is the phase detector gain in volts per radian
ω_n is the natural loop bandwidth
ξ is the loop damping factor
R1 is loop amplifier input impedance

Note: K_0 is dependant on sensitivity of VCO used.
K_D = 0.25V/rad single ended, 0.5V/rad differential

From these factors the loop 3dB bandwidth can be determined from the following expression;

$$\omega_{3dB}^2 = \omega_n^2(2\zeta^2+1) \pm \omega_n^2\sqrt{(2\zeta^2+1)^2+1}$$

Which approximates to $\omega_{3dB} = 2\omega_n$ when $\zeta = \frac{1}{\sqrt{2}}$

■ AFC FACILITY

An analog frequency error detect circuit, which generates DC voltage proportional to the integral of frequency error is contained in UTC L2572.As the incident RF is high then the AFC voltage increases, as low then the voltage decreases. ADC converts the AFC voltage can then be an to be read by the micro controller for frequency fine tuning.

Around the aligned frequency the AFC detect circuit contains a deadband centre. From zero window to approximately 25MHz width assuming an oscillator dF/dV of 15MHz/V the deadband can be adjusted. The AFC voltage does not integrate if the incident RF is within this window, except by component leakage.

With reference to Fig. 6; the demodulated video is fed to a dual comparator which can be compared with two reference voltages in normal operation, corresponding to the extremes of the deadband, or window. These voltages are variable and the window adjust input can set it.

Two digital outputs corresponding to voltages above or below the voltage window, or frequency above or below deadband can be produced by the comparators. These digital control signals can control a complimentary current source pump. The current signals are then fed to an amplifier's input. it is arranged as an integrator, so integrating the pulses into a DC voltage.

Both the current source and sink are disabled if the frequency is correctly aligned, therefore the DC output voltage can be constant. Due to component leakage there will be a small drift; the maximum drift can be calculated from here:

$$\frac{dV}{dt} = \frac{I}{2500.C} \quad \text{where} \quad I = \frac{Vcc}{R_{EXT}} \quad , \quad C = C_{EXT}$$

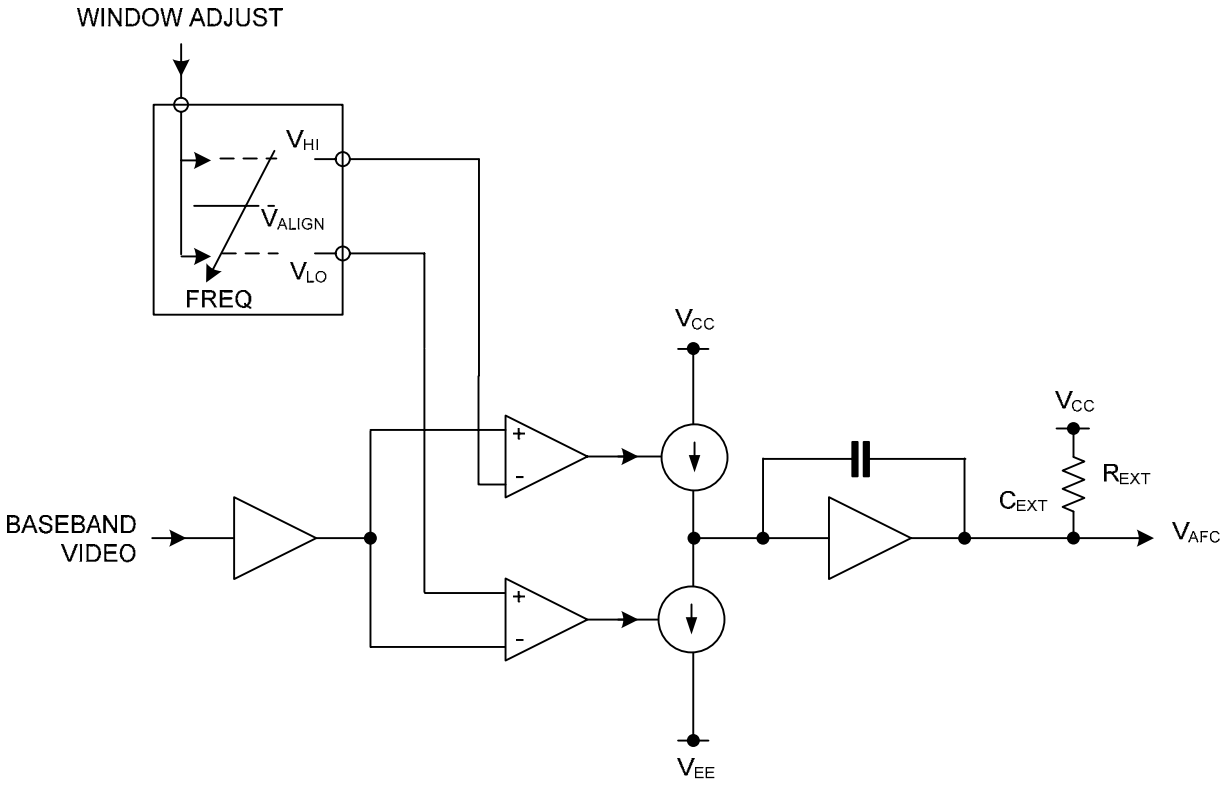


Fig. 6 AFC System Block Diagram