



### GENERAL DESCRIPTION



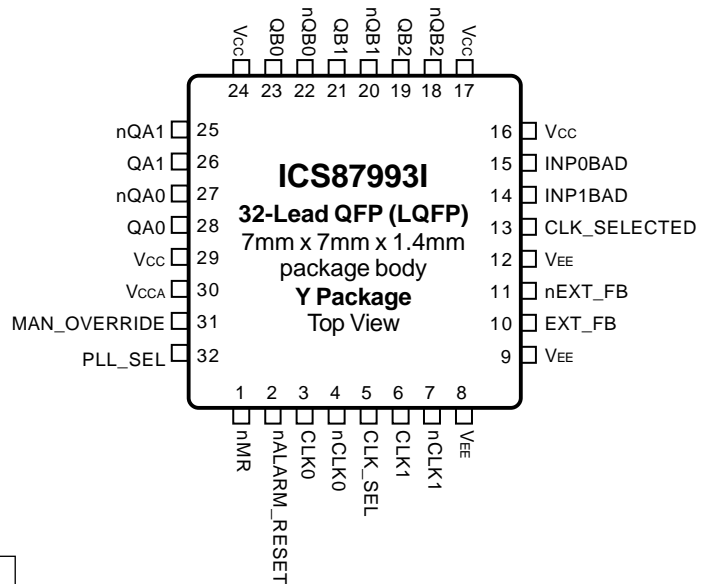
The ICS87993I is a PLL clock driver designed specifically for redundant clock tree designs. The device receives two differential LVPECL clock signals from which it generates 5 new differential LVPECL clock outputs. Two of the output pairs regenerate the input signal frequency and phase while the other three pairs generate 2x, phase aligned clock outputs. External PLL feedback is used to also provide zero delay buffer performance.

The ICS87993I Dynamic Clock Switch (DCS) circuit continuously monitors both input CLK signals. Upon detection of a failure (CLK stuck HIGH or LOW for at least 1 period), the INP\_BAD for that CLK will be latched (H). If that CLK is the primary clock, the DCS will switch to the good secondary clock and phase/frequency alignment will occur with minimal output phase disturbance. The typical phase bump caused by a failed clock is eliminated.

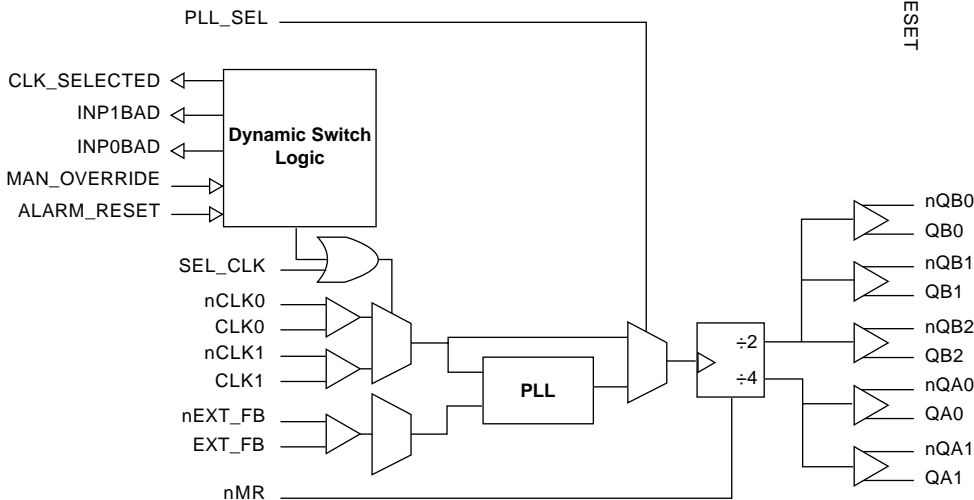
### FEATURES

- 5 differential 3.3V LVPECL outputs
- Selectable differential clock inputs
- CLKx, nCLKx pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- VCO range: 200MHz to 500MHz
- External feedback for “zero delay” clock regeneration with configurable frequencies
- Cycle-to-cycle jitter (RMS): 20ps (maximum)
- Output skew: 70ps (maximum), within one bank
- 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Pin compatible with MPC993

### PIN ASSIGNMENT



### BLOCK DIAGRAM





**TABLE 1. PIN DESCRIPTIONS**

Number	Name	Type		Description
1	nMR	Input	Pullup	Active LOW Master Reset. When logic LOW, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic HIGH, the internal dividers and the outputs are enabled. LVCMOS / LVTTTL interface levels.
2	nALARM_RESET	Input	Pullup	When LOW, resets the input bad flags and aligns CLK_SELECTED with SEL_CLK. LVCMOS / LVTTTL interface levels.
3	CLK0	Input	Pulldown	Non-inverting differential clock input.
4	nCLK0	Input	Pullup	Inverting differential clock input.
5	SEL_CLK	Input	Pulldown	Clock select input. When LOW, selects CLK0, nCLK0 inputs. When HIGH, selects CLK1, nCLK1 inputs. LVCMOS / LVTTTL interface levels.
6	CLK1	Input	Pulldown	Non-inverting differential clock input.
7	nCLK1	Input	Pullup	Inverting differential clock input.
8, 9, 12	V <sub>EE</sub>	Power		Negative supply pins.
10	EXT_FB	Input	Pulldown	Differential external feedback.
11	nEXT_FB	Input	Pullup	Differential external feedback.
13	CLK_SELECTED	Output		LOW, when CLK0, nCLK0 is selected, HIGH, when CLK1, nCLK1 is selected. LVCMOS / LVTTTL interface levels.
14	INP1BAD	Output		Indicates detection of a bad input reference clock 1 with respect to the feedback signal. The output is active HIGH and will remain HIGH until the alarm reset is asserted.
15	INP0BAD	Output		Indicates detection of a bad input reference clock 0 with respect to the feedback signal. The output is active HIGH and will remain HIGH until the alarm reset is asserted.
16, 17, 24, 29	V <sub>CC</sub>	Power		Core supply pins.
18, 19	nQB2, QB2	Output		Differential output pair. LVPECL interface levels.
20, 21	nQB1, QB1	Output		Differential output pair. LVPECL interface levels.
22, 23	nQB0, QB0	Output		Differential output pair. LVPECL interface levels.
25, 26	nQA1, QA1	Output		Differential output pair. LVPECL interface levels.
27, 28	nQA0, QA0	Output		Differential output pair. LVPECL interface levels.
30	V <sub>CCA</sub>	Power		Analog supply pin.
31	MAN_OVERRIDE	Input	Pulldown	Manual override. When HIGH, disables internal clock switch circuitry. LVCMOS / LVTTTL interface levels.
32	PLL_SEL	Input	Pullup	Selects between the PLL and reference clock as the input to the dividers. When LOW, selects reference clock. When HIGH, selects PLL. LVCMOS / LVTTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		KΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		KΩ



### ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V_{CC}$	4.6V
Inputs, $V_i$	-0.5V to $V_{CC} + 0.5V$
Outputs, $I_o$	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, $\theta_{JA}$	47.9°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 3A. POWER SUPPLY DC CHARACTERISTICS,  $V_{CC} = V_{CCA} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{CCA}$	Analog Supply Voltage		3.135	3.3	3.465	V
$I_{EE}$	Power Supply Current			80	180	mA
$I_{CCA}$	Analog Supply Current			15	20	mA

**TABLE 3B. LVCMOS/LVTTL DC CHARACTERISTICS,  $V_{CC} = V_{CCA} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	LVCMOS Inputs	2		3.3	V
$V_{IL}$	Input Low Voltage	LVCMOS Inputs	-0.3		0.8	V
$I_{IH}$	Input High Current	SEL_CLK, MAN_OVERRIDE $V_{IN} = V_{CC} = 3.465V$			5	$\mu\text{A}$
		nALARM_RESET, PLL_SEL, nMR $V_{IN} = V_{CC} = 3.465V$			120	$\mu\text{A}$
$I_{IL}$	Input Low Current	SEL_CLK, MAN_OVERRIDE $V_{IN} = 0V, V_{CC} = 3.465V$	-5			$\mu\text{A}$
		nALARM_RESET, PLL_SEL, nMR $V_{IN} = 0V, V_{CC} = 3.465V$	-120			$\mu\text{A}$
$V_{OH}$	Output High Voltage; NOTE 1		2.4			V
$V_{OL}$	Output Low Voltage; NOTE 1				0.5	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CC}/2$ . See Parameter Measurement Information Section, "3.3V Output Load AC Test Circuit diagram".

**TABLE 3C. DIFFERENTIAL DC CHARACTERISTICS,  $V_{CC} = V_{CCA} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	CLK0, CLK1, EXT_FB $V_{IN} = V_{CC} = 3.465V$			5	$\mu\text{A}$
		nCLK0, nCLK1, nEXT_FB $V_{IN} = V_{CC} = 3.465V$			120	$\mu\text{A}$
$I_{IL}$	Input Low Current	CLK0, CLK1, EXT_FB $V_{IN} = 0V, V_{CC} = 3.465V$	-5			$\mu\text{A}$
		nCLK0, nCLK1, nEXT_FB $V_{IN} = 0V, V_{CC} = 3.465V$	-120			$\mu\text{A}$
$V_{PP}$	Peak-to-Peak Input Voltage		0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2		$V_{EE} + 0.5$		$V_{CC} - 0.85$	V

NOTE 1: Common mode voltage is defined as  $V_{IH}'$ .

NOTE 2: For single ended applications, the maximum input voltage for CLK, nCLK is  $V_{CC} + 0.3V$ .



**TABLE 3D. LVPECL DC CHARACTERISTICS,  $V_{CC} = V_{CCA} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		$V_{CC} - 1.4$		$V_{CC} - 1.0$	V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{CC} - 2.0$		$V_{CC} - 1.7$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .

**TABLE 4. AC CHARACTERISTICS,  $V_{CC} = V_{CCA} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units	
$f_{VCO}$	PLL VCO Lock Range		200		500	MHz	
$t_{PWI}$			25		75	%	
$t_{PD}$	Propagation Delay	CLKx to Q	PLL_SEL = LOW	2.8	3.45	4.1	ns
		CLKx to EXT_FB; NOTE 2	PLL_SEL = HIGH $f_{VCO} \leq 360MHz$	-150	0	170	ps
			PLL_SEL = HIGH $f_{VCO} \leq 500MHz$	-150	0	200	ps
$t_R / t_F$	Output Rise Time	20% to 80% @ 50MHz	200		800	ps	
$tsk(o)$	Output Skew; NOTE 3	Within Bank			70	ps	
		All Outputs			100	ps	
$\Delta_{PER/CYCLE}$	Rate of change of Periods	Tested at typical conditions	75MHz Output; NOTE 1, 4		20	50	ps/cycle
			150MHz Output; NOTE 1, 4		10	25	ps/cycle
			75MHz Output; NOTE 1, 5		200	400	ps/cycle
			150MHz Output; NOTE 1, 5		100	200	ps/cycle
odc	Output Duty Cycle	$f \leq 360MHz$	45		55	%	
$f_{jit(cc)}$	Cycle-to-Cycle Jitter (RMS); NOTE 1				20	ps	
$t_L$	PLL Lock Time; NOTE 1				10	ms	

All parameters measured at  $f_{MAX}$  unless noted otherwise.

NOTE 1: These parameters are guaranteed by characterization. Not tested in production.

NOTE 2: Defined as the time difference between the input reference clock and the averaged feedback input signal, when the PLL is locked and the input reference frequency is stable.

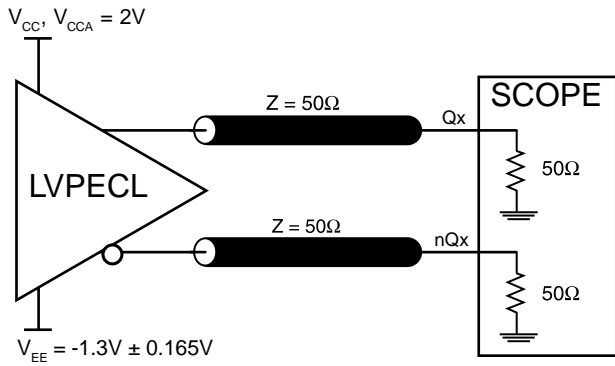
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

NOTE 4: Specification holds for a clock switch between two signals no greater than 400ps out of phase. Delta period change per cycle is averaged over the clock switch excursion.

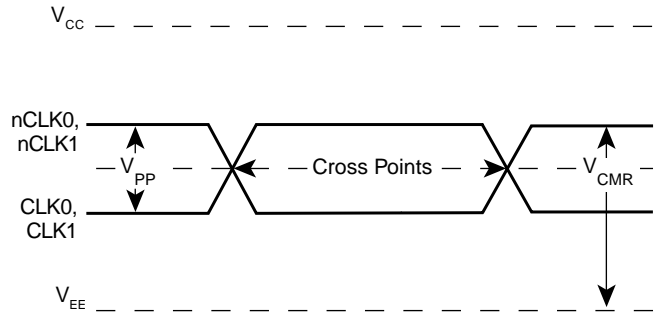
NOTE 5: Specification holds for a clock switch between two signals no greater than  $\pm\pi$  out of phase. Delta period change per cycle is averaged over the clock switch excursion.



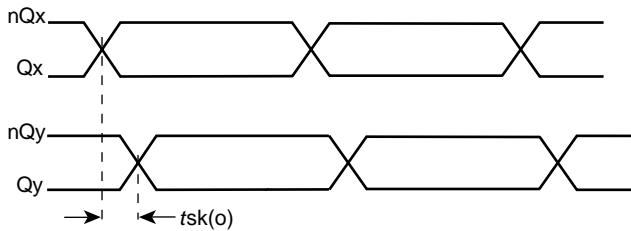
## PARAMETER MEASUREMENT INFORMATION



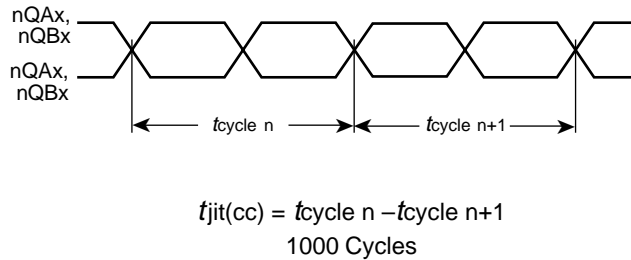
**3.3V OUTPUT LOAD AC TEST CIRCUIT**



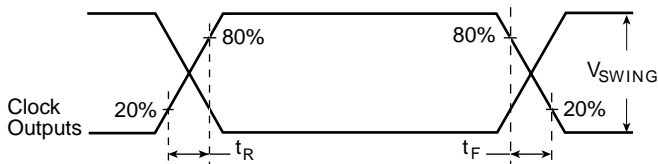
**DIFFERENTIAL INPUT LEVEL**



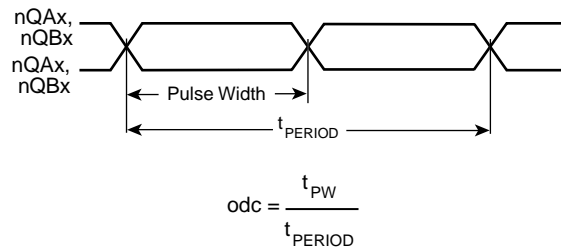
**OUTPUT SKEW**



**CYCLE-TO-CYCLE JITTER**



**OUTPUT RISE/FALL TIME**



**odc & t<sub>PERIOD</sub>**



## APPLICATION INFORMATION

### POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS87993I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{CC}$  and  $V_{CCA}$  should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a  $10\Omega$  resistor along with a  $10\mu\text{F}$  and a  $.01\mu\text{F}$  bypass capacitor should be connected to each  $V_{CCA}$  pin.

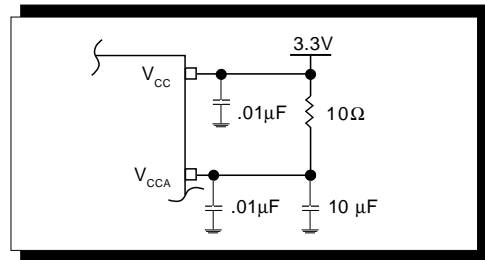


FIGURE 1. POWER SUPPLY FILTERING

### TERMINATION FOR LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

F<sub>OUT</sub> and nF<sub>OUT</sub> are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to

drive  $50\Omega$  transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

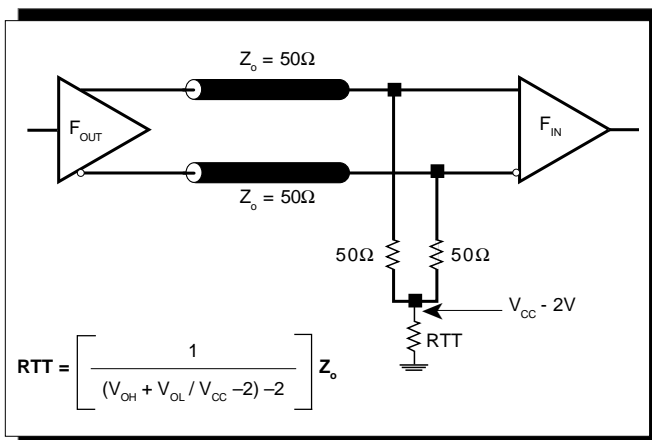


FIGURE 2A. LVPECL OUTPUT TERMINATION

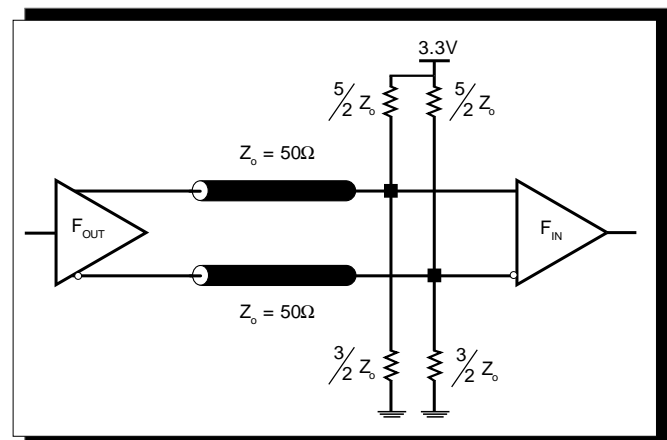


FIGURE 2B. LVPECL OUTPUT TERMINATION



### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 3 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{CC}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio

of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{CC} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .

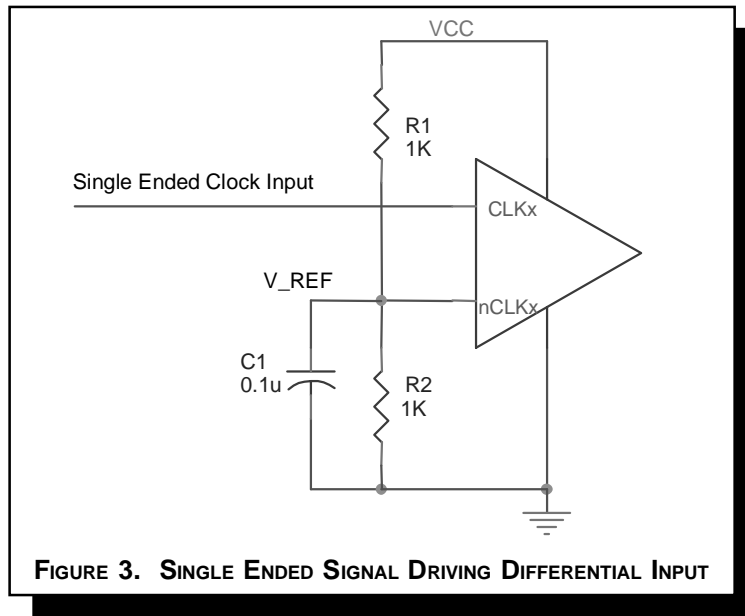


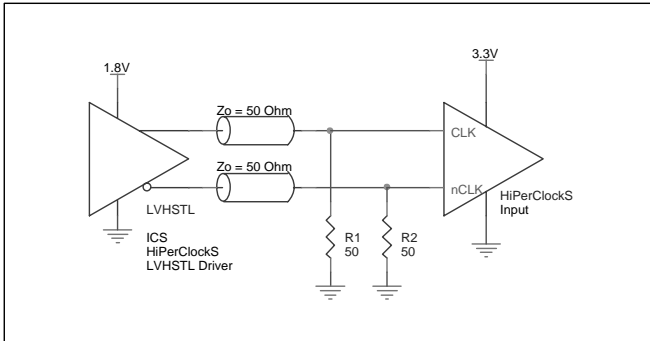
FIGURE 3. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT



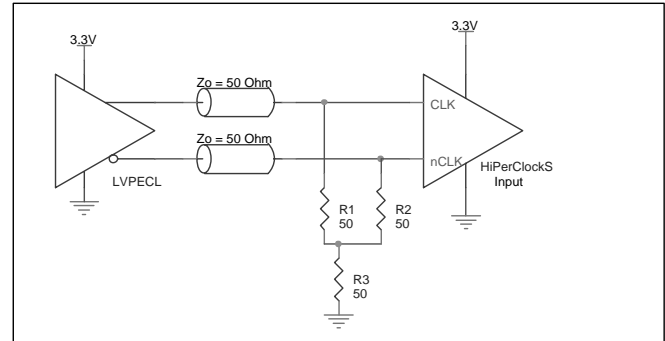
### DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK/nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSTL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 4A to 4E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested

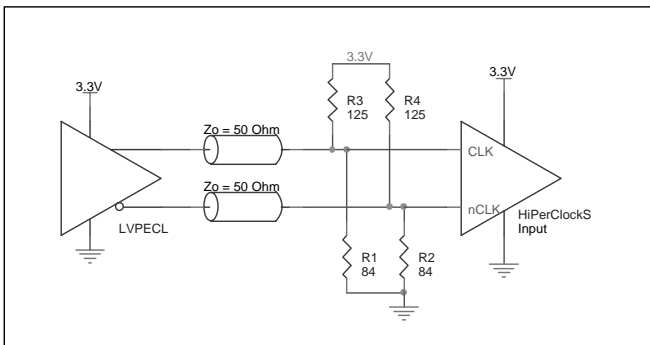
here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 4A*, the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



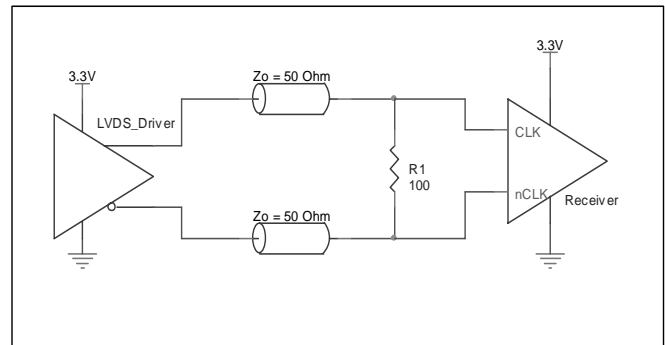
**FIGURE 4A. HiPerClockS CLK/nCLK INPUT DRIVEN BY ICS HiPerClockS LVHSTL DRIVER**



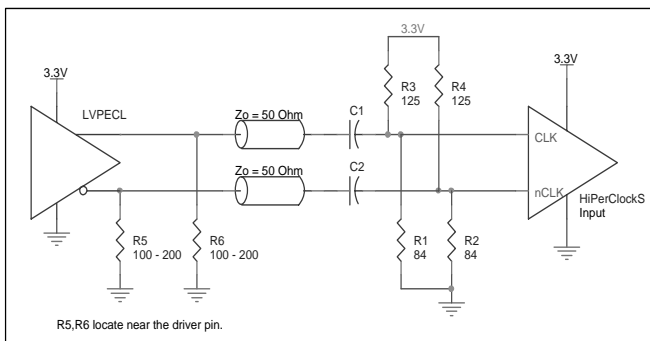
**FIGURE 4B. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**



**FIGURE 4C. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**



**FIGURE 4D. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVDS DRIVER**



**FIGURE 4E. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER WITH AC COUPLE**





### SCHEMATIC EXAMPLE

Figure 5A shows a schematic example of the ICS87993I. In this example, the CLK0/nCLK0 input is selected as primary. The input is driven by an LVPECL driver. Feedback can be either from

Bank A or Bank B depending on the application. The decoupling capacitors should be physically located near the power pin. For ICS87993I, the unused outputs can be left floating.

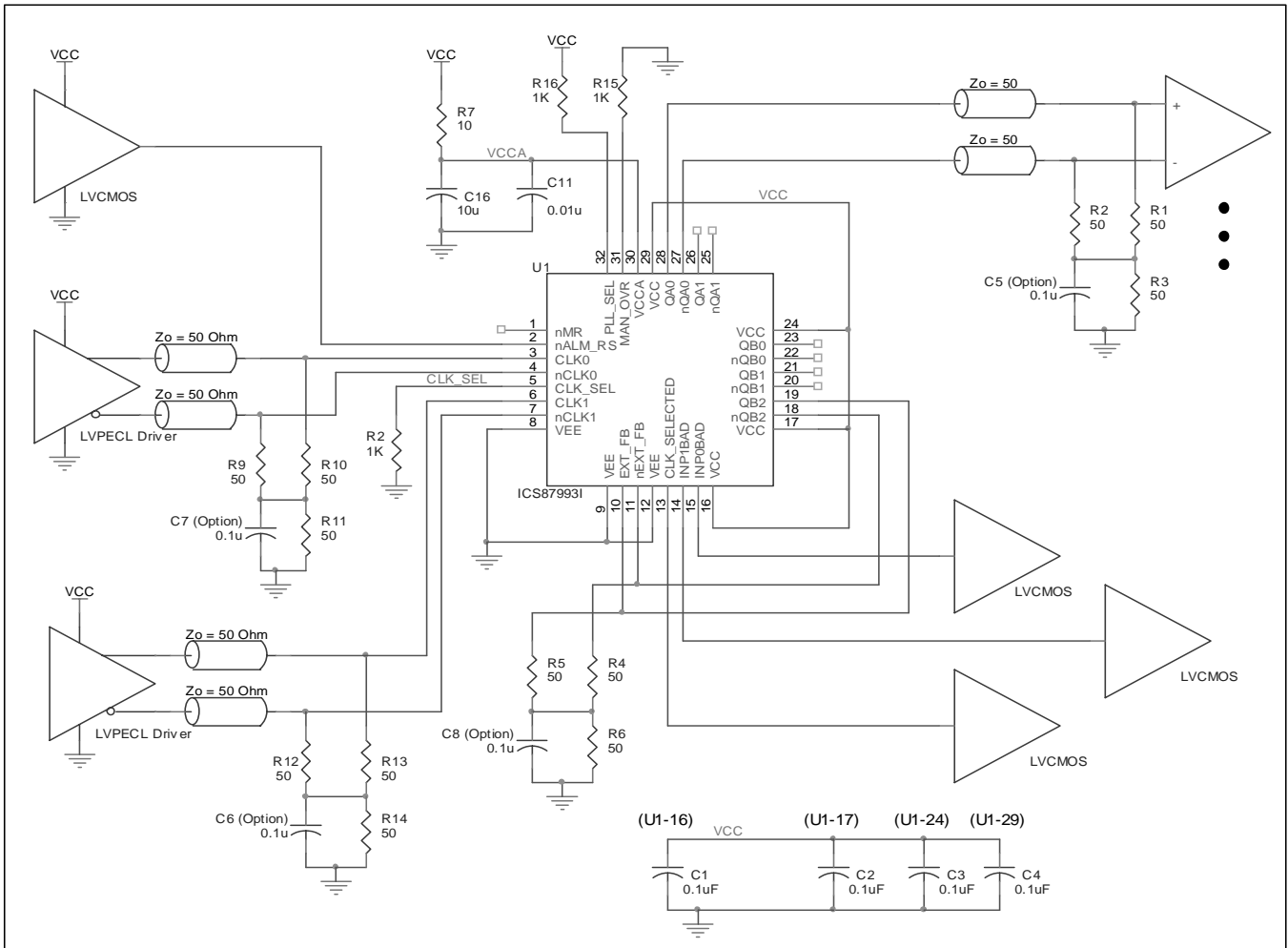


FIGURE 5A. ICS87993I LVPECL SCHEMATIC EXAMPLE



The following component footprints are used in this layout example:

All the resistors and capacitors are size 0603.

### POWER AND GROUNDING

Place the decoupling capacitors as close as possible to the power pins. If space allows, placement of the decoupling capacitor on the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin caused by the via.

Maximize the power and ground pad sizes and number of vias capacitors. This can reduce the inductance between the power and ground planes and the component power and ground pins.

The RC filter consisting of R7, C11, and C16 should be placed as close to the  $V_{DDA}$  pin as possible.

### CLOCK TRACES AND TERMINATION

Poor signal integrity can degrade the system performance or cause system failure. In synchronous high-speed digital systems, the clock signal is less tolerant to poor signal integrity than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The shape of the trace and the

trace delay might be restricted by the available space on the board and the component location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signal traces.

- The differential 50Ω output traces should have same length.
- Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.
- Keep the clock traces on the same layer. Whenever possible, avoid placing vias on the clock traces. Placement of vias on the traces can affect the trace characteristic impedance and hence degrade signal integrity.
- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow a separation of at least three trace widths between the differential clock trace and the other signal trace.
- Make sure no other signal traces are routed between the clock trace pair.
- The series termination resistors should be located as close to the driver pins as possible.

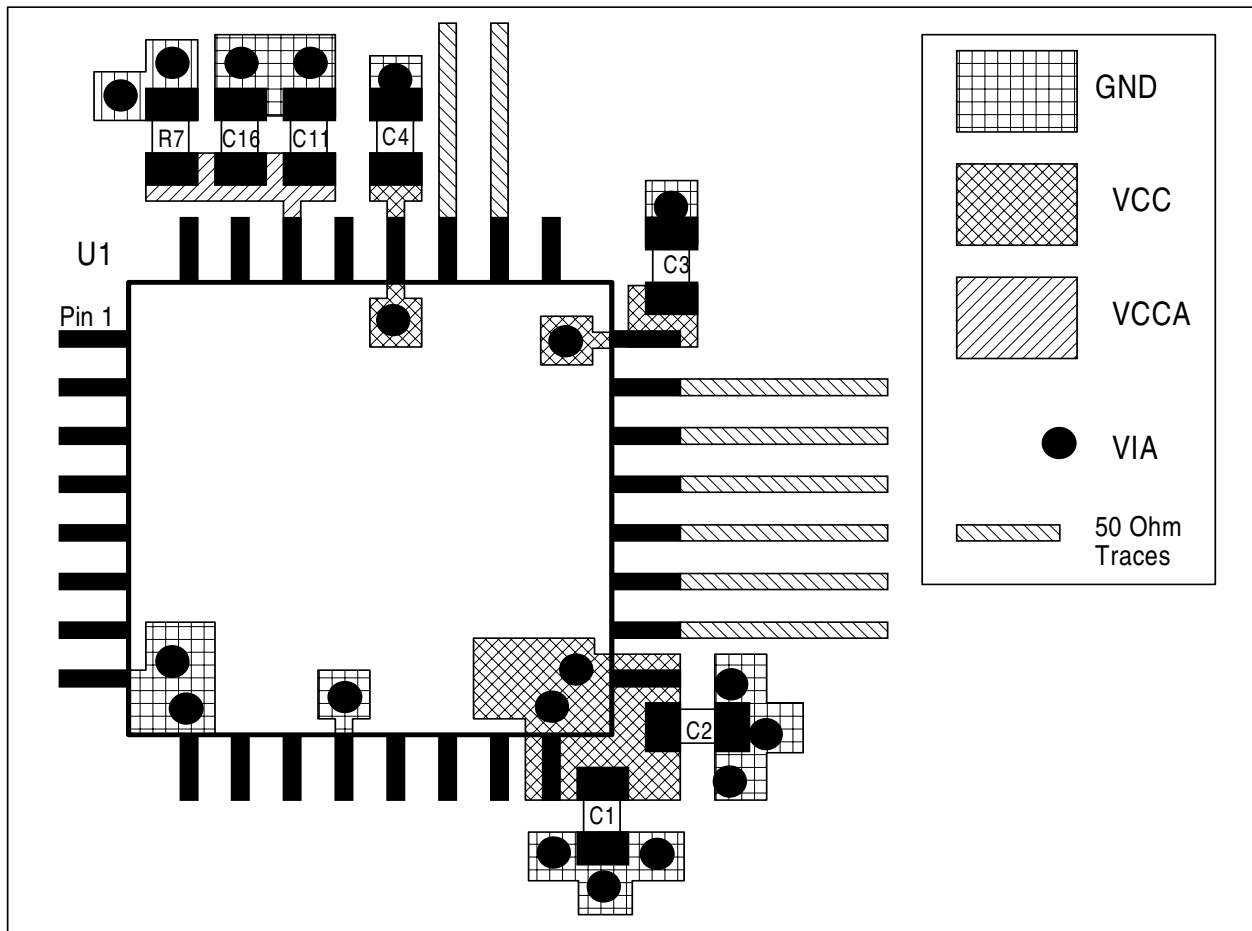


FIGURE 5B. PCB BOARD LAYOUT FOR ICS87993I



## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS87993I. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS87993I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 180 = 624mW$
- Power (outputs)<sub>MAX</sub> = **30.2mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $5 * 30.2mW = 151mW$

**Total Power**<sub>MAX</sub> (3.465V, with all outputs switching) =  $624mW + 151mW = 775mW$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 42.1°C/W per Table 5 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.775W * 42.1^\circ C/W = 117.6^\circ C. \text{ This is below the limit of } 125^\circ C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**TABLE 5. THERMAL RESISTANCE  $\theta_{JA}$  FOR 32-PIN LQFP, FORCED CONVECTION**

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

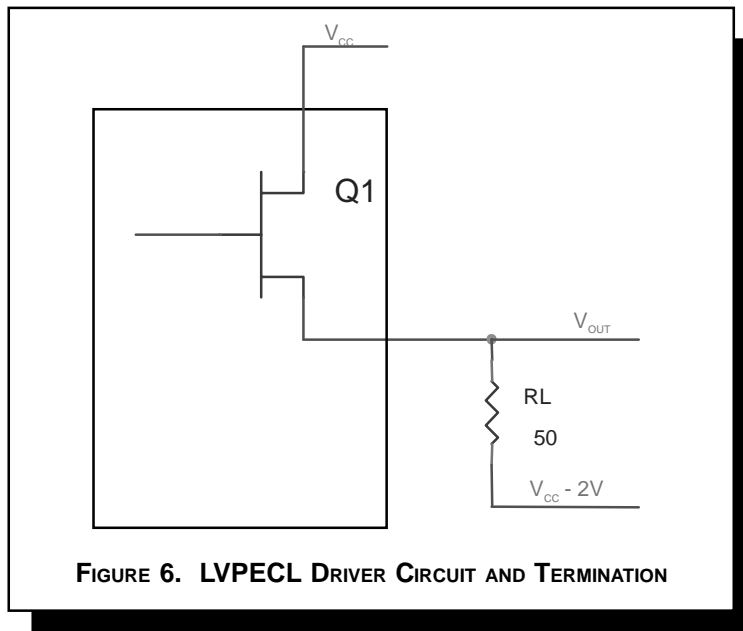
**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.



### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 6*.



**FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CC} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CC\_MAX} - 1.0V$

$$(V_{CC\_MAX} - V_{OH\_MAX}) = 1.0V$$

- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CC\_MAX} - 1.7V$

$$(V_{CC\_MAX} - V_{OL\_MAX}) = 1.7V$$

$Pd\_H$  is power dissipation when the output drives high.  
 $Pd\_L$  is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - 1V)/50\Omega] * 1V = \mathbf{20.0mW}$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$$

Total Power Dissipation per output pair =  $Pd\_H + Pd\_L = \mathbf{30.2mW}$



## RELIABILITY INFORMATION

TABLE 6.  $\theta_{JA}$  VS. AIR FLOW TABLE

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### TRANSISTOR COUNT

The transistor count for ICS87993I is: 2745



PACKAGE OUTLINE - Y SUFFIX

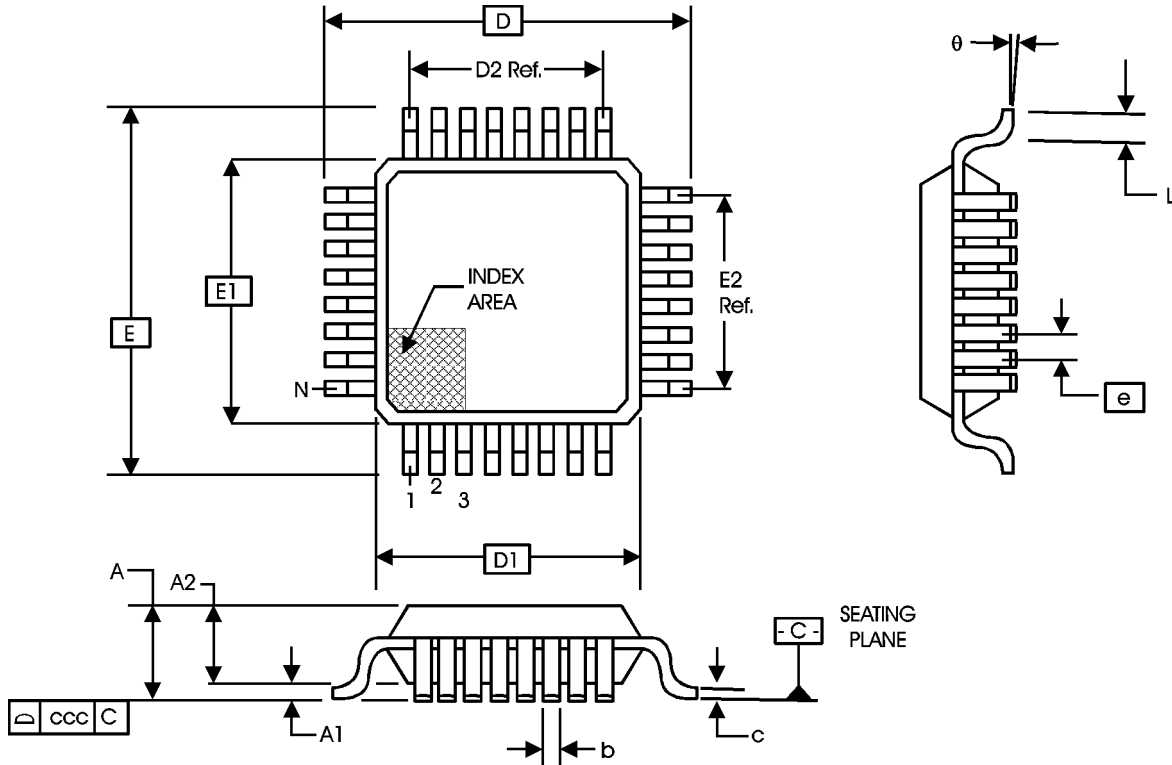


TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N	32		
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D	9.00 BASIC		
D1	7.00 BASIC		
D2	5.60 Ref.		
E	9.00 BASIC		
E1	7.00 BASIC		
E2	5.60 Ref.		
e	0.80 BASIC		
L	0.45	0.60	0.75
$\theta$	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026



Integrated  
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Systems, Inc.

# ICS87993I

## 1-TO-5 DIFFERENTIAL-TO-3.3V LVPECL PLL CLOCK DRIVER W/DYNAMIC CLOCK SWITCH

**TABLE 8. ORDERING INFORMATION**

Part/Order Number	Marking	Package	Count	Temperature
ICS87993AYI	ICS87993AYI	32 Lead LQFP	250 per tray	-40°C to 85°C
ICS87993AYIT	ICS87993AYI	32 Lead LQFP on Tape and Reel	1000	-40°C to 85°C

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REVISION HISTORY SHEET				
Rev	Table	Page	Description of Change	Date
A	T4	4	AC Table - deleted Note 6.	1/16/03
		7	Added "Wiring the Differential Input to Accept Single Ended Levels".	
B	T1	1	Features Section - changed VCO max. from 360MHz to 500MHz.	5/21/03
		2	Pin Descriptions Table - revised nMR description.	
		2	Pin Characteristics Table - changed C <sub>IN</sub> from max. 4pF to typical 4pF.	
	T2	3	Absolute Maximum Ratings - changed V <sub>o</sub> to I <sub>o</sub> and included Continuous Current and Surge Current	
		4	AC Characteristics Table - changed fVCO from 360MHz to 500MHz. t <sub>PD</sub> - added test conditions to CLKx to EXT_FB. Added another line with 500MHz test conditions. odc - added test conditions.	
	T4	8	Added <i>Differential Clock Input Interface</i> in the Application Information section.	
9 & 10		Added Schematic Example.		