ADC-847
Microprocessor-Compatible 8-Bit A/D Converter

1

FEATURES

- **Microprocessor compatible**
- **9 Microseconds conversion time**
- **8-Bit resolution**
- **± ¼ LSB linearity error**
- **Ratiometric operation**

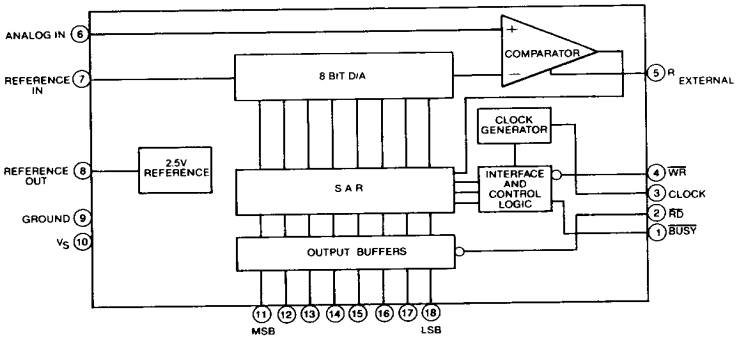
GENERAL DESCRIPTION

DATEL ADC-847 is a low cost, monolithic, 8-bit A/D converter designed to interface directly with a microprocessor via three-state outputs. The device appears as a memory location or I/O port to the microprocessor and thus requires a minimum of interfacing logic. Using the successive approximation technique, the ADC-847 completes an 8-bit conversion in 9 microseconds with a maximum linearity error as low as ± ¼ LSB.

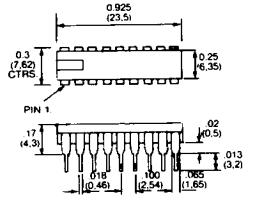
The data outputs of the ADC-847 are provided with three-state buffers to allow connection to a common data bus. The digital control lines; $\overline{WR}$, $\overline{RD}$ and $\overline{BUSY}$ are active low and are available in most microprocessor memory systems. The $\overline{BUSY}$ output uses a passive pull-up for CMOS/TTL compatibility which also allows up to four $\overline{BUSY}$ outputs to be connected together to form a common interrupt line. The ADC-847 will operate as a normal A/D converter for non-microprocessor applications.

Other important features include single supply operation capability, ratiometric operation, internal reference circuit and internal clock generator. The clock generator requires only an external capacitor or the device may be driven with an external clock. The reference circuit only requires an external resistor and capacitor or an external reference voltage can be connected to the reference input (Pin 7) if required. The ADC-847 is an ideal choice for many process control and instrumentation applications.

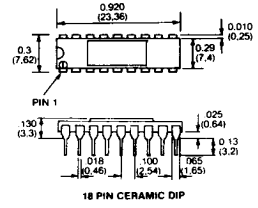
The ADC-847 is available for operation over the commercial, 0°C to +70°C and military, −55°C to +125°C temperature ranges and is packaged in either an 18 pin plastic or ceramic DIP.



MECHANICAL DIMENSIONS INCHES (MM)



18 PIN PLASTIC DIP



18 PIN CERAMIC DIP

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	$\overline{BUSY}$ (STATUS)
2	$\overline{RD}$ (OUTPUT ENABLE)
3	CLOCK
4	$\overline{WR}$ (START CONVERSION)
5	EXTERNAL RESISTOR
6	ANALOG INPUT
7	REFERENCE INPUT
8	REFERENCE OUTPUT
9	GROUND
10	+ V SUPPLY
11	DB7 (MSB)
12	DB6
13	DB5
14	DB4
15	DB3
16	DB2
17	DB1
18	DBO (LSB)

ABSOLUTE MAXIMUM RATINGS, ALL MODELS	ADC-847A	ADC-847B	ADC-847M
Supply Voltage		+7.0V	
Digital Input Voltage		V_S	
Analog Input Voltage		V_S	

FUNCTIONAL SPECIFICATIONS, ALL MODELS

Typical at +25°C, +5V dc supply voltage, 900 kHz clock frequency, unless otherwise noted.

ANALOG INPUTS	ADC-847A	ADC-847B	ADC-847M
Analog Input Ranges		0 to +5V, 0 to +10V, ±5V, ±10V	
Input Resistance		100 kΩ	
Reference Input Range		+1V to +3V	
Input Current[1]		1 μA	
DIGITAL INPUTS			
Input Logic Level, Vin ("1"), minimum		2V	
Input Logic Level, Vin ("0"), maximum		0.8V	
Input Logic Level, Iin ("1")[2]		300 μA	
Input Logic Level, Iin ("0")[3]		±10 μA	
Clock Input Voltage (pin 3)			
high level, minimum		4.0V	
low level, maximum		0.8V	
Clock Input Current, high level, maximum		800 μA	
low level, maximum		−500 μA	
Clock Pulse Width, minimum		500 nsec.	
$\overline{WR}$ (Write)		Start conversion pulse. 200 nsec. minimum pulse width. Active low input.	
$\overline{RD}$ (Read)		Active low state enables 3-state outputs.	
Input Clamp Diode Voltage, maximum		−1.5V	
DIGITAL OUTPUTS			
Parallel Output Data		8 parallel lines of three-state, gateable output data.	
Output Coding, Unipolar		Binary	
Bipolar		Offset Binary	
$\overline{BUSY}$		Active low output. High when conversion complete. Low when conversion in progress.	
Output Logic Level, Vout ("1"), minimum		2.4V	
Vout ("0"), maximum		0.4V	
Output Logic Level, Iout ("1"), maximum		100 μA	
Iout ("0"), maximum		1.6 mA	
Off-state output leakage current, maximum		2 μA	
PERFORMANCE			
Resolution		8 binary bits	
Linearity Error, maximum	±1 LSB	±¼ LSB	±¼ LSB
Differential Linearity Error, maximum	±1 LSB	±½ LSB	±½ LSB
Conversion Time		9 μsec.	
Internal Clock Frequency, maximum		1 MHz	
External Clock Frequency, maximum		1 MHz	
Reference Output Voltage, maximum[4]	2.600V	2.570V	2.570V
Reference Slope Resistance, maximum		2 Ω	
Reference Voltage Tempco		50 ppm/°C	
Reference Current, maximum		15 mA	
minimum		4 mA	
Linearity Tempco		±3.0 ppm/°C	
Zero Tempco		±8.0 ppm/°C	
Full-Scale Tempco		±2.5 ppm/°C	
POWER REQUIREMENTS			
Supply Voltage Range		+4.5V dc to +5.5V dc	
Supply Current, maximum		40 mA	
Power Consumption		125 mW	

PHYSICAL/ENVIRONMENTAL			
Operating Temp. Range			
ADC-847 A	0°C to +70°C		
ADC-847 B	0°C to +70°C		
ADC-847 M	−55°C to +125°C		
Storage Temp. Range	−55°C to +125°C		
Package Type, 18-Pin DIP	Plastic	Plastic	Ceramic

FOOTNOTES:

1. Input voltage = +3V and Rext = 82 kΩ.
2. Input voltage = 2.4V, supply voltage = 5.5V. For $\overline{RD}$ input, Iin ("1") = −150 μA.
3. Input voltage = +0.4V, supply voltage = 5.5V. For $\overline{RD}$ input, Iin ("0") = −300 μA.
4. Rref = 390Ω, Cref = 4.7 μF.

TECHNICAL NOTES

1. The internal clock generator requires an external capacitor (100 pf for 1 MHz) connected between Pin 3 and ground. The oscillator frequency may be trimmed with an external trim resistor (2 KΩ maximum) connected in series with the capacitor. For optimum accuracy and stability of the oscillator frequency without trimming, the use of a crystal or ceramic resonator connected between Pins 3 and 9 is recommended.

   An external clock signal from a TTL or CMOS gate to Pin 3 may be used if the application requires.
2. A 390Ω reference resistor (Rref) should be connected between Pins 8 and 10. This will supply a nominal reference current of 6.4 mA. Also, a 4.7 μF stabilizing/decoupling capacitor (Cref) should be connected between Pins 8 and 9. For internal reference operation, Vref OUT (Pin 8) is connected to Vref IN (Pin 7).
3. An external reference may be used if required. Voltage should be in the range of +1.5 to +3.0 volts and may be connected to Vref IN. The slope of such a reference source should be less than 2.5 Ω/n, where n is the number of converters supplied.
4. A continuous conversion can be accomplished by inverting the $\overline{BUSY}$ and feeding it to the convert ($\overline{WR}$) input. To ensure reliable operation, an initial start pulse is required. This can be accomplished by using a NOR gate instead of an inverter and feeding it with a positive going pulse. The pulse can be derived from a simple R.C. network that gives a single pulse when power is applied.
5. For ratiometric operation, if the output from a transducer varies with its supply, then an external reference for the A/D should be derived from the same supply. The external reference can vary

from +1.5V to +3.0V. Operation with a reference voltage less than +1.5V is possible but reduced overdrive to the comparator will increase its delay and the conversion time will need to be increased.

6. The $\overline{WR}$ (start conversion pulse) can be completely asynchronous with respect to the clock, and will produce valid data between 7½ and 8½ clock pulses later depending on the timing of the clock and CONVERT signals.
7. Upon receiving a convert pulse, the A/D is reset. (The MSB is set to "1" all other bits are set to "0" and the $\overline{BUSY}$ output goes low.) The A/D will remain in this state until the convert pulse returns high. After the start conversion input goes high, the MSB decision will be made on the falling clock edge after a rising clock edge (See timing diagram). This will insure that the MSB is allowed to settle for at least half a clock period or 550 nanoseconds at maximum clock frequency.

   The START CONVERSION ($\overline{WR}$) input is not locked out during a conversion. Therefore, if pulsed low at any time, the conversion will restart.
8. The ADC-847 can be operated with a single supply. However, a negative supply voltage is required to supply the tail current of the comparator. Since this current is only 25 to 150 μA and does not have to be well stabilized, it can be supplied by a simple diode pump circuit driven from the $\overline{BUSY}$ output. (See single supply operation.)

CALIBRATION PROCEDURE

For calibration procedure, unipolar and bipolar, apply continuous convert pulses to start conversion ($\overline{WR}$) input long enough to allow a complete conversion and monitor the digital outputs.

CALIBRATION

UNIPOLAR

Zero Adjust Apply 0.5 LSB to the analog input and adjust the ZERO ADJUST pot until the LSB (Bit 8) just flickers between 0 and 1 with all other bits at 0.

Gain Adjust Apply FS — 1.5 LSB to the analog input and adjust the GAIN ADJUST pot until the LSB (Bit 8) output just flickers between 0 and 1 with all other bits at 1.

COMPONENT VALUES					
INPUT RANGE	TP_1	TP_2	R_1	R_2	R_3
+5V	5k	1M	5.6k	8.2k	680k
+10V	10k	1M	11k	5.6k	680k

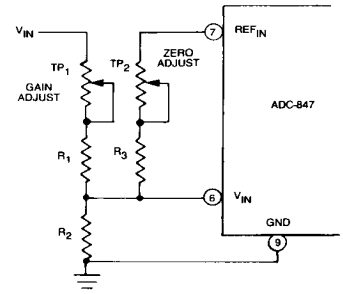
BIPOLAR

Offset Adjust Apply −(FS − 0.5 LSB) to the analog input and adjust the OFFSET ADJUST pot until the LSB (Bit 8) output just flickers between 0 and 1 with all other bits at 0.

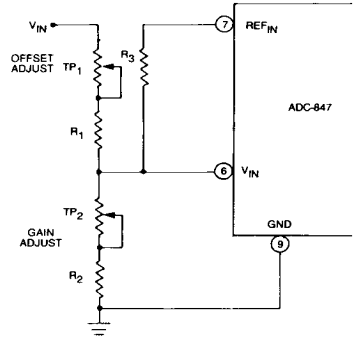
Gain Adjust Apply +(FS − 1.5 LSB) to the analog input and adjust the GAIN ADJUST pot until the LSB (Bit 8) just flickers between 0 and 1 with all other bits at 1.

After gain adjust, repeat offset adjust procedure.

COMPONENT VALUES					
INPUT RANGE	TP_1	TP_2	R_1	R_2	R_3
±5V	5k	5k	13k	13k	7.5k
±10V	10k	5k	27k	8.2k	8.2k



CONNECTION FOR UNIPOLAR OPERATION



CONNECTIONS FOR BIPOLAR OPERATION

CODING TABLES

UNIPOLAR

DIGITAL OUTPUT	ANALOG INPUT
11111111	FS-1 LSB
11000000	0.75 FS
10000000	0.5 FS
01000000	0.25 FS
00000000	0

$$1\ LSB = \frac{FS}{256}$$

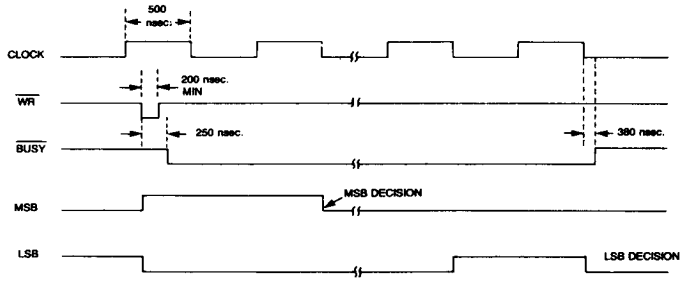
BIPOLAR

DIGITAL OUTPUT	ANALOG INPUT
11111111	+ (FS-1 LSB)
11000000	+ 0.5 FS
10000000	0
01000000	− 0.5 FS

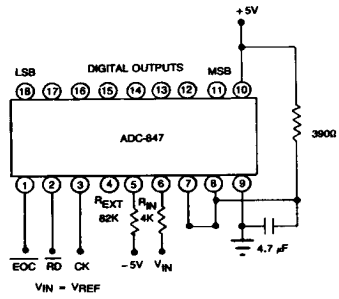
$$1\ LSB = \frac{2\ FS}{256}$$

TIMING AND CONNECTION

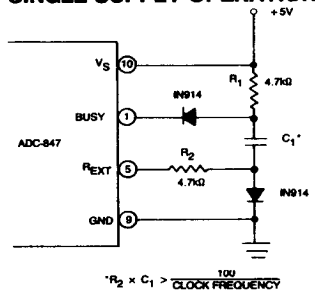
TIMING DIAGRAM



TYPICAL CONNECTION

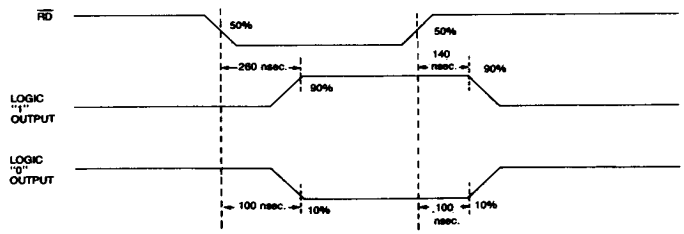


SINGLE SUPPLY OPERATION

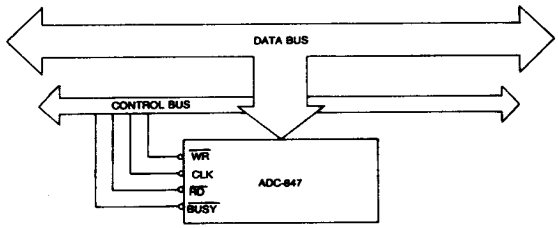


DIODE PUMP CIRCUIT TO SUPPLY COMPARATOR TAIL CURRENT. SEE TECHNICAL NOTE 8.

OUTPUT ENABLE/DISABLE DELAYS



TYPICAL CONNECTION TO MICROPROCESSOR DATABASE



The ADC-847 is primarily designed to interface directly to a microprocessor via three-state outputs. The device appears as a memory location or I/O peripheral to the microprocessor thus requiring a minimum of external interface logic.

ORDERING INFORMATION

MODEL NO.	LINEARITY ERROR	OPERATING TEMP. RANGE
ADC-847A	±1 LSB	0°C to +70°C
ADC-847B	±¼ LSB	0°C to +70°C
ADC-847M	±¼ LSB	−55°C to +125°C

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