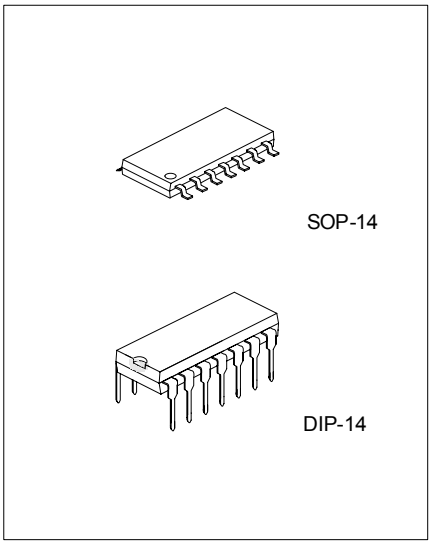
# 3515A

**CMOS IC**

# PC POWER SUPPLY SUPERVISOR




* Pb-free plating product number: 3515AL

## ■ DESCRIPTION

The UTC **3515A** is specially designed for switching power supply system. it provides protection circuits, power good output (PGO) indicator, fault protection output (FPOB) and a PSONB control.

The protection circuits include over voltage protection (OVP), under voltage protection (UVP) and over current protection (OCP) monitoring for system voltages and currents.

When 3.3V, 5V or 12V voltage is decreasing to 2.68V, 4.3V and 9.9V respectively, the under voltage protection (UVP) function will be enabled. FPOB will be set to high to turn off the PWM controller IC. Toggling the PSONB from low to high will reset the fault protection latch.

The voltage difference across external current shunt is used for OCP functions. An external resistor can be used to adjust protection threshold.

The power supply is turned on after 38mS delay time when PSONB signal is set from high to low. To turn off power supply, PSONB signal is set from low to high with the delay time 38mS. The PGI circuitry provides a power-down warning signal for PGO. When PGI input is lower than the internal 1.20V reference voltage, PGO signal is pulled low.

## ■ FEATURES

* OVP/UVP monitors 3.3V, 5V, 12V input voltage level.
* OCP monitors $I_{S33}$, $I_{S5}$, $I_{S12}$ input current sense.
* Fault protection output (FPOB) with Open Drain Output stage.
* Power good output (PGO) with Open Drain Output stage.
* 38ms de-bounce time for PSONB input signal.
* 300ms time delay from PGI to PGO.
* 2.4ms time delay for PSONB to turn off FPOB.

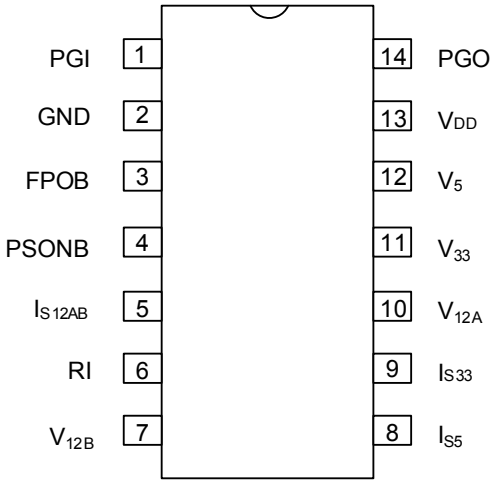
## ■ ORDERING INFORMATION

| Ordering Number | | Package | Packing |
|---|---|---|---|
| Normal | Lead Free Plating | | |
| 3515A-D14-T | 3515AL-D14-T | DIP-14 | Tube |
| 3515A-S14-R | 3515AL-S14-R | SOP-14 | Tape Reel |
| 3515A-S14-T | 3515AL-S14-T | SOP-14 | Tube |

3515AL-D14-T
(1)Packing Type
(2)Package Type
(3)Lead Plating

(1) R: Tape Reel, T: Tube
(2) D14: DIP-14, S14: SOP-14
(3) L: Lead Free Plating, Blank: Pb/Sn

## ■ PIN ASSIGNMENT




## ■ FUNCTION DESCRIPTION

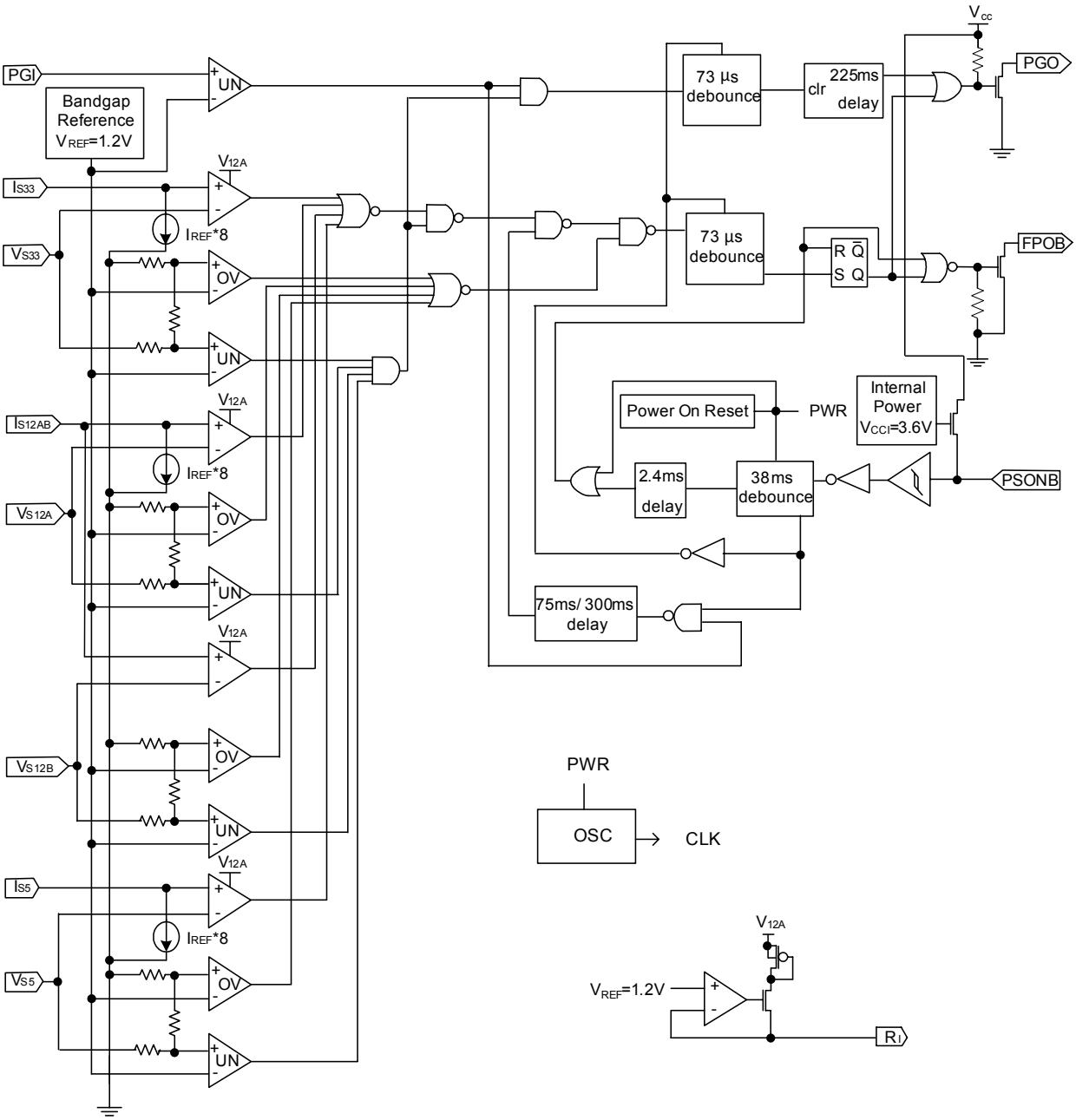
| PGI | PSONB | UV&OC Protection | OV Protection | FPOB | PGO |
|---|---|---|---|---|---|
| PGI<1.2V | L | No | No | L | L |
| PGI<1.2V | L | No | Yes | H | L |
| PGI<1.2V | L | Yes | No | L | L |
| PGI<1.2V | L | Yes | Yes | H | L |
| PGI>1.2V | L | No | No | L | H |
| PGI>1.2V | L | No | Yes | H | L |
| PGI>1.2V | L | Yes | No | H | L |
| PGI>1.2V | L | Yes | Yes | H | L |
| X | H | X | X | H | L |

Note: FPOB=L means: fault is not latched. FPOB=H means: fault is latched
PGO=L means: fault. PGO=H means: No fault
X=do not care

## ■ PIN DESCRIPTIONS

| PIN NO. | PIN NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| 1 | PGI | Input | Power Good Input. For ATX SMPS, it detects AC line voltage through the main transformer. |
| 2 | GND | Supply | Ground |
| 3 | FPOB | Output | Fault Protection Output. Output signal to control the primary PWM IC through an opto-coupler. When FPOB is low, the PWM IC is enabled. |
| 4 | PSONB | Input | Remote On/Off logic input from CPU or main-board. The power supply will be turned on/off after 38mS delay. |
| 5 | $I_{S12AB}$ | Input | 12V $_{AB}$ over current protection. |
| 6 | RI | Input | Reference setting. One external resistor Ri connected between RI and GND pin will determine a reference current, $I_{REF}$ = 1.20/Ri, for OCP programming. |
| 7 | $V_{12B}$ | Input | 12V over/under voltage protection. |
| 8 | $I_{S5}$ | Input | 5V over current protection. |
| 9 | $I_{S33}$ | Input | 3.3V over current protection |
| 10 | $V_{12A}$ | Input | 12V over/under voltage protection. |
| 11 | $V_{33}$ | Input | 3.3V over/under voltage protection |
| 12 | $V_5$ | Input | 5V over/under voltage protection. |
| 13 | $V_{DD}$ | Supply | Power supply. |
| 14 | PGO | Output | Power good logic output, 0 or 1(open-drain). Power good=1 means that the power supply is good for operation. The power good delay is 300mS. |

## ■ BLOCK DIAGRAM



## ■ ABSOLUTE MAXIMUM RATINGS

| PARAMETER | | SYMBOL | RATINGS | UNIT |
|---|---|---|---|---|
| Supply Voltage, $V_{DD}$, $V_{12A}$ | | | -0.3 ~ 16 | V |
| Input Voltage | $V_5$,$V_{33}$, PSONB, $I_{S5}$, $I_{S33}$ | $V_{IN}$ | -0.3 ~ 7 | V |
| | $I_{S12AB}$, $V_{12B}$ | | -0.3 ~ 16 | V |
| | PGI | | -0.3 ~ $V_{DD}$+0.3 | V |
| Output Voltage | FPOB | $V_{OUT}$ | -0.3 ~ 7 | V |
| | PGO | | -0.3 ~ 7 | V |
| Operating Temperature | | $T_{OPR}$ | -40 ~ +125 | ℃ |
| Storage Temperature | | $T_{STG}$ | -55 ~ +150 | ℃ |

Note Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

## ■ RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | SYMBOL | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Supply Voltage $V_{DD}$ | | $V_{DD}$ | 4 | 12 | 15 | V |
| Supply Voltage $V_{CC2}$ | | | 9.5 | 12 | 15 | V |
| Input Voltage | $V_5$,$V_{33}$ ,PGI ,PSONB | $V_{IN}$ | | | 7 | V |
| | $V_{12A}$, $V_{12B}$ | | | | 15 | V |
| Output Voltage | FPOB | $V_{OUT}$ | | | 7 | V |
| | PGO | | | | 7 | V |
| Output Sink Current | FPOB | $I_{O(SINK)}$ | | | 30 | mA |
| | PGO | | | | 10 | mA |
| RI Output Current | | $I_{O(RI)}$ | 10 | | 65 | uA |
| Supply Voltage Rising Time ($V_{DD}$) | | $t_R$ | 1 | | | ms |

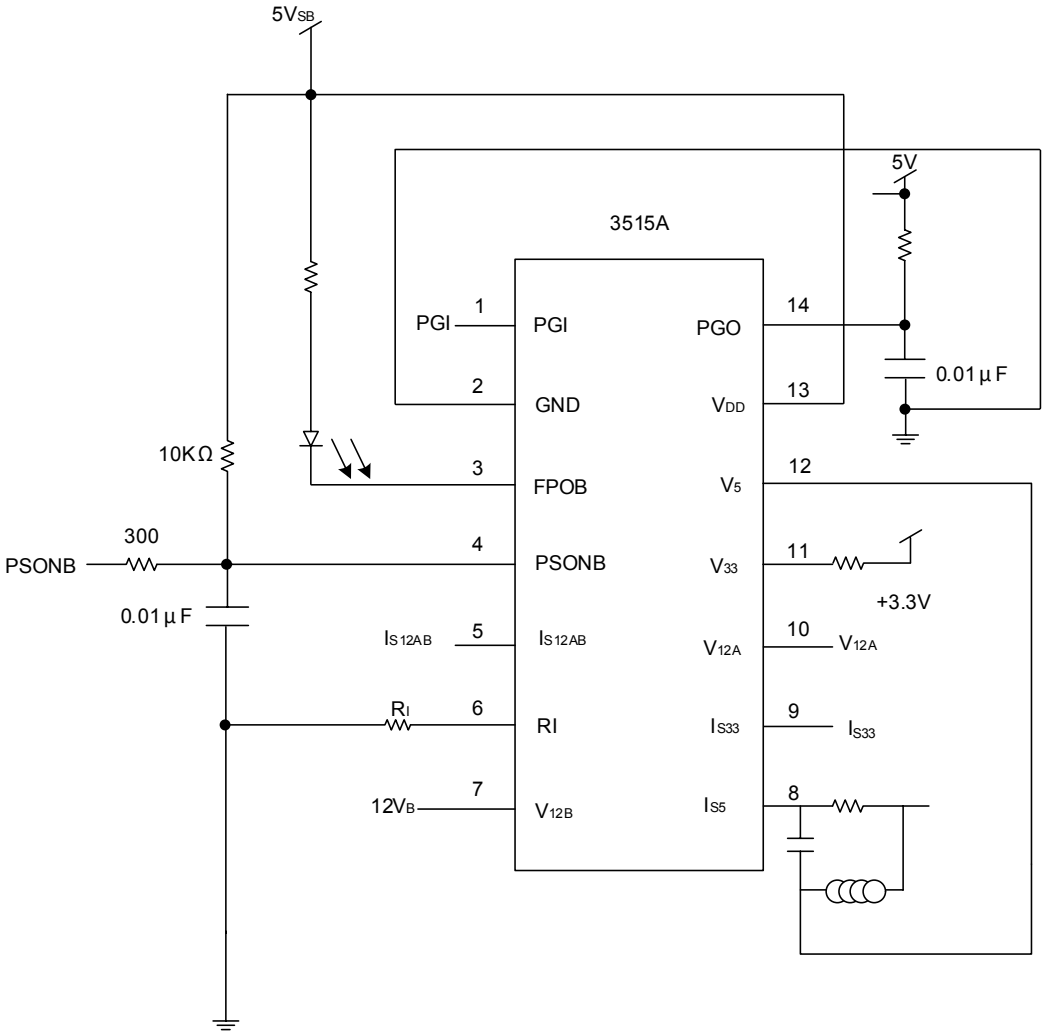
## ■ ELECTRICAL CHARACTERISTICS (Ta=25°C and $V_{DD}$=5V and $V_{12A}$=12V)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Over Voltage Detection** | | | | | | |
| Over Voltage Threshold | $V_{12A}$, $V_{12B}$ | | 13.2 | 13.8 | 14.4 | V |
| | $V_5$ | | 5.7 | 6.1 | 6.5 | V |
| | $V_{33}$ | | 3.7 | 3.9 | 4.1 | V |
| Low Level Output Voltage (FPOB) | $V_{OL}$ | $I_{SINK}$=10mA | | | 0.3 | V |
| | | $I_{SINK}$=30mA | | | 0.7 | |
| Output Leakage Current (FPOB) | $I_{LEAK}$ | $V_{(FPOB)}$=5V | | | 5 | uA |
| **PSONB** | | | | | | |
| High-Level Input Voltage | $V_{IH}$ | | 2 | | | V |
| Low-Level Input Voltage | $V_{IL}$ | | | | 0.8 | V |
| Input Pull-up Current | $I_{IN}$ | PSONB=0V | | 120 | | uA |
| **PGI and PGO** | | | | | | |
| Under Voltage Threshold | $V_{12A}$, $V_{12B}$ | | 9.5 | 10 | 10.5 | V |
| | $V_5$ | | 4.1 | 4.30 | 4.47 | V |
| | $V_{33}$ | | 2.55 | 2.69 | 2.83 | V |
| Input Threshold Voltage (PGI) | $V_{I(THD)}$ | | 1.16 | 1.20 | 1.24 | V |
| Low Level Output Voltage (PGO) | $V_{OL}$ | $I_{SINK}$=10mA | | | 0.4 | V |
| Output Leakage Current (PGO) | $I_{LEAK}$ | PGO=5V | | | 5 | uA |

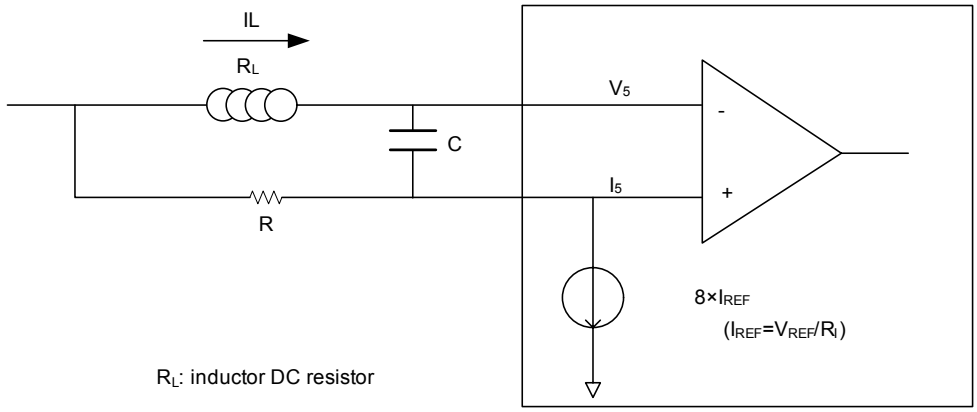
## ■ ELECTRICAL CHARACTERISTICS (Cont.)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SWITCHING CHARACTERISTICS** | | | | | | |
| PSONB ON(PSONB Low to FPOB Low) | $T_{(PSONB\ ON)}$ | $V_{DD}$=5V | 32 | 38 | 62 | ms |
| PSONB OFF(PSONB Hi to PGO Low) | $T_{(PSONB\ OFF)}$ | $V_{DD}$=5V | 32 | 38 | 62 | ms |
| PGI to PGO Delay Time | $T_{PG}$ | $V_{DD}$=5V | 200 | 300 | 490 | ms |
| Timing PGO Low to FPOB high | $T_{PSOFF}$ | $V_{DD}$=5V | 2.0 | 2.4 | 4 | ms |
| UVD/OCD Turn on Delay Time | $T_{UVP1}$ | FPOB=Low & PGI > 1.2V | 65 | 75 | 122 | ms |
| | $T_{UVP2}$ | FPOB=Low & PGI < 1.2V | 260 | 300 | 488 | ms |
| Noise Deglitch Time | $t_{g1}$ | | 63 | 75 | 120 | μs |
| Noise Deglitch Time for Latch | $t_{g2}$ | | 63 | 75 | 120 | μs |
| **TOTAL DEVICE** | | | | | | |
| Low Voltage | $V_{DD}$ | | | 3.0 | | V |
| Supply Current | $I_{DD}$ | PSONB=5V | | | 1 | mA |

## ■ APPLICATION INFORMATION



## ■ APPLICATION INFORMATION



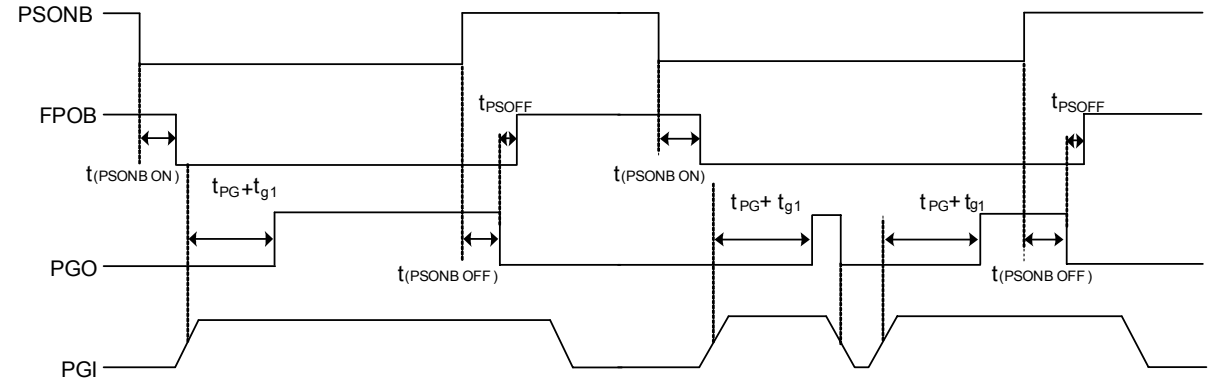

If IL* $R_L$ > (8 * $I_{REF}$) * R, then OCP active.
And the capacitor C is used to avoide power on fail or dynamic load failWe suggest C > 1μF.

EX：How to select the resistor of R? Assume $R_I$=30KΩ, $R_L$=3mΩ, OCP=20A。

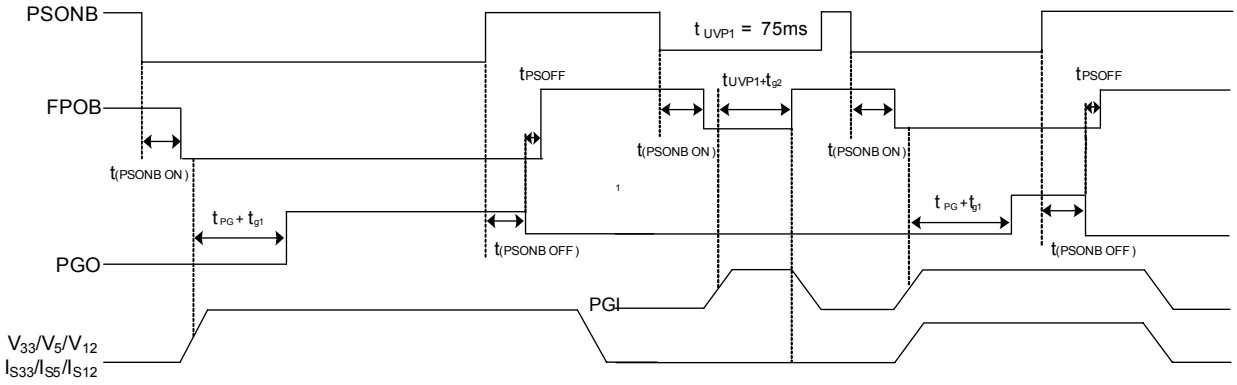
Sol：R = ( $I_L$ * $R_L$ ) / ( 8 * $I_{REF}$ )
= ( 20A * 3mΩ) / { 8 * ( 1.2V / 30KΩ)}
= 187.5Ω

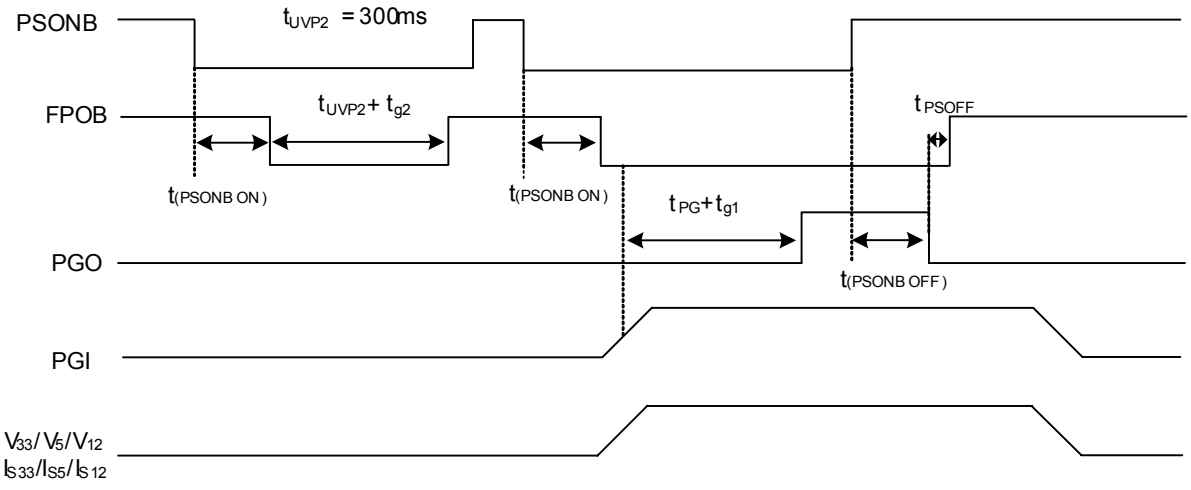
## ■ TYPICAL TIMMING DIAGRAM

**1) PGI (UNDER-VOLTAGE):**




**2) $V_{33}$, $V_5$, $V_{12A}$, $V_{12B}$ (UNDER-VOLTAGE) or $I_{S33}$, $I_{S5}$, $I_{S12AB}$ (OVER-CURRENT):**



## ■ TYPICAL TIMMING DIAGRAM(Cont.)

**3) $V_{33}$, $V_5$, $V_{12A}$, $V_{12B}$ (OVER-VOLTAGE).**