SPT7910

12-BIT, 10 MSPS, ECL, A/D CONVERTER

FEATURES

- Monolithic
- 12-Bit 10 MSPS Converter
- 67 dB SNR @ 500 kHz Input
- On-Chip Track/Hold
- Bipolar ±2.0 V Analog Input
- Low Power (1.4 W Typical)
- 5 pF Input Capacitance
- ECL Outputs

APPLICATIONS

- Radar Receivers
- Professional Video
- Instrumentation
- Medical Imaging
- Electronic Warfare
- Digital Communications
- Digital Spectrum Analyzers
- Electro-Optics

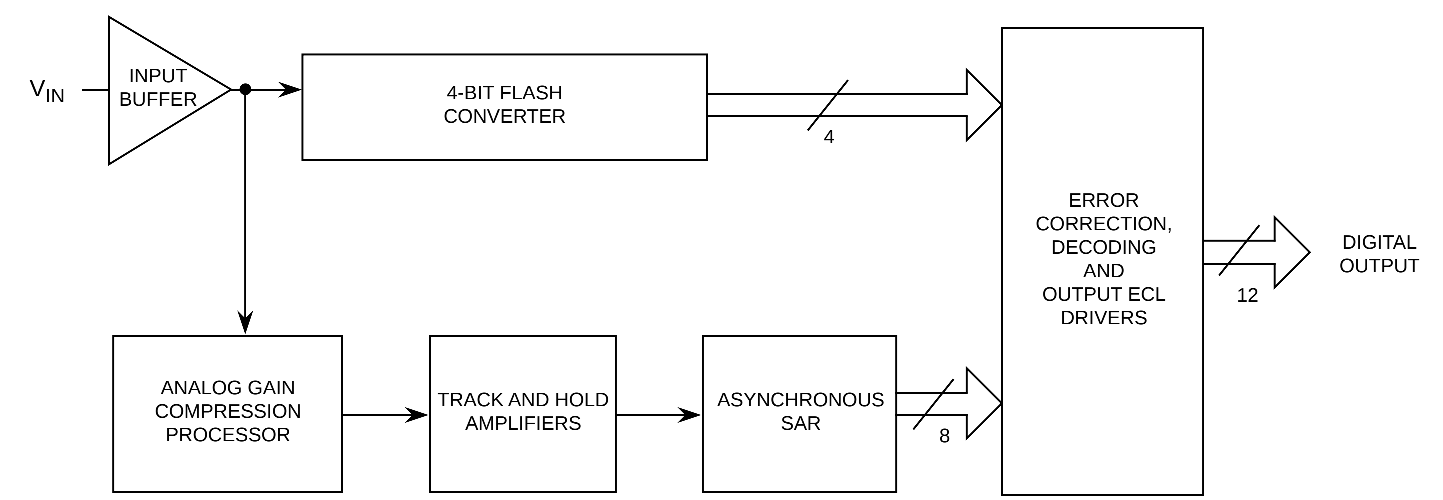
GENERAL DESCRIPTION

The SPT7910 analog-to-digital converter is industry's first 12-bit monolithic analog-to-digital converter capable of sample rates greater than 10 MSPS. On board input buffer and track/hold function assures excellent dynamic performance without the need for external components. Drive requirement problems are minimized with an input capacitance of only 5 pF.

Inputs and outputs are ECL to provide a higher level of noise immunity in high speed system applications. An overrange output signal is provided to indicate overflow conditions. Output data format is straight binary. Power dissipation is very low at only 1.4 watts with power supply voltages of +5.0 and -5.2 volts. The SPT7910 also provides a wide input voltage range of ±2.0 volts.

The SPT7910 is available in a 32-lead ceramic sidebrazed DIP package and in die form. A commercial temperature range of 0 to +70 °C is currently offered.

BLOCK DIAGRAM



Signal Processing Technologies, Inc.

4755 Forge Road, Colorado Springs, Colorado 80907, USA

Phone: (719) 528-2300 FAX: (719) 528-2370

ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

V_{CC} .... -0.3 to +6 V
V_{EE} .... +0.3 to -6 V

Input Voltages

Analog Input .... $V_{FB} \leq V_{IN} \leq V_{FT}$
V_{FT}, V_{FB}. .... +3.0 V, -3.0 V
Reference Ladder Current .... 12 mA

Output

Digital Outputs .... 0 to -30 mA

Temperature

Operating Temperature .... 0 to 70 °C
Junction Temperature .... 175 °C
Lead Temperature, (soldering 10 seconds) .... 300 °C
Storage Temperature ....-65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A=T_{MIN} to T_{MAX}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, DV_{CC}=+5.0 V, V_{IN}=±2.0 V, V_{SB}=-2.0 V, V_{ST}=+2.0 V, f_{CLK}=10 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7910 MIN	TYP	MAX	UNITS
Resolution			12			Bits
DC Accuracy (+25 °C)						
Integral Nonlinearity	± Full Scale	V		±2.0		LSB
Differential Nonlinearity	250 kHz Sample Rate	V		±0.8		LSB
No Missing Codes		VI		Guaranteed		
Analog Input						
Input Voltage Range		VI		±2.0		V
Input Bias Current		VI		30	60	μA
Input Resistance	V_{IN}=0 V	VI	100	300		kΩ
Input Capacitance		V		5		pF
Input Bandwidth	3 dB Small Signal	V		120		MHz
+FS Error		V		±5.0		LSB
-FS Error		V		±5.0		LSB
Reference Input						
Reference Ladder Resistance		VI	500	800		Ω
Reference Ladder Tempco		V		0.8		Ω/°C
Timing Characteristics						
Maximum Conversion Rate		VI	10			MHz
Overvoltage Recovery Time		V		20		ns
Pipeline Delay (Latency)		IV			1	Clock Cycle
Output Delay		V		5		ns
Aperture Delay Time		V		1		ns
Aperture Jitter Time		V		5		ps-RMS
Dynamic Performance						
Effective Number of Bits						
f_{IN}=500 kHz				10.2		Bits
f_{IN}=1.0 MHz				10.0		Bits
f_{IN}=3.58 MHz				9.5		Bits

ELECTRICAL SPECIFICATIONS

T_A=T_{MIN} to T_{MAX}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, DV_{CC}=+5.0 V, V_{IN}=±2.0 V, V_{SB}=-2.0 V, V_{ST}=+2.0 V, f_{CLK}=10 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7910 MIN	SPT7910 TYP	SPT7910 MAX	UNITS
Dynamic Performance						
Signal-To-Noise Ratio (without Harmonics)						
f_{IN}=500 kHz	+25 °C	I	64	67		dB
	T_{MIN} to T_{MAX}	IV	58	61		dB
f_{IN}=1 MHz	+25 °C	I	64	66		dB
	T_{MIN} to T_{MAX}	IV	58	60		dB
f_{IN}=3.58 MHz	+25 °C	I	62	64		dB
	T_{MIN} to T_{MAX}	IV	58	60		dB
Harmonic Distortion[1]						
f_{IN}=500 kHz	+25 °C	I	63	66		dB
	T_{MIN} to T_{MAX}	IV	59	62		dB
f_{IN}=1.0 MHz	+25 °C	I	63	65		dB
	T_{MIN} to T_{MAX}	IV	59	61		dB
f_{IN}=3.58 MHz	+25 °C	I	59	61		dB
	T_{MIN} to T_{MAX}	IV	57	59		dB
Signal-to-Noise and Distortion						
f_{IN}=500 kHz	+25 °C	I	60	63		dB
	T_{MIN} to T_{MAX}	IV	55	58		dB
f_{IN}=1.0 MHz	+25 °C	I	60	62		dB
	T_{MIN} to T_{MAX}	IV	55	57		dB
f_{IN}=3.58 MHz	+25 °C	I	57	59		dB
	T_{MIN} to T_{MAX}	IV	54	56		dB
Spurious Free Dynamic Range[2]	+25 °C	V		74		dB
Differential Phase[3]	+25 °C	V		0.2		Degree
Differential Gain[3]	+25 °C	V		0.7		%
Digital Inputs						
Logic 1 Voltage		VI	-1.1			V
Logic 0 Voltage		VI			-1.5	V
Maximum Input Current Low		VI	-500	±200	+750	µA
Maximum Input Current High		VI	-500	±300	+750	µA
Pulse Width Low (CLK)		IV	30			ns
Pulse Width High (CLK)		IV	30		300	ns
Digital Outputs						
Logic 1 Voltage	50 Ω to -2 V	VI	-1.1	-0.8		V
Logic 0 Voltage	50 Ω to -2 V	VI		-1.8	-1.5	V
Power Supply Requirements						
Voltages V_{CC}		IV	+4.75		+5.25	V
$-V_{EE}$		IV	-4.95		-5.45	V
Currents I_{CC}		VI		150	190	mA
$-I_{EE}$		VI		125	160	mA
Power Dissipation	Outputs Open	VI		1.4	1.8	W
Power Supply Rejection Ratio	(5 V±0.25 V, -5.2 V ±0.25 V)	V		1.0		LSB

Typical thermal impedances (unsoldered, in free air): 32L sidebrazed DIP. θ_{ja} = 50 °C/W.

[1]64 distortion BINS from 4096 pt FFT.

[2]f_{IN} = 1 MHz.

[3]f_{IN} = 3.58 and 4.35 MHz.

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Figure 1A: Timing Diagram

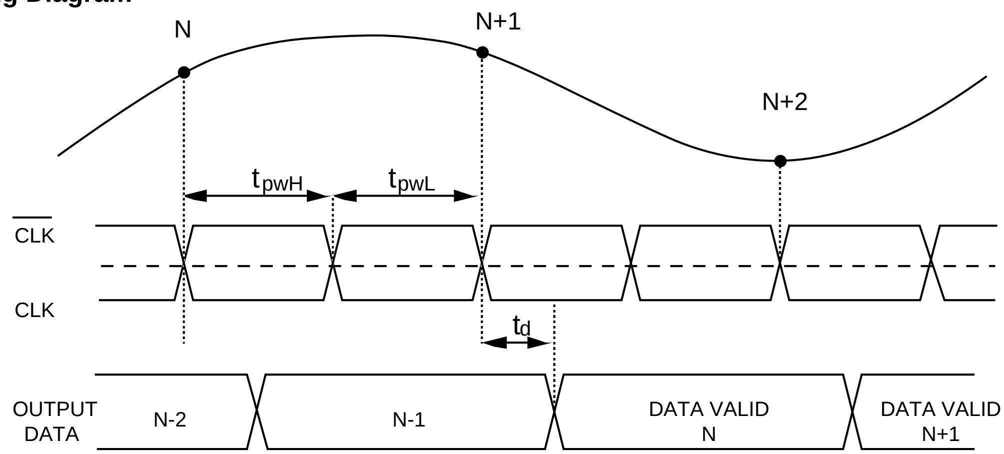


Figure 1B: Single Event Clock

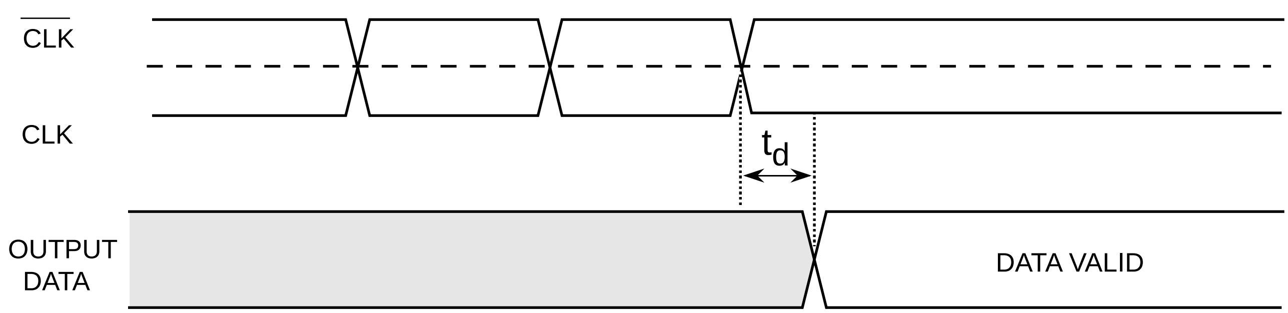


Table I - Timing Parameters

PARAMETERS	DESCRIPTION	MIN	TYP	MAX	UNITS
t_d	CLK to Data Valid Prop Delay	-	5		ns
t_{pwH}	CLK High Pulse Width	30	-	300	ns
t_{pwL}	CLK Low Pulse Width	30	-	-	ns

SPECIFICATION DEFINITIONS

APERTURE DELAY

Aperture delay represents the point in time, relative to the rising edge of the CLOCK input, that the analog input is sampled.

APERTURE JITTER

The variations in aperture delay for successive samples.

DIFFERENTIAL GAIN (DG)

A signal consisting of a sine wave superimposed on various DC levels is applied to the input. Differential gain is the maximum variation in the sampled sine wave amplitudes at these DC levels.

DIFFERENTIAL PHASE (DP)

A signal consisting of a sine wave superimposed on various DC levels that is applied to the input. Differential phase is the maximum variation in the sampled sine wave phases at these DC levels.

EFFECTIVE NUMBER OF BITS (ENOB)

SINAD = 6.02N + 1.76, where N is equal to the effective number of bits.

$$N = \frac{SINAD - 1.76}{6.02}$$

+/- FULL-SCALE ERROR (GAIN ERROR)

Difference between measured full scale response [(+Fs) - (-Fs)] and the theoretical response (+4 V -2 LSBs) where the +FS (full scale) input voltage is defined as the output transition between 1-10 and 1-11 and the -FS input voltage is defined as the output transition between 0-00 and 0-01.

INPUT BANDWIDTH

Small signal (50 mV) bandwidth (3 dB) of analog input stage.

DIFFERENTIAL NONLINEARITY (DNL)

Error in the width of each code from its theoretical value. (Theoretical = $V_{FS}/2^N$)

INTEGRAL NONLINEARITY (INL)

Linearity error refers to the deviation of each individual code (normalized) from a straight line drawn from -Fs through +Fs. The deviation is measured from the edge of each particular code to the true straight line.

OUTPUT DELAY

Time between the clock's triggering edge and output data valid.

OVERVOLTAGE RECOVERY TIME

The time required for the ADC to recover to full accuracy after an analog input signal 125% of full scale is reduced to 50% of the full-scale value.

SIGNAL-TO-NOISE RATIO (SNR)

The ratio of the fundamental sinusoid power to the total noise power. Harmonics are excluded.

SIGNAL-TO-NOISE AND DISTORTION (SINAD)

The ratio of the fundamental sinusoid power to the total noise and distortion power.

TOTAL HARMONIC DISTORTION (THD)

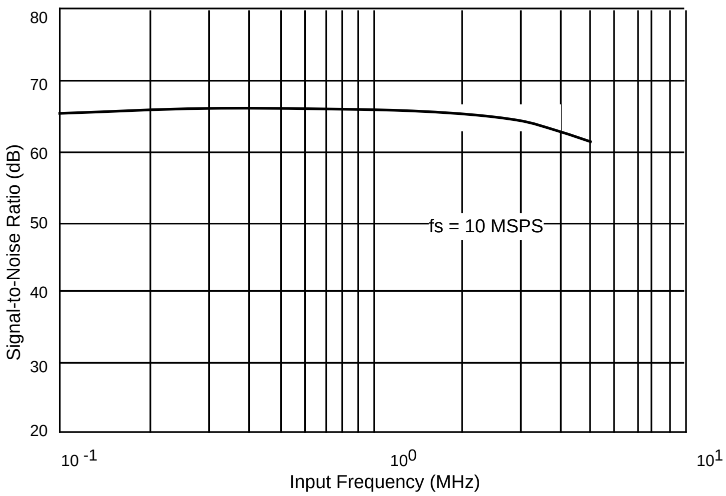
The ratio of the total power of the first 64 harmonics to the power of the measured sinusoidal signal.

SPURIOUS FREE DYNAMIC RANGE (SFDR)

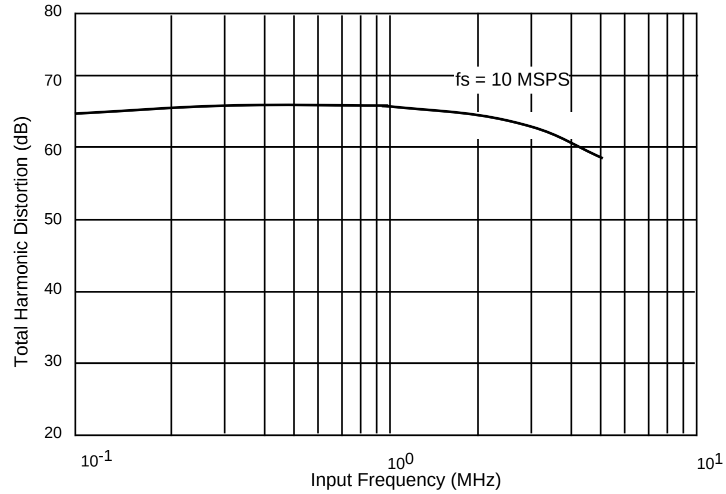
The ratio of the fundamental sinusoidal amplitude to the single largest harmonic or spurious signal.

TYPICAL PERFORMANCE CHARACTERISTICS

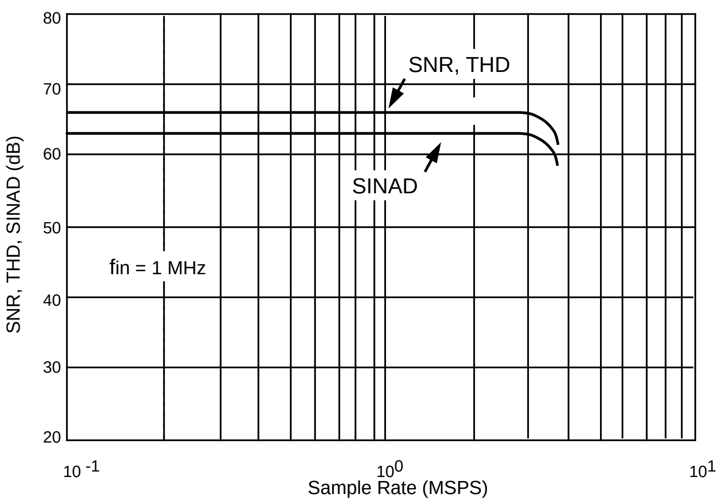
SNR vs Input Frequency



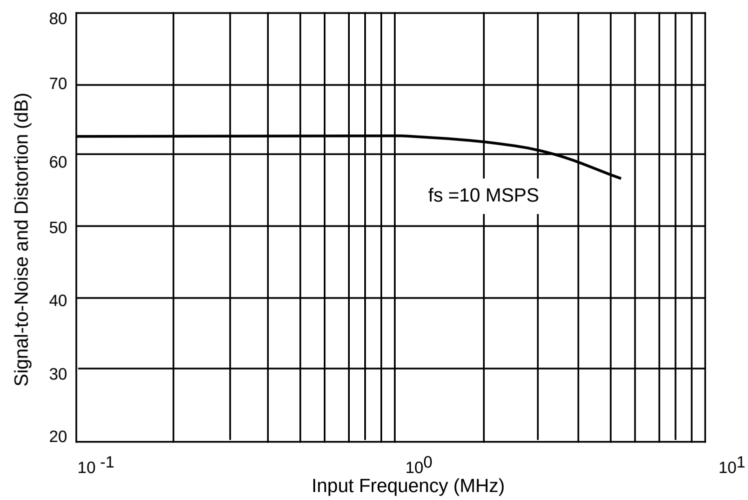
THD vs Input Frequency



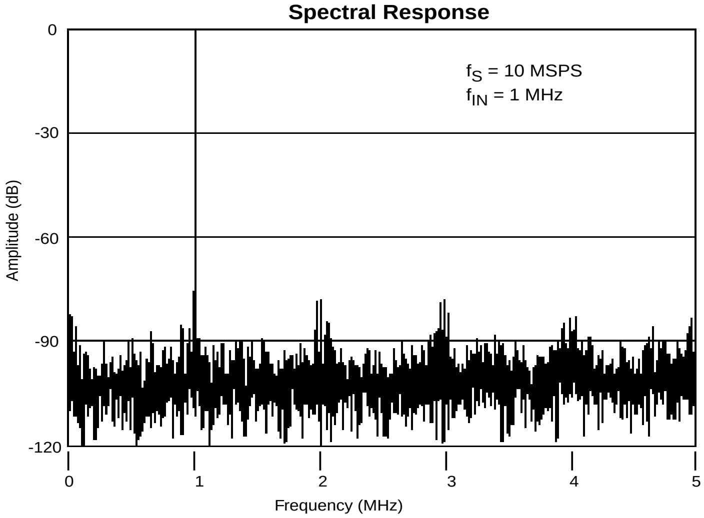
SNR, THD, SINAD vs Sample Rate



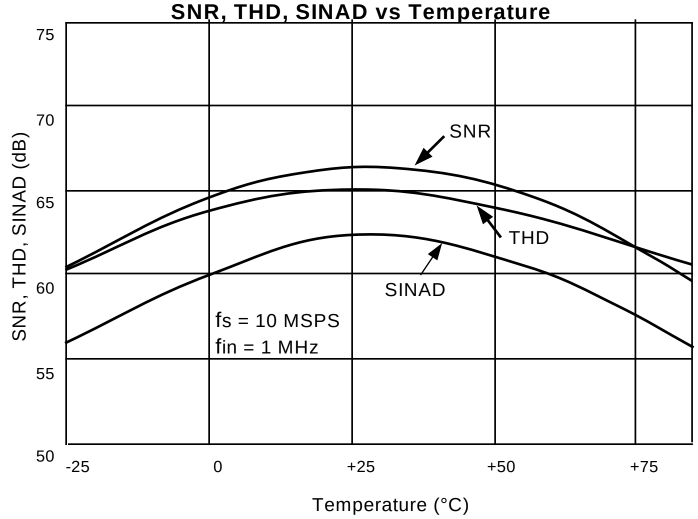
SINAD vs Input Frequency



Spectral Response



SNR, THD, SINAD vs Temperature



TYPICAL INTERFACE CIRCUIT

The SPT7910 requires few external components to achieve the stated operation and performance. Figure 2 shows the typical interface requirements when using the SPT7910 in normal circuit operation. The following section provides a description of the pin functions and outlines critical performance criteria to consider for achieving the optimal device performance.

POWER SUPPLIES AND GROUNDING

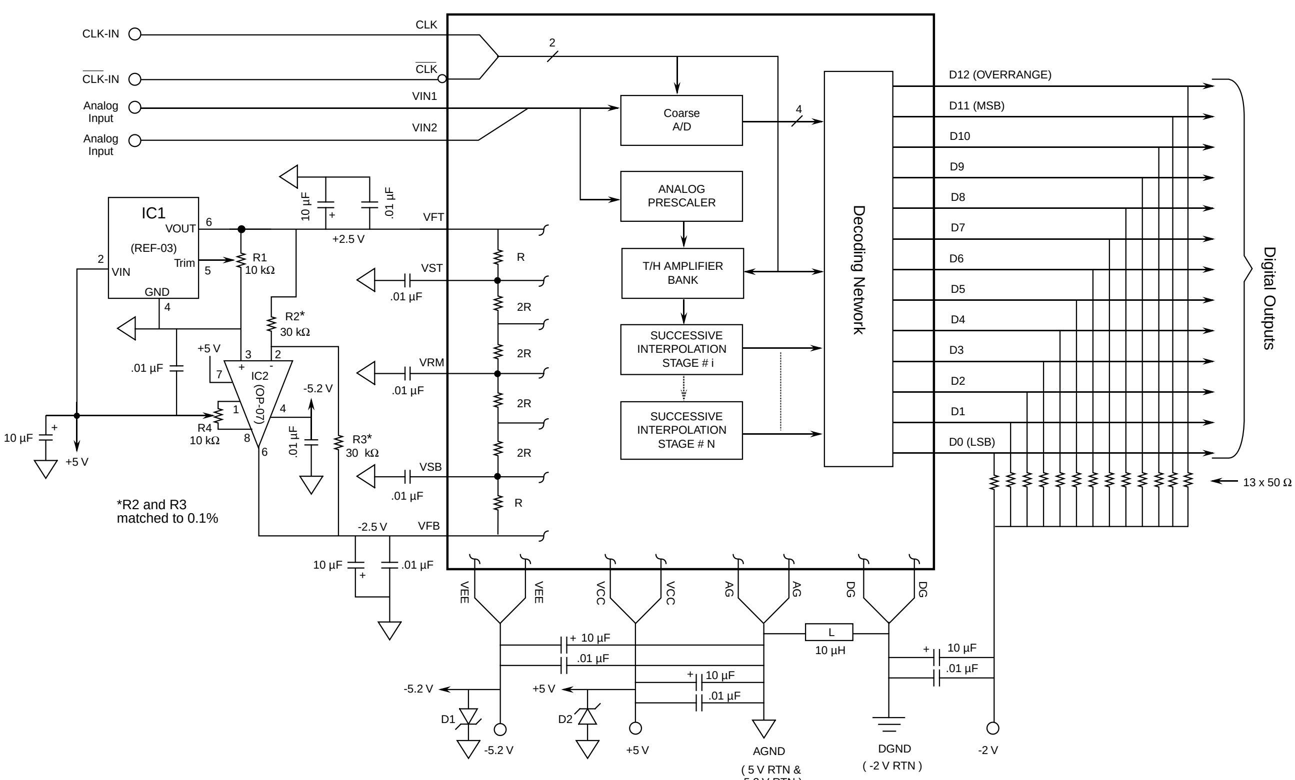
The SPT7910 requires the use of two supply voltages, V_{EE} and V_{CC}. Both supplies should be treated as analog supply sources. This means the V_{EE} and V_{CC} ground returns of the device should both be connected to the analog ground plane. All other -5.2 V requirements of the external digital logic circuit should be connected to the digital ground plane. Each power supply pin should be bypassed as closely as possible to the device with .01 µF and 10 µF capacitors as shown in figure 2.

The two grounds available on the SPT7910 are AGND and DGND. DGND is used only for ECL outputs and is to be referenced to the output pulldown voltage. These grounds are not tied together internal to the device. The use of ground planes is recommended to achieve the best performance of the SPT7910. The AGND and the DGND ground planes should be separated from each other and only connected together at the device through an inductance or ferrite bead. Doing this will minimize the ground noise pickup.

VOLTAGE REFERENCE

The SPT7910 requires the use of two voltage references: V_{FT} and V_{FB}. V_{FT} is the force for the top of the voltage reference ladder (+2.5 V typ), V_{FB} (-2.5 V typ) is the force for the bottom of the voltage reference ladder. Both voltages are applied across an internal reference ladder resistance of 800 ohms. In addition, there are five reference ladder taps (V_{ST},V_{RT1}, V_{RT2}, V_{RT3}, and V_{SB}). V_{ST} is the sense for the top of the reference ladder (+2.0 V), V_{RT2} is the midpoint of the ladder (0.0 V typ) and V_{SB} is the sense for the bottom of the reference ladder (-2.0 V). V_{RT1} and V_{RT3} are quarter point ladder taps (+1.0 and -1.0 V typical, respectively). The voltages seen at V_{ST} and V_{SB} are the true full scale input voltages of the device when V_{FT} and V_{FB} are driven to the recommended voltages (+2.5 V and -2.5 V typical respectively). V_{ST} and V_{SB} should be used to monitor the actual full scale input voltage of the device. V_{RT1}, V_{RT2} and V_{RT3} should not be driven to the expected ideal values as is commonly done with standard flash converters. When not being used, a decoupling capacitor of .01 uF connected to AGND from each tap is recommended to minimize high frequency noise injection.

Figure 2 - Typical Interface Circuit



NOTE: D1=D2=1N5817 or equivalent. (Used to prevent damage caused by power sequencing.)

The analog input range will scale proportionally with respect to the reference voltage if a different input range is required. The maximum scaling factor for device operation is ± 20% of the recommended reference voltages of V_{FT} and V_{FB}. However, because the device is laser trimmed to optimize performance with V_{SB} and V_{ST} equal to -2.0 V and +2.0 V respectively, the accuracy of the device will degrade if operated beyond a ± 2% range.

The following errors are defined:

+FS error = top of ladder offset voltage = $\Delta(+FS - V_{ST})$
-FS error = bottom of ladder offset voltage = $\Delta(-FS - V_{SB})$

Where the +FS (full scale) input voltage is defined as the input approximately 1 LSB above the output transition of 1—10 and 1—11 and the -FS input voltage is defined as the input approximately 1 LSB below the output transition of 0—00 and 0—01.

An example of a reference driver circuit recommended is shown in figure 2. IC1 is REF-03, the +2.5 V reference with a tolerance of 0.6% or ± 0.015 V. The potentiometer R1 is 10 kΩ and supports a minimum adjustable range of up to 150 mV. IC2 is recommended to be an OP-07 or equivalent device. R2 and R3 must be matched to within 0.1% with good TC tracking to maintain a 0.3 LSB matching between V_{FT} and V_{FB}. If 0.1% matching is not met, then potentiometer R4 can be used to adjust the V_{FB} voltage to the desired level. R1 and R4 should be adjusted such that V_{ST} and V_{SB} are exactly +2.0 V and -2.0 V respectively.

ANALOG INPUT

V_{IN1} and V_{IN2} are the analog inputs. Both inputs are tied to the same point internally. Either one may be used as an analog input sense and the other for an input force. The inputs can also be tied together and driven from the same source. The full scale input range will be 80% of the reference voltage or ±2 volts with V_{FB}=-2.5 V and V_{FT}=+2.5 V.

The drive requirements for the analog inputs are minimal when compared to conventional Flash converters due the SPT7910's extremely low input capacitance of only 5 pF and very high input impedance of 300 kΩ. For example, for an input signal of ± 2 V p-p with an input frequency of 10 MHz, the peak output current required for the driving circuit is only 628 µA.

CLOCK INPUT

The clock inputs (CLK, $\overline{CLK}$) are designed to be driven differentially with ECL levels. Differential clock driving is highly recommended to minimize the effects of clock jitter. The clock may be driven single ended since $\overline{CLK}$ is internally biased to -1.3 V. $\overline{CLK}$ may be left open, but a .01 µF bypass capacitor to AGND is recommended. As with all high speed circuits, proper terminations are required to avoid signal reflections and possible ringing that can cause the device to trigger at an unwanted time.

The clock input duty cycle should be 50% where possible, but performance will not be degraded if kept within the range of 40-60%. However, in any case the clock pulse width (tpwH) must be kept at 300 ns maximum to ensure proper operation of the internal track and hold amplifier. (See the timing diagram.) The analog input signal is latched on the rising edge of the CLK.

DIGITAL OUTPUTS

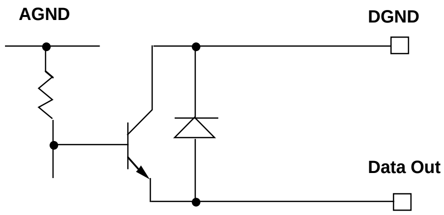
The format of the output data (D0-D11) is straight binary. (See table II.) These outputs are ECL 10K and 10KH compatible with the output circuit shown in figure 3. The outputs are latched on the rising edge of CLK with a propagation delay of 5 ns. There is a one clock cycle latency between CLK and the valid output data (see timing diagram). These digital outputs can drive 50 ohms to ECL levels when pulled down to -2 V. Output loading pulled down to -5.2 V is not recommended. The total specified power dissipation of the device does not include the power used by these loads. The additional power used by these loads can vary between 10 and 300 mW typically (including the overrange load) depending on the output codes. If lower power levels are desired, the output loads can be reduced, but careful consideration to the resistive and capacitive loads in relation to the operating frequency must be considered.

Table II - Output Data Information

ANALOG INPUT	OVERRANGE D12	OUTPUT CODE D11-DO
>+2.0 V + 1/2 LSB	1	1111 1111 1111
+2.0 V -1 LSB	O	1111 1111 111Ø
0.0 V	O	ØØØØ ØØØØ ØØØØ
-2.0 V +1 LSB	O	OOOO OOOO OOOØ
<-2.0 V	O	OOOO OOOO OOOO

(Ø indicates the flickering bit between logic 0 and 1).

Figure 3 - Output Circuit



OVERRANGE OUTPUT

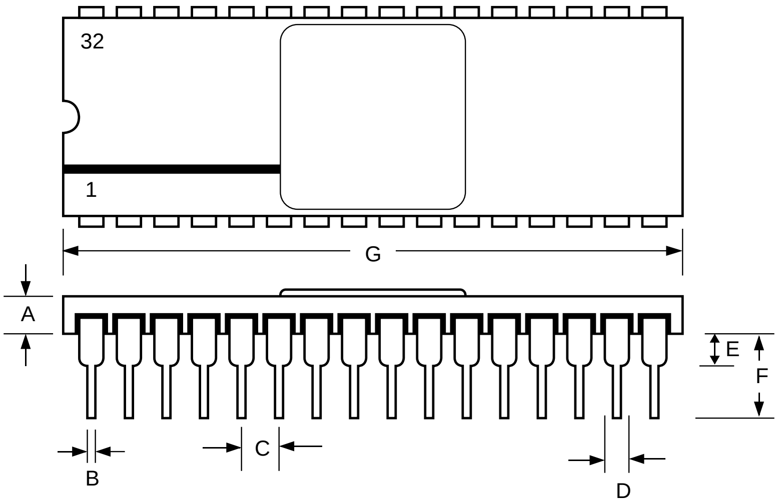
The OVERRANGE OUTPUT (D12) is an indication that the analog input signal has exceeded the full scale input voltage by 1 LSB. When this condition occurs, the output will switch to logic 1. All other data outputs are unaffected by this operation. This feature makes it possible to include the SPT7910 into higher resolution systems.

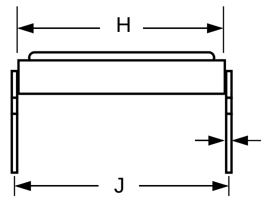
EVALUATION BOARD

The EB7910 Evaluation Board is available to aid designers in demonstrating the full performance of the SPT7910. This board includes a reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. An application note (AN7910) describing the operation of this board as well as information on the testing of the SPT7910 is also available. Contact the factory for price and availability.

PACKAGE OUTLINE

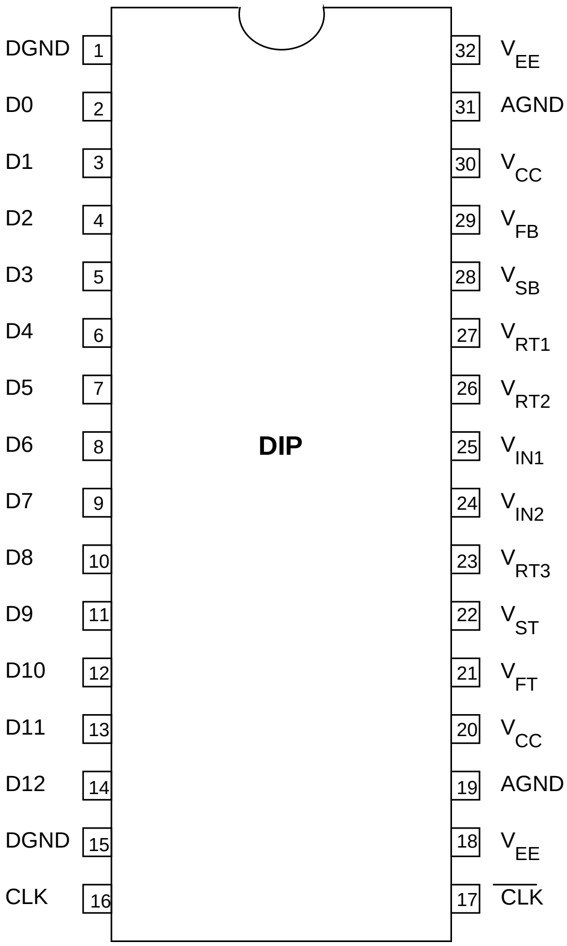
32-Lead Sidebrazed





SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.081	0.099	2.06	2.51
B	0.016	0.020	0.41	0.51
C	0.095	0.105	2.41	2.67
D		.050 typ		1.27
E	0.040		1.02	5.72
F	0.175	0.225	4.45	41.15
G	1.580	1.620	40.13	15.37
H	0.585	0.605	14.86	0.30
I	0.009	0.012	0.23	15.75
J	0.600	0.620	15.24	15.75

PIN ASSIGNMENTS



PIN FUNCTIONS

NAME	FUNCTION
DGND	Digital Ground
AGND	Analog Ground
D0-D11	ECL Outputs (D0=LSB)
D12	ECL Output Overrange
CLK	Clock
$\overline{CLK}$	Inverted Clock
V_{EE}	-5.2 V Supply
V_{CC}	+5.0 V supply
V_{RT1},V_{RT2},V_{RT3}	Voltage Reference Taps
V_{IN1}, V_{IN2}	Inputs (tied together at the die)
V_{FT}	Force for Top of Reference Ladder
V_{ST}	Sense for Top of Reference Ladder
V_{FB}	Force for Bottom of Reference Ladder
V_{SB}	Sense for Bottom of Reference Ladder

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
SPT7910SCJ	0 to +70 °C	32L Sidebrazed DIP
SPT7910SCU	+25 °C	Die*

*Please see the die specification for guaranteed electrical performance.

WARNING - LIFE SUPPORT APPLICATIONS POLICY - SPT products should not be used within Life Support Systems without the specific written consent of SPT. A Life Support System is a product or system intended to support or sustain life which, if it fails, can be reasonably expected to result in significant personal injury or death.

Signal Processing Technologies believes that ultrasonic cleaning of its products may damage the wire bonding, leading to device failure. It is therefore not recommended, and exposure of a device to such a process will void the product warranty.