

CCLD-912 Model
9X14 mm SMD, 3.3V, LVDS



Differential LVDS Clock Oscillator

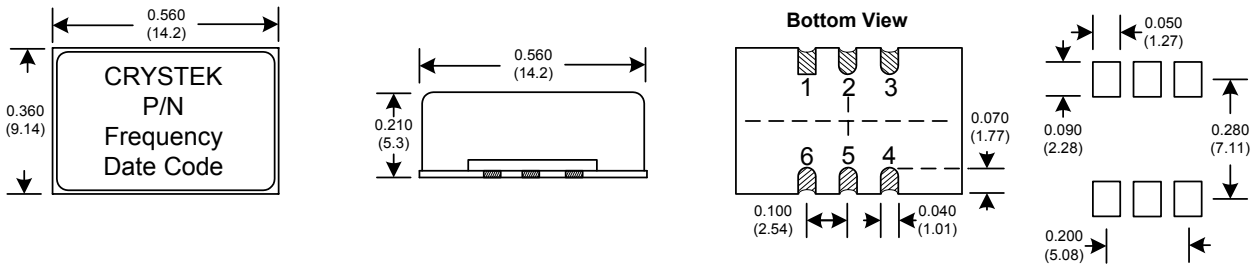


Frequency Range: 77.760MHz to 161MHz
Frequency Stability: ±25ppm to ±100ppm
Temperature Range: 0°C to 70°C
 (Option M) -20°C to 70°C
 (Option X) -40°C to 85°C
Storage: -55°C to 120°C
Input Voltage: 3.3V ± 0.3V
Input Current: 35mA Typ, 47mA Max
Output: Differential LVDS
 Symmetry: 45/55% Max @ 50% Vdd
 Rise/Fall Time: 1ns Max @ 20% to 80% Vdd
 Load: 100 Ohms Connected between OUT and COUT
 Logic: Output Voltage Levels "0" = 1.10V Typical, 0.90V Min
 "1" = 1.45V Typical, 1.65V Max
 Disable Time 200ns Max
 Enable Time 200ns Max
Jitter: 12KHz to 20MHz 1ps RMS Max

Designed to meet today's requirements for 3.3V LVDS applications. The CCLD-912 is a very low noise, low jitter clock oscillator. Also available in 2.5V model. Available on tape and reel in quantities of 500ea.

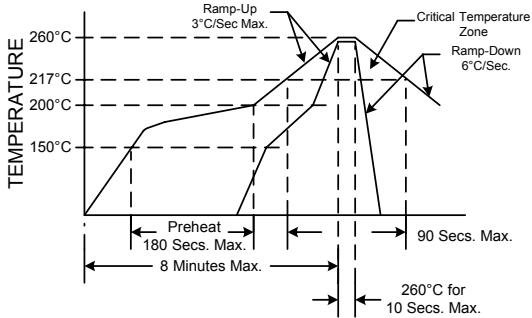
Aging: <3ppm 1st/yr, 1ppm every year thereafter

SUGGESTED PAD LAYOUT



Bypass Capacitor Recommended

RECOMMENDED REFLOW SOLDERING PROFILE



NOTE: Reflow Profile with 240°C peak also acceptable.

Pad	Connection
1	E/D
2	N/C
3	GND
4	OUT
5	COUT
6	Vdd

Table 2

Crystek Part Number Guide

CCLD-912 X - 25 - 155.520

#1 Crystek 9X14 SMD LVDS Osc.
 #2 Model 912 = 77.760MHz ~ 161MHz
 #3 Temp. Range: Blank = 0/70°C, M= -20/70°C, X= -40/85°C
 #4 Stability: (see Table 1)
 #5 Frequency in MHz: 3 or 6 decimal places

Stability Indicator:	
Blank (std)	± 100ppm
50	± 50ppm
25	± 25ppm

Table 1

Example:
 CCLD-912X-25-155.520 = 3.3V, 45/55, -40/85°C, 25ppm, 155.520 MHz

Tri-State Function	
E/D pin	Output pin
Open	Active
"1" level 0.7V Min	Active
"0" level 0.3V Max	High Z

Table 3

Specifications subject to change without notice.

TD-031103 Rev.B