

16 BIT LVTTTL TO GTL/GTL + UNIVERSAL BUS TRANSCEIVERS WITH LIVE INSERTION

- HIGH SPEED GTL/GTL+ UNIVERSAL TRANSCEIVER:
 $t_{PD} = 4.6 \text{ ns (MAX.) A to B at } V_{CC} = 3V$
- COMBINES D-TYPE LATCHES AND D-TYPE FLIP-FLOPS FOR OPERATION IN TRANSPARENT, LATCHED, OR CLOCKED MODE
- OPERATING VOLTAGE RANGE:
 $V_{CC(OPR)} = 3.0V \text{ to } 3.6V$
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 24mA \text{ (MIN) at } V_{CC} = 3V \text{ (A PORT)}$
- OUTPUT IMPEDANCE:
 $I_{OL} = 100mA \text{ (MIN) at } V_{CC} = 3V \text{ (B PORT)}$
- HIGH-IMPEDANCE STATE DURING POWER UP AND POWER DOWN up to $V_{CC} = \text{BIAS} V_{CC} = 1.5V$ PERMIT LIVE INSERTION
- B-PORT PRECHARGED BY $\text{BIAS} V_{CC}$ REDUCE NOISE ON THE LINE DURING LIVE INSERTION
- EDGE RATE-CONTROL INPUT CONFIGURES THE B-PORT OUTPUT RISE AND FALL TIMES
- BUS HOLD ON DATA INPUTS ELIMINATES THE NEED FOR EXTERNAL PULL-UP/ PULL-DOWN RESISTORS (A PORT)
- DISTRIBUTED V_{CC} AND GND PIN CONFIGURATION MINIMIZES HIGH-SPEED SWITCHING NOISE IN PARALLEL COMMUNICATIONS
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 1655

DESCRIPTION

The 74GTL1655A devices are 16-bit high-drive (100mA), low-output-impedance universal bus transceivers designed for backplane applications. The 74GTL1655A devices provide live-insertion capability for backplane applications by tolerating active signals on the data ports when the devices are powered off. In addition, a biasing pin preconditions the GTL/GTL+ port to minimize disruption to an active backplane. The edge rate-control (V_{ERC}) input is provided so the rise and fall time of the B outputs can be configured to optimize for various backplane loading conditions. Data flow in each direction is

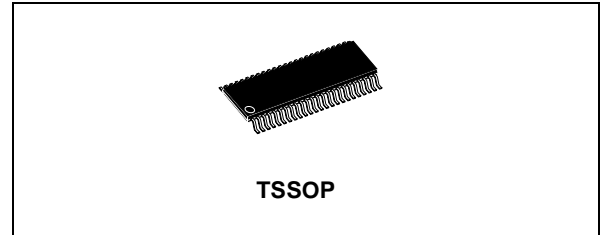
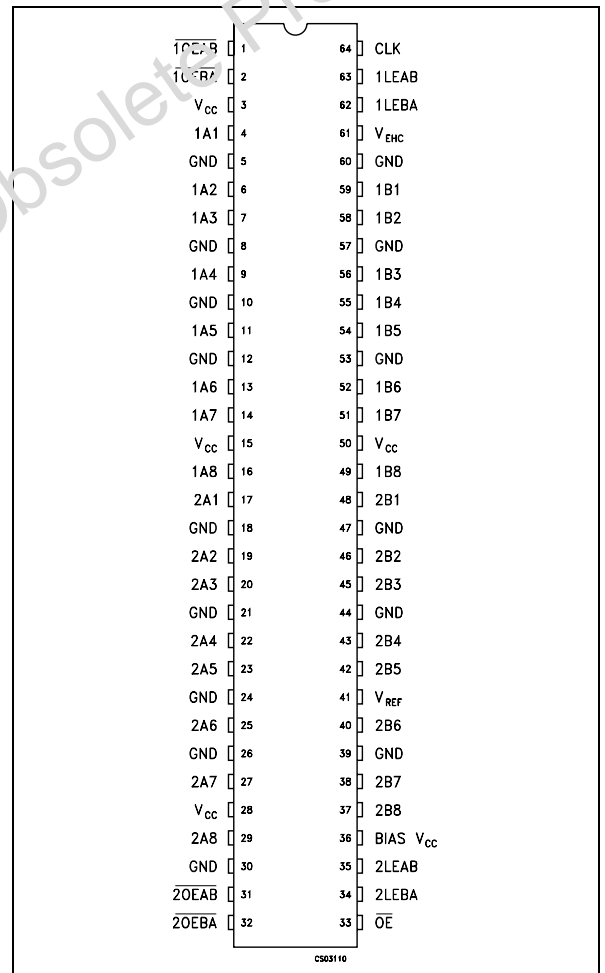


Table 1: Order Codes

PACKAGE	T & P
TSSOP	74GTL1655A1TR

Figure 1: Pin Connection



controlled by output-enable (\overline{OEAB} and \overline{OEBA}), latch-enable (LEAB and LEBA), and clock (CLK) inputs. For A-to-B data flow, the devices operate in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLK is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When \overline{OEAB} is low, the outputs are active. When \overline{OEAB} is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B, but uses \overline{OEBA} , LEBA, and CLK. The output enable (\overline{OE}) is used to disable both ports simultaneously.

Active bus-hold circuitry is provided on the A port to hold unused or floating data inputs at a valid logic level. When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5V, \overline{OE} should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

All input and output are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

Figure 2: Input And Output Equivalent Circuit

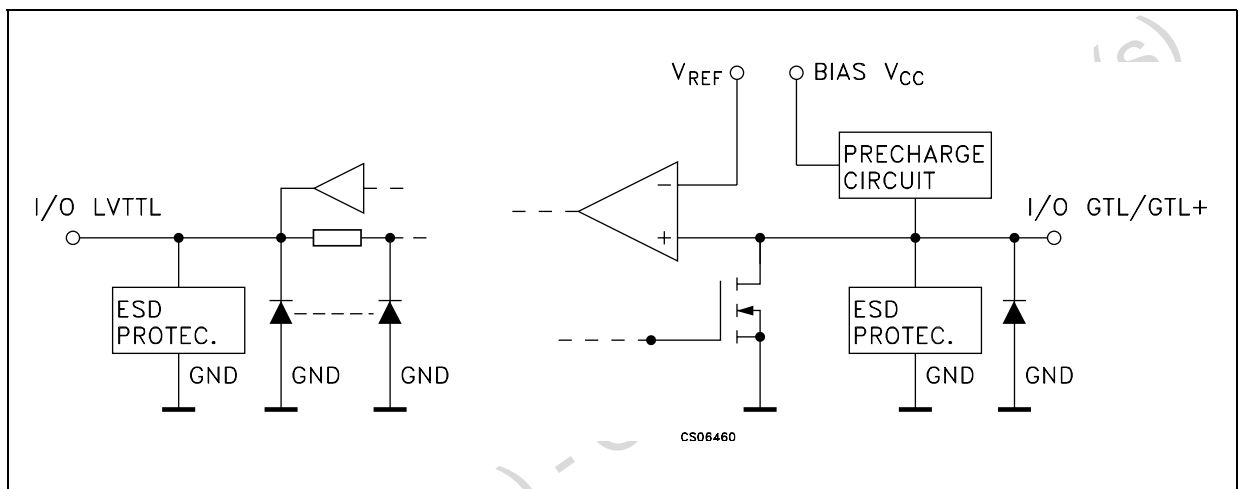




Table 2: Pin Description

PIN N°	SYMBOL	NAME AND FUNCTION
1, 2	1OEAB, 1OEBA	Output Enable Input
4, 6, 7, 9, 11, 13, 14, 16	1A1 to 1A8	Data Inputs/Outputs LVTTL
17, 19, 20, 22, 23, 25, 27, 29	2A1 to 2A8	Data Inputs/Outputs LVTTL
31, 32	2OEAB, 2OEBA	Output Enable Input
33	\overline{OE}	Output Enable Input
34, 35	2LEBA, 2LEAB	Latch Enable
36	BIAS V_{CC}	Pre-Charge Supply Voltage
37, 38, 40, 42, 43, 45, 46, 48	2B8 to 2B1	Data Inputs/Outputs GTL/GTL+
41	V_{REF}	GTL Voltage Reference Input
49, 51, 52, 54, 55, 56, 58, 59	2A1 to 2A8	Data Inputs/Outputs GTL/GTL+
61	V_{ERC}	Edge Rate Control
62, 63	1LEBA, 1LEAB	Latch Enable
64	CLK	Clock Input (LOW to HIGH edge triggered)
5, 8, 10, 12, 18, 21, 24, 26, 30, 39, 44, 47, 53, 57, 60	GND	Ground (0V)
3, 15, 28, 50	V_{CC}	Positive Supply Voltage

Table 3: Function Table (1)

INPUTS				OUTPUT	MODE
$\overline{\text{OEAB}}$	LEAB	CLK	A	B	
H	X	X	X	Z	Isolation
L	H	X	L	L	Transparent
L	H	X	H	H	Transparent
L	L		L	L	Registered
L	L		H	H	Registered
L	L	H	X	B0 ⁽²⁾	Previous State
L	L	L	X	B0 ⁽³⁾	Previous State

1) A to B data flow is shown. B to A flow is similar, but uses $\overline{\text{OEBA}}$, LEBA and CLK

2) Output level before the indicated steady-state input conditions were established, provided that CLK was high before LEAB went low

3) Output level before the indicated steady-state input conditions were established

Table 4: Output Enable Truth Table

INPUTS			OUTPUTS	
$\overline{\text{OE}}$	$\overline{\text{OEAB}}$	$\overline{\text{OEBA}}$	A PORT	B PORT
L	L	L	Active	Active
L	L	H	Z	Active
L	H	L	Active	Z
L	H	H	Z	Z
H	X	X	Z	Z

Table 5: B-Port Edge Rate Control (V_{ERC}) Truth Table

INPUT V_{ERC}		OUTPUT B PORT EDGE RATE
LOGIC LEVEL	NOMINAL VOLTAGE	
H	V_{CC}	Slow
L	GND	Fast

Figure 3: Logic Diagram

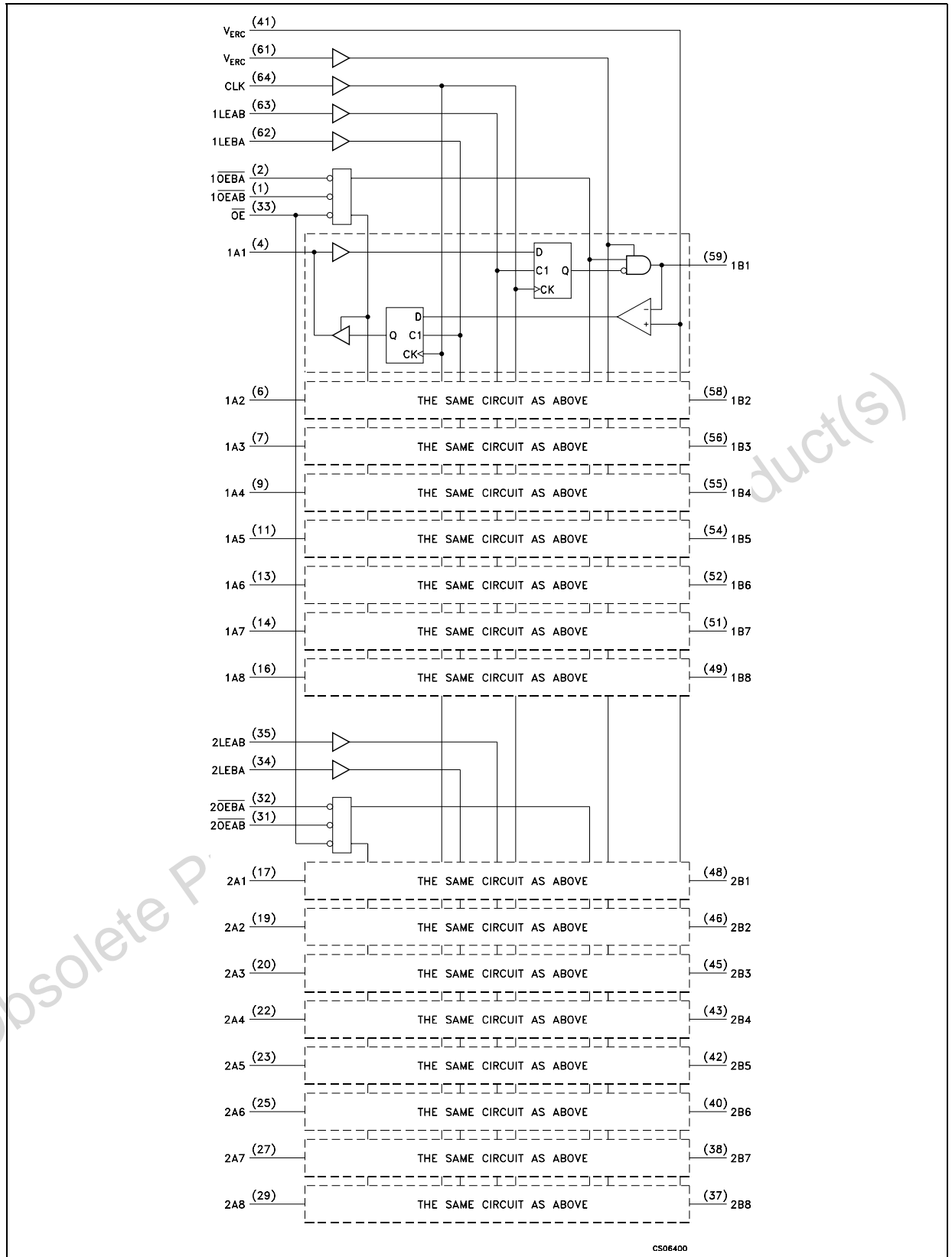


Table 6: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage, Bias V_{CC}	-0.5 to +4.6	V
V_{IA}	DC Input Voltage A Side, Control Input	-0.5 to +4.6	V
V_{IB}	DC Input Voltage B Side, V_{ERC} , V_{REF}	-0.5 to +4.6	V
V_{OA}	DC Output Voltage A Side	-0.5 to +4.6	V
V_{OB}	DC Output Voltage B Side	-0.5 to +4.6	V
I_{IK}	DC Input Diode Current	- 50	mA
I_{OK}	DC Output Diode Current	- 50	mA
I_{OA}	DC Output Current A Side	\pm 48	mA
I_{OB}	DC Output Current B Side in the Low State	200	mA
T_{stg}	Storage Temperature	-65 to +150	$^{\circ}$ C
T_L	Lead Temperature (10 sec)	300	$^{\circ}$ C

Absolute Maximum Rating are those value beyond which damage to the device may occur. Functional operation under these condition is not implied

Table 7: Recommended Operating Conditions

Symbol	Parameter	Value			Unit	
		Min.	Typ.	Max.		
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	
V_{TT}	Termination Voltage	GTL	1.14	1.2	1.26	V
		GTL+	1.35	1.5	1.65	
V_{REF}	Supply Voltage	GTL	0.74	0.8	0.87	V
		GTL+	0.87	1	1.1	
V_I	Input Voltage	B port	0		V_{TT}	V
		other	0		V_{CC}	
V_{IH}	High Level Input Voltage	B port	$V_{REF}+0.05$			V
		other	2			
V_{IL}	Low Level Input Voltage	B port			$V_{REF}-0.05$	V
		other			0.8	
I_{IK}	Input Clamp Current			-18	mA	
I_{OH}	High Level Output Current	A port			-24	mA
I_{OL}	Low Level Output Current	A port			24	mA
		B port			100	
dt/dV_{CC}	Power -up ramp rate		200		μ s/V	
T_{op}	Operating Temperature		-40		85	$^{\circ}$ C

1) V_{TT} and R_{TT} can be adjusted to adapt backplane impedance if DC recommended I_{OL} ratings are not exceeded

2) V_{REF} can be adjusted to optimize noise margin (typ two-thirds V_{TT})

Table 8: DC Specifications

Symbol	Parameter		Test Condition		Value			Unit
			V _{CC} (V)		-40 to 85 °C			
					Min.	Typ.	Max.	
V _{IK}	High Level Input Voltage		3				-1.2	V
V _{OHA}	High Level Output Voltage A Port		3 to 3.6	I _O =-100μA	V _{CC} -0.2			V
			3	I _O =-12mA	2.4			
			3	I _O =-24mA	2.2			
V _{OLA}	Low Level Output Voltage A Port		3 to 3.6	I _O =100μA			0.2	V
			3	I _O =12mA			0.4	
			3	I _O =24mA			0.55	
V _{OLB}	Low Level Output Voltage B Port		3	I _O =40mA			0.2	V
			3	I _O =80mA			0.4	
			3	I _O =100mA			0.5	
I _I	Input Current	Control	3.6	V _I = V _{CC} or GND			±10	μA
		B Port	3.6	V _I = V _{TT} or GND			±10	μA
I _{off}	Power Off Leakage Current		0	V _I or V _O = 0 to 3.6V			±100	μA
I _{I(HOLD)}	Bus Hold A Port Input Current		3	V _I = 0.8V	75		20	μA
			3	V _I = 2V	-75			
			3.6	V _I = 0 to V _{CC}			± 500	
I _{OZHB}	3-State Output Current B Port		3.6	V _O = 1.5V			10	μA
I _{OZLB}	3-State Output Current B Port		3.6	V _O = 0.4V			-10	μA
I _{OZ} (*)	3-State Output Current A Port		3.6	V _O = V _{CC} or GND			±10	μA
I _{OZPU} **	3-State Output Current A Port		0 to 1.5	V _O = 0.5 to 3V OE = LOW			±50	μA
I _{OZPD} **	3-State Output Current A Port		1.5 to 0	V _O = 0.5 to 3V OE = LOW			±50	μA
I _{CC}	Quiescent Supply Current		3.6	V _I = V _{CC} or GND I _O =0		10	40	mA
ΔI _{CC}	Δ Supply Current except B port		3.6	V _{IN} = V _{CC} or GND One input V _{CC} = 0.6V			1	mA
C _I	Control Input Capacitance			V _{IN} = V _{CC} or GND		3	5	pF
C _O	Input Capacitance A Port			V _O = V _{CC} or GND		5	6	pF
	Input Capacitance B Port						6	

(*) For I/O ports, the parameter I_{OZ} includes the input leakage current

(**) Is also guaranteed when connecting BiasV_{CC} with V_{CC}.

Table 9: Live Insertion Specifications

Symbol	Parameter	Test Condition		Value			Unit
		V _{CC} (V)		-40 to 85 °C			
				Min.	Typ.	Max.	
I _{CC} (Bias V _{CC})	Quiescent Bias Current	0 to 3.0	V _{O(Bport)} = 0 to 1.2V			5	mA
		3 to 3.6	V _{I(Bias V_{CC})} = 3 to 3.6V			10	μA
V _O	Output Voltage B Port	0	V _{I(Bias V_{CC})} = 3.3V	1		1.2	V
I _O	Output Current B Port	0	V _{O(Bport)} = 0.4V V _{I(Bias V_{CC})} = 3 to 3.6V	-1			μA
		0 to 3.6	OE = 3.3V			100	μA
		0 to 1.5	OE = 0 to 3.3V			100	μA

Table 10: AC Electrical Characteristics for GTL

(V_{CC}=3.3 ± 0.3V, V_{TT}=1.2V, V_{REF}=0.8V, V_{ERC}=V_{CC} or GND)

Symbol	Parameter	Test Condition	Value			Unit
			-40 to 85 °C			
			Min.	Typ.	Max.	
f _{MAX}	Maximum Frequency A to B or B to A		160			MHz
t _{PLH}	Propagation Delay Time A to B	V _{ERC} =V _{CC} R _L =12.5Ω C _L =30pF	1.5		5.2	ns
t _{PHL}			1.5		6.2	
t _{PLH}	Propagation Delay Time CK to B	V _{ERC} =V _{CC} R _L =12.5Ω C _L =30pF	1.5		5.5	ns
t _{PHL}			1.5		5.8	
t _{PLH}	Propagation Delay Time LEAB to B	V _{ERC} =V _{CC} R _L =12.5Ω C _L =30pF	1.5		5.8	ns
t _{PHL}			1.5		6.4	
t _{EN}	Enable Delay Time OEAB or OE to B	V _{ERC} =V _{CC} R _L =12.5Ω C _L =30pF	1.5		5.4	ns
t _{DIS}	Disable Delay Time OEAB or OE to B		1.5		6.2	
t _{PLH}	Propagation Delay Time A to B	V _{ERC} =GND R _L =12.5Ω C _L =30pF	1.5		4.3	ns
t _{PHL}			1.5		4.6	
t _{PLH}	Propagation Delay Time CK to B	V _{ERC} =GND R _L =12.5Ω C _L =30pF	1.5		4.3	ns
t _{PHL}			1.5		4.9	
t _{PLH}	Propagation Delay Time LEAB to B	V _{ERC} =GND R _L =12.5Ω C _L =30pF	1.5		4.9	ns
t _{PHL}			1.5		4.8	
t _{EN}	Enable Delay Time OEAB or OE to B	V _{ERC} =GND R _L =12.5Ω C _L =30pF	1.5		4.8	ns
t _{DIS}	Disable Delay Time OEAB or OE to B		1.5		4.2	
t _{PLH}	Propagation Delay Time B to A	R _L =500Ω C _L =50pF	1.5		4.7	ns
t _{PHL}			1.5		4.8	
t _{PLH}	Propagation Delay Time CK to A	R _L =500Ω C _L =50pF	1.5		4	ns
t _{PHL}			1.5		4	
t _{PLH}	Propagation Delay Time LEBA to A	R _L =500Ω C _L =50pF	1.5		4	ns
t _{PHL}			1.5		3.7	

Symbol	Parameter	Test Condition	Value			Unit	
			-40 to 85 °C				
			Min.	Typ.	Max.		
t_{EN}	Enable Delay Time OEBA or OE to A	$R_L=500\Omega$ $R_1=500\Omega$ $C_L=50pF$	1		4.6	ns	
t_{DIS}	Disable Delay Time OEBA or OE to A		1		6.1		
t_{SU}	Set-up Time	Data before clock	2.7			ns	
		Data before LE	Ck High	2.8			
			Ck Low	2.6			
t_H	Hold Time	Data after clock	0.4			ns	
		Data after LE Ck High or LOW	0.9				
t_W	Pulse duration	LE High	3			ns	
		CK High or Low	3				
Slew rate	Slew rate B output both transition (0.6 to 1.3V)	$V_{ERC}=V_{CC}$			1	ns/V	
		$V_{ERC}=GND$			1		
t_{sk}	Skew between drivers (in the same package)	Switching in the same direction			1	ns	
		Switching in any direction			1		

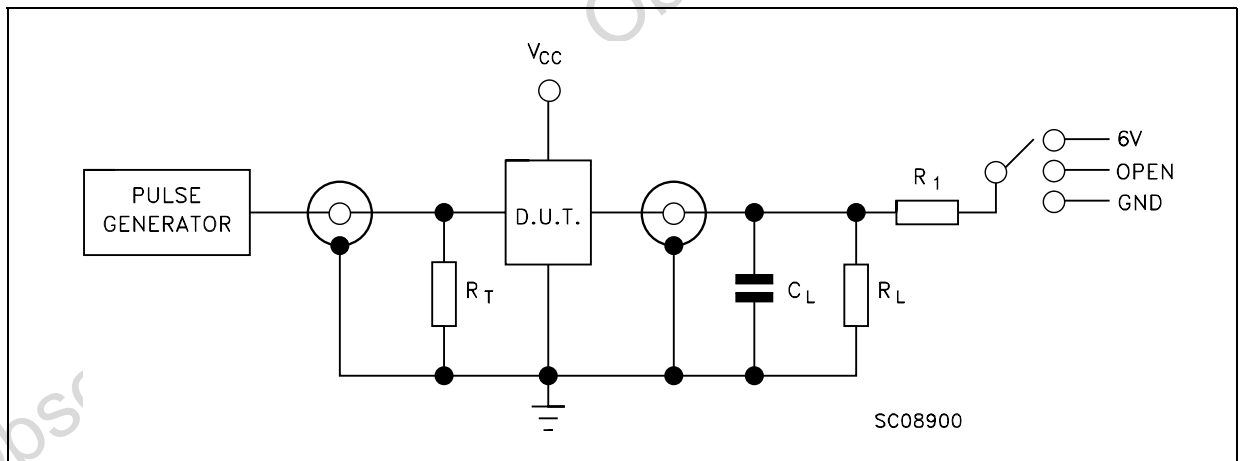
Table 11: AC Electrical Characteristics for GTL+

($V_{CC}=3.3 \pm 0.3V$, $V_{TT}=1.5V$, $V_{REF}=1.0V$, $V_{ERC}=V_{CC}$ or GND)

Symbol	Parameter	Test Condition	Value			Unit
			-40 to 85 °C			
			Min.	Typ.	Max.	
f_{MAX}	Maximum Frequency B to A or A to B		160			MHz
t_{PLH}	Propagation Delay Time A to B	$V_{ERC}=V_{CC}$ $R_L=12.5\Omega$ $C_L=30pF$	1.5		5.1	ns
			t_{PHL}	1.5		
t_{PLH}	Propagation Delay Time CK to B	$V_{ERC}=V_{CC}$ $R_L=12.5\Omega$ $C_L=30pF$	1.5		5.4	ns
			t_{PHL}	1.5		
t_{PLH}	Propagation Delay Time LEAB to B	$V_{ERC}=V_{CC}$ $R_L=12.5\Omega$ $C_L=30pF$	1.5		5.7	ns
			t_{PHL}	1.5		
t_{EN}	Enable Delay Time OEAB or OE to B	$V_{ERC}=V_{CC}$ $R_L=12.5\Omega$ $C_L=30pF$	1.5		5.5	ns
t_{DIS}	Disable Delay Time OEAB or OE to B		1.5		5.8	
t_{PLH}	Propagation Delay Time A to B	$V_{ERC}=GND$ $R_L=12.5\Omega$ $C_L=30pF$	1.0		4.3	ns
			t_{PHL}	1.0		
t_{PLH}	Propagation Delay Time CK to B	$V_{ERC}=GND$ $R_L=12.5\Omega$ $C_L=30pF$	1.0		4.0	ns
			t_{PHL}	1.0		
t_{PLH}	Propagation Delay Time LEAB to B	$V_{ERC}=GND$ $R_L=12.5\Omega$ $C_L=30pF$	1.0		4.0	ns
			t_{PHL}	1.0		
t_{EN}	Enable Delay Time OEAB or OE to B	$V_{ERC}=GND$ $R_L=12.5\Omega$ $C_L=30pF$	1.0		5.1	ns
t_{DIS}	Disable Delay Time OEAB or OE to B		1.0		4.9	

Symbol	Parameter	Test Condition	Value			Unit	
			-40 to 85 °C				
			Min.	Typ.	Max.		
t_{PLH}	Propagation Delay Time B to A	$R_L=500\Omega$ $C_L=50pF$	1.5		4.8	ns	
t_{PHL}			1.5		4.7		
t_{PLH}	Propagation Delay Time CK to A	$R_L=500\Omega$ $C_L=50pF$	1.5		4.4	ns	
t_{PHL}			1.5		4.1		
t_{PLH}	Propagation Delay Time LEBA to A	$R_L=500\Omega$ $C_L=50pF$	1.5		4	ns	
t_{PHL}			1.5		3.7		
t_{EN}	Enable Delay Time OEBA or OE to A	$R_L=500\Omega$ $R_1=500\Omega$ $C_L=50pF$	1		4.2	ns	
t_{DIS}	Disable Delay Time OEBA or OE to A		1		6.1		
Slew rate	Slew rate B output both transition (0.6 to 1.3V)	$V_{ERC}=V_{CC}$ $R_L=12.5\Omega$ $C_L=30pF$			1	ns/V	
		$V_{ERC}=GND$ $R_L=12.5\Omega$ $C_L=30pF$			1		
t_W	Pulse duration	LE High	3			ns	
		CK High or Low	3				
t_{SU}	Set-up Time	Data before clock	2.7			ns	
		Data before LE	Ck High	2.8			
			Ck Low	2.6			
t_H	Hold Time	Data after clock	0.4			ns	
		Data after LE Ck High or LOW	0.9				
t_{sk}	Skew between drivers (in the same package)	Switching in the same direction			1	ns	
		Switching in any direction			1		

Figure 4: Test Circuit For "A" Outputs



Test	Switch
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	6V
t_{PZH} , t_{PHZ}	GND

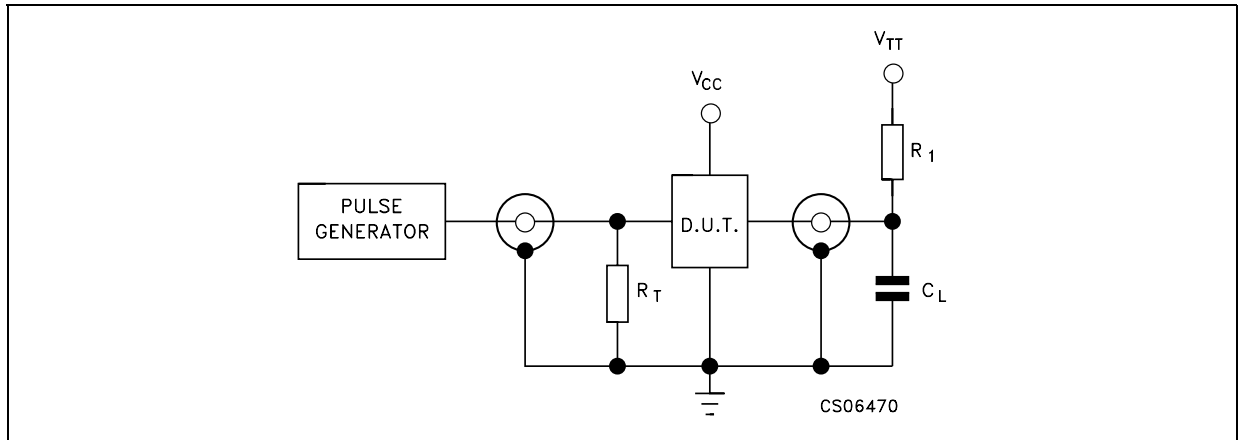
$C_L = 50pF$ or equivalent (includes jig and probe capacitance)

$R_L = R_1 = 500\Omega$ or equivalent

$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

$t_r = t_f \leq 2.5ns$

Table 12: Test Circuit For "B" Outputs



$C_L = 30\text{pF}$ or equivalent (includes jig and probe capacitance)

$R_L = R_1 = 12.5\Omega$ or equivalent

$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

$t_r = t_f \leq 2.5\text{ns}$

Figure 5: Waveform - Pulse Duration (A Port, Control Pin)

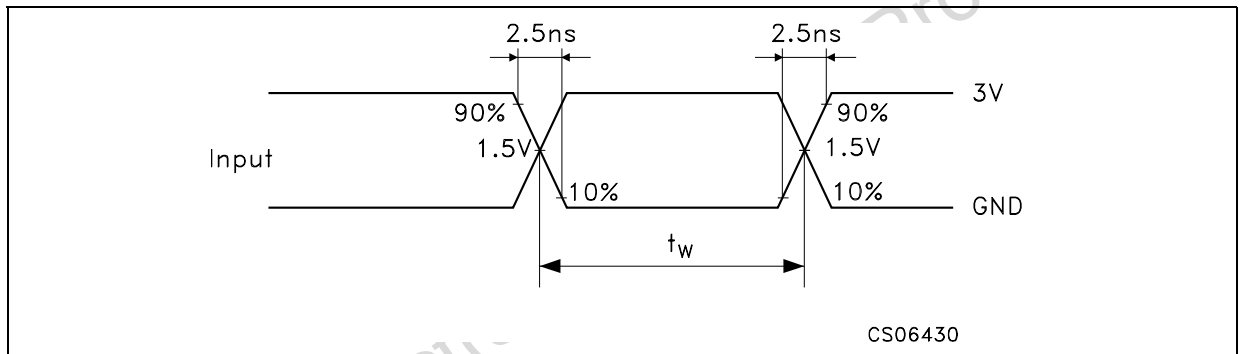


Figure 6: Waveform - Clock To B Port Propagation Delay Time

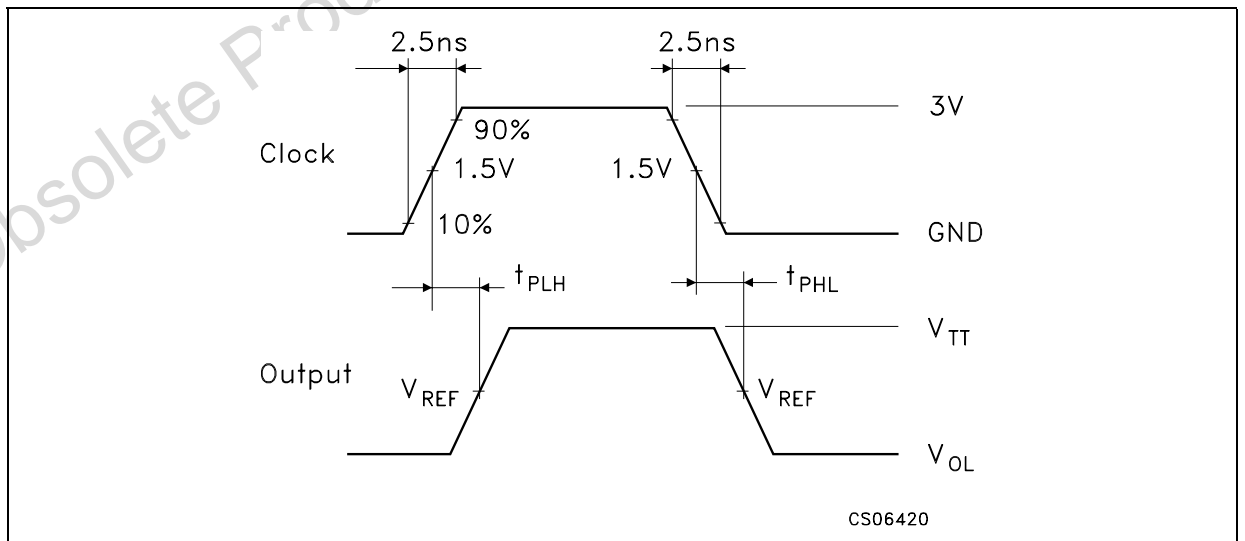


Figure 7: Waveform - Clock To A Port Propagation Delay Time

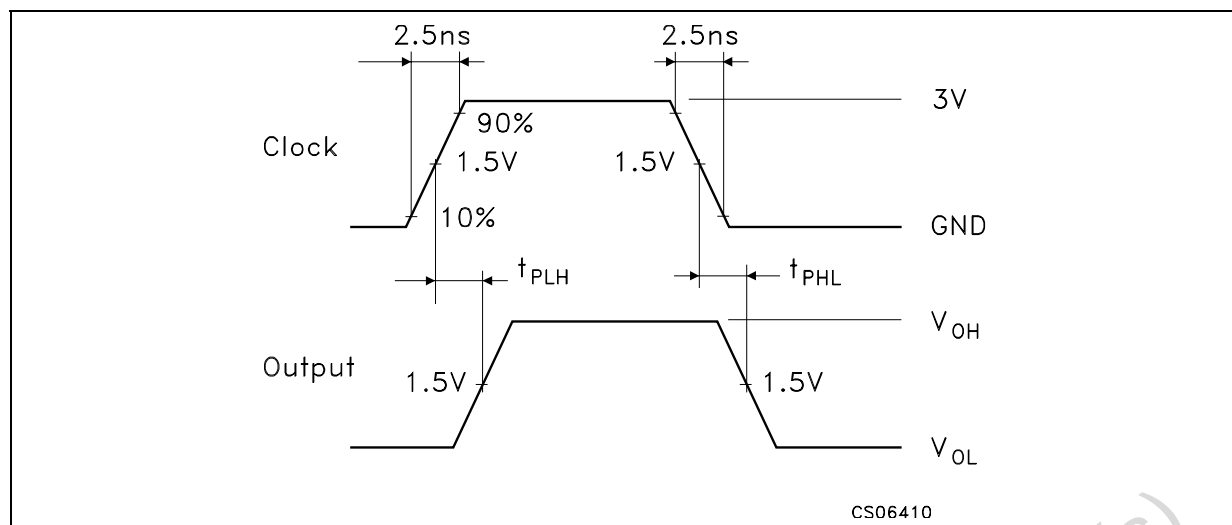


Figure 8: Waveform - Setup And Hold Time

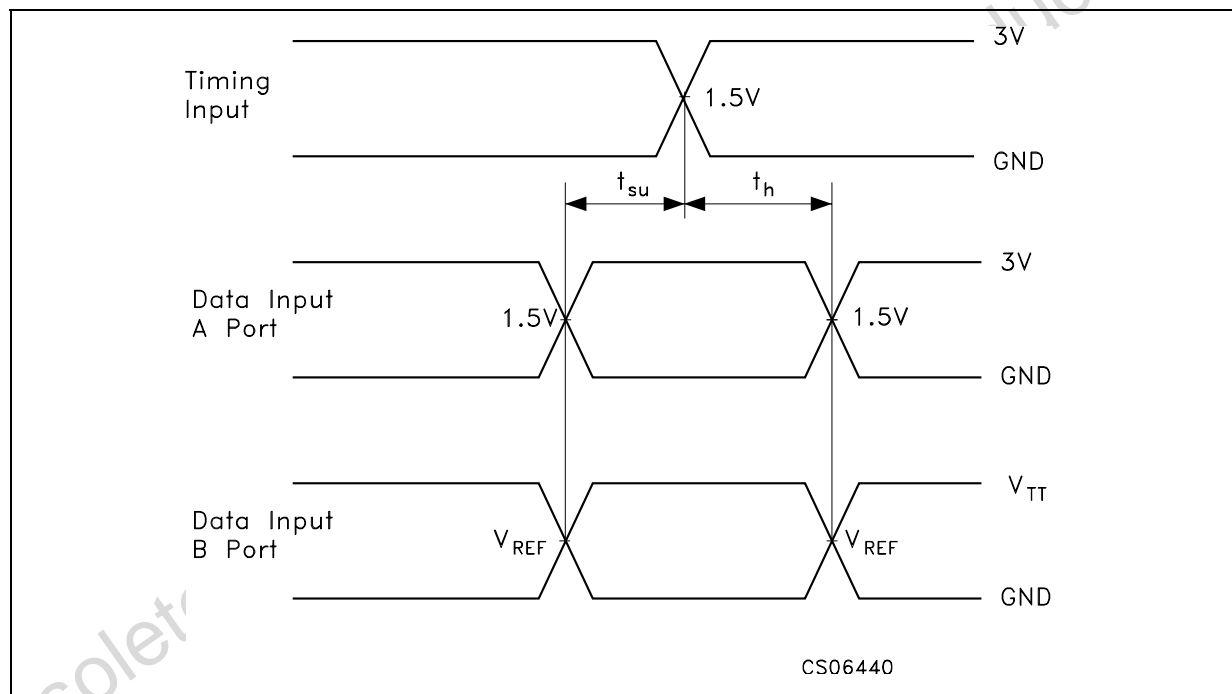
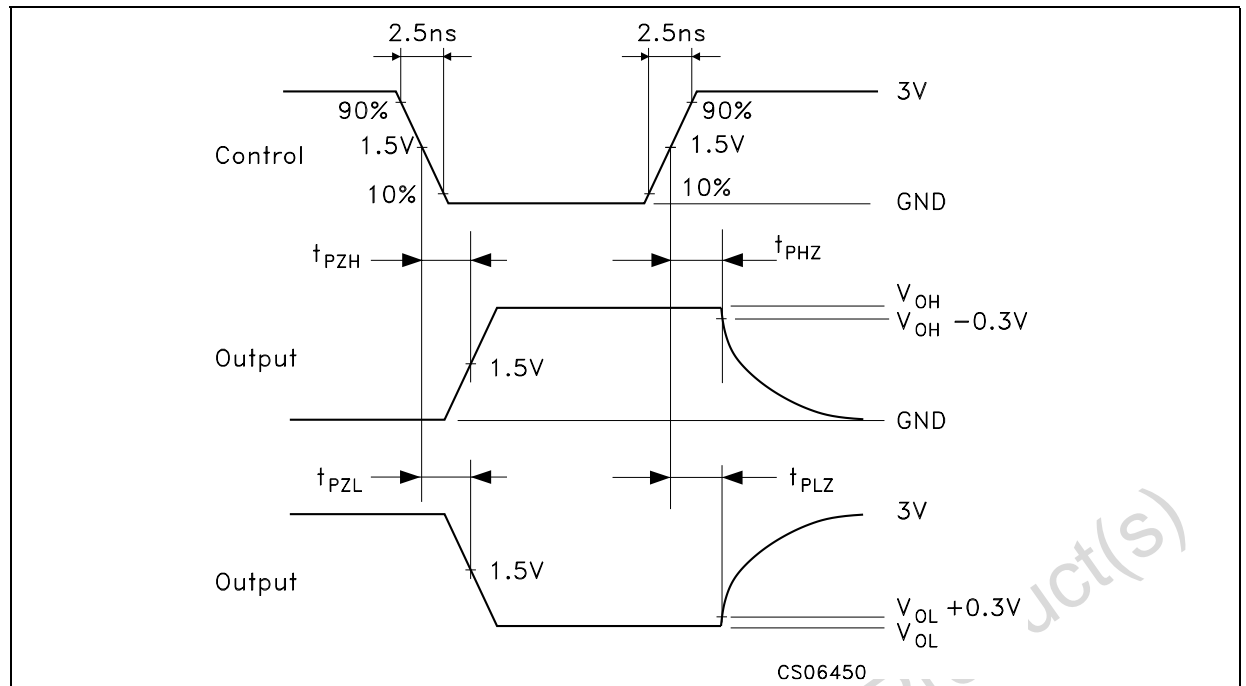
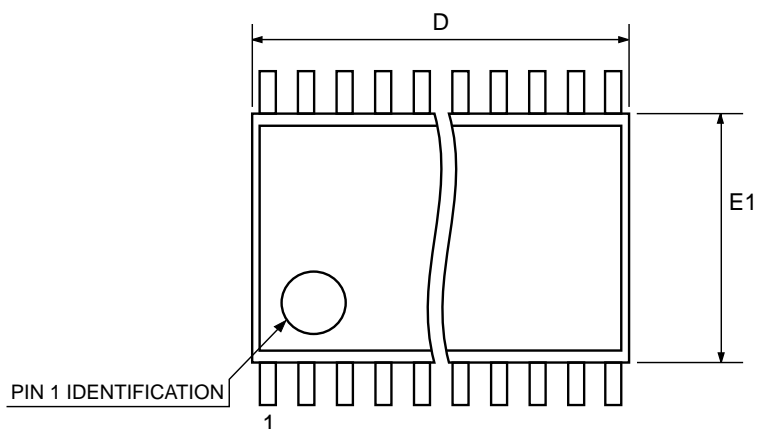
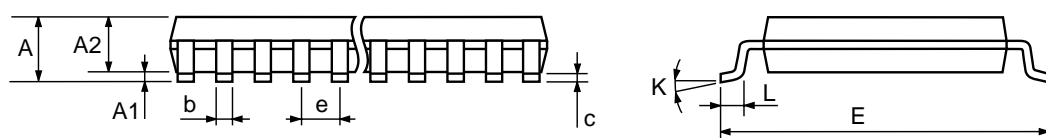


Figure 9: Waveform - Enable And Disable Time (A Port)



TSSOP64 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.1			0.043
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.17		0.27	0.0067		0.011
c	0.09		0.20	0.0035		0.0079
D	16.9		17.1	0.665		0.673
E		8.1			0.318	
E1	6.0		6.2	0.236		0.244
e		0.5 BSC			0.0197 BSC	
K	0°		8°	0°		8°
L	0.50		0.75	0.020		0.030



7187824A

Tape & Reel TSSOP64 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	8.7		8.9	0.342		0.350
Bo	17.2		17.4	0.677		0.685
Ko	1.4		1.6	0.055		0.063
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476

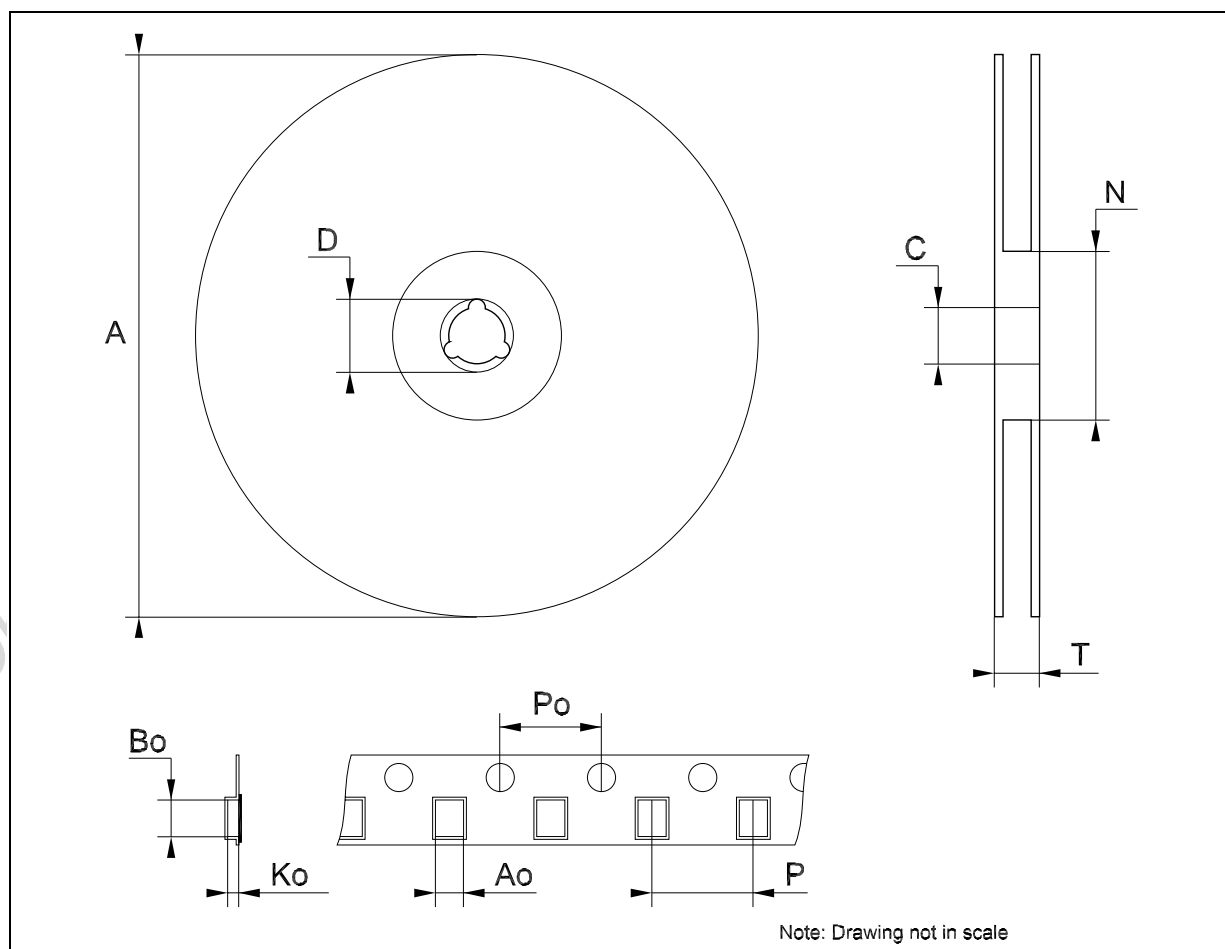


Table 13: Revision History

Date	Revision	Description of Changes
18-Oct-2004	1	First Release.

Obsolete Product(s) - Obsolete Product(s)

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