

PIN-PROGRAMMABLE PRECISION CLOCK MULTIPLIER/JITTER ATTENUATOR

Description

The Si5323 is a jitter-attenuating precision clock multiplier for high-speed communication systems, including SONET OC-48/OC-192, Ethernet, and Fibre Channel. The Si5323 accepts dual clock inputs ranging from 8 kHz to 707 MHz and generates two equal frequency-multiplied clock outputs ranging from 8 kHz to 1050 MHz. The input clock frequency and clock multiplication ratio are selectable from a table of popular SONET, Ethernet, and Fibre Channel rates. The Si5323 is based on Silicon Laboratories' 3rd-generation DSPLL[®] technology, which provides any-rate frequency synthesis and jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The DSPLL loop bandwidth is digitally programmable, providing jitter performance optimization at the application level. Operating from a single 1.8, 2.5, or 3.3 V supply, the Si5323 is ideal for providing clock multiplication and jitter attenuation in high performance timing applications.

Applications

- SONET/SDH OC-48/OC-192 line cards
- GbE/10GbE, 1/2/4/8/10GFC line cards
- ITU G.709 line cards
- Optical modules
- Test and measurement

Features

- Selectable output frequencies ranging from 8 kHz to 1050 MHz
- Ultra-low jitter clock outputs with jitter generation as low as 0.3 ps rms (50 kHz–80 MHz)
- Integrated loop filter with selectable loop bandwidth (60 Hz to 8.4 kHz)
- Meets OC-192 GR-253-CORE jitter specifications
- Dual clock inputs w/manual or automatically controlled hitless switching
- Dual clock outputs with selectable signal format (LVPECL, LVDS, CML, CMOS)
- Support for ITU G.709 FEC ratios (255/238, 255/237, 255/236)
- LOL, LOS alarm outputs
- Pin-controlled output phase adjust
- Pin-programmable settings
- On-chip voltage regulator for 1.8, 2.5, or 3.3 V $\pm 10\%$ operation
- Small size: 6 x 6 mm 36-lead QFN
- Pb-free, ROHS compliant

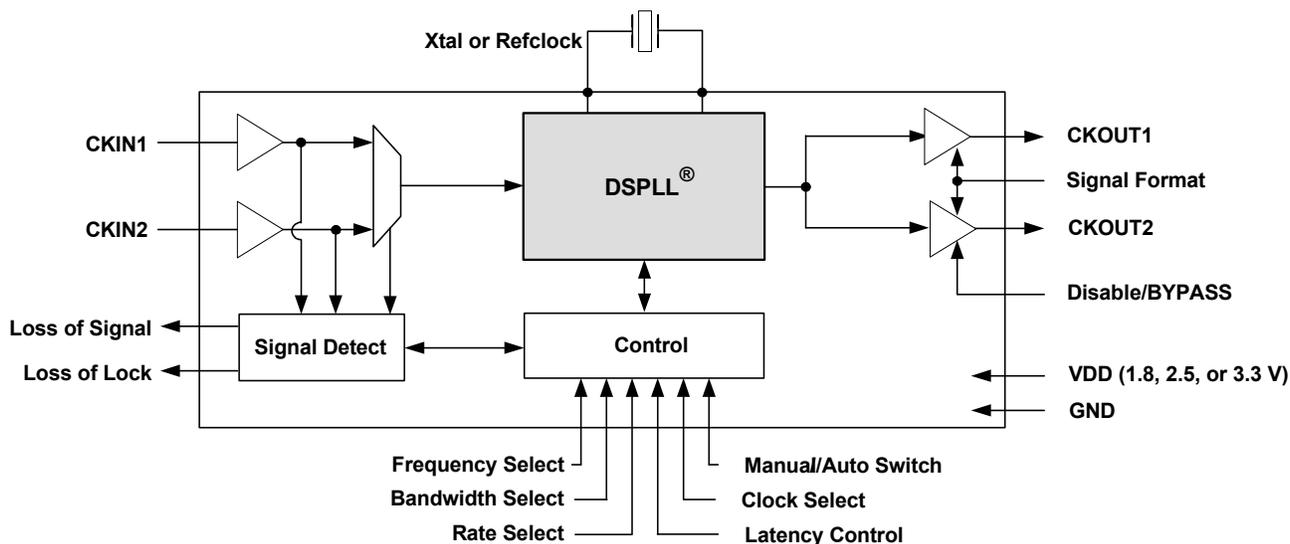


Table 1. Performance Specifications
 $(V_{DD} = 1.8, 2.5, \text{ or } 3.3 \text{ V} \pm 10\%, T_A = -40 \text{ to } 85 \text{ }^\circ\text{C})$

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Temperature Range	T_A		-40	25	85	$^\circ\text{C}$
Supply Voltage	V_{DD}		2.97	3.3	3.63	V
			2.25	2.5	2.75	V
			1.62	1.8	1.98	V
Supply Current	I_{DD}	$f_{OUT} = 622.08 \text{ MHz}$ Both CKOUTs enabled LVPECL format output		251	279	mA
		CKOUT2 disabled	—	217	243	mA
		$f_{OUT} = 19.44 \text{ MHz}$ Both CKOUTs enabled CMOS format output	—	204	234	mA
		CKOUT2 disabled	—	194	220	mA
		Tristate/Sleep Mode		TBD	TBD	mA
Input Clock Frequency (CKIN1, CKIN2)	CK_F	Input frequency and clock multiplication ratio pin-selectable from table of values using FRQSEL and FRQTBL settings. Consult Silicon Laboratories configuration software DSPLLsim or Any-Rate Precision Clock Family Reference Manual at www.silabs.com/timing for table selections.	0.008	—	707.35	MHz
Output Clock Frequency (CKOUT1, CKOUT2)	CK_{OF}		0.008	—	1049.76	MHz
Input Clocks (CKIN1, CKIN2)						
Differential Voltage Swing	CK_{NDPP}		0.25	—	1.9	V _{PP}
Common Mode Voltage	CK_{NVCM}	1.8V $\pm 10\%$	0.9	—	1.4	V
		2.5V $\pm 10\%$	1.0	—	1.7	V
		3.3V $\pm 10\%$	1.1	—	1.95	V
Rise/Fall Time	CK_{NTRF}	20–80%	—	—	11	ns
Duty Cycle	CK_{NDC}	Whichever is less	40	—	60	%
			50	—	—	ns
Output Clocks (CKOUT1, CKOUT2)						
Common Mode	V_{OCM}	LVPECL 100 Ω load line-to-line	$V_{DD} - 1.42$	—	$V_{DD} - 1.25$	V
Differential Output Swing	V_{OD}		1.1	—	1.9	V
Single Ended Output Swing	V_{SE}		0.5	—	0.93	V
Note: For a more comprehensive listing of device specifications, please consult the Silicon Laboratories Any-Rate Precision Clock Family Reference Manual. This document can be downloaded from www.silabs.com/timing .						

Table 1. Performance Specifications (Continued) $(V_{DD} = 1.8, 2.5, \text{ or } 3.3 \text{ V } \pm 10\%, T_A = -40 \text{ to } 85 \text{ }^\circ\text{C})$

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rise/Fall Time	CKO_{TRF}	20–80%	—	230	350	ps
Duty Cycle	CKO_{DC}		45	—	55	%
PLL Performance						
Jitter Generation	J_{GEN}	$f_{OUT} = 622.08 \text{ MHz}$, LVPECL output format 50 kHz–80 MHz	—	0.3	TBD	ps rms
		12 kHz–20 MHz	—	0.3	TBD	ps rms
Jitter Transfer	J_{PK}		—	0.05	0.1	dB
External Reference Jitter Transfer	J_{PKEXTN}		—	TBD	TBD	dB
Phase Noise	CKO_{PN}	$f_{OUT} = 622.08 \text{ MHz}$ 100 Hz offset	—	TBD	TBD	dBc/Hz
		1 kHz offset	—	TBD	TBD	dBc/Hz
		10 kHz offset	—	TBD	TBD	dBc/Hz
		100 kHz offset	—	TBD	TBD	dBc/Hz
		1 MHz offset	—	TBD	TBD	dBc/Hz
Subharmonic Noise	SP_{SUBH}	Phase Noise @ 100 kHz Off-set	—	TBD	TBD	dBc
Spurious Noise	SP_{SPUR}	Max spur @ $n \times F3$ ($n \geq 1, n \times F3 < 100 \text{ MHz}$)	—	TBD	TBD	dBc
Package						
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	—	38	—	$^\circ\text{C/W}$
Note: For a more comprehensive listing of device specifications, please consult the Silicon Laboratories Any-Rate Precision Clock Family Reference Manual. This document can be downloaded from www.silabs.com/timing .						

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	–0.5 to 3.6	V
LVC MOS Input Voltage	V_{DIG}	–0.3 to ($V_{DD} + 0.3$)	V
Operating Junction Temperature	T_{JCT}	–55 to 150	C
Storage Temperature Range	T_{STG}	–55 to 150	C
ESD HBM Tolerance (100 pF, 1.5 k Ω)		2	kV
ESD MM Tolerance		200	V
Latch-Up Tolerance		JEESD78 Compliant	
Note: Permanent device damage may occur if the Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.			

155.52 MHz in, 622.08 MHz out

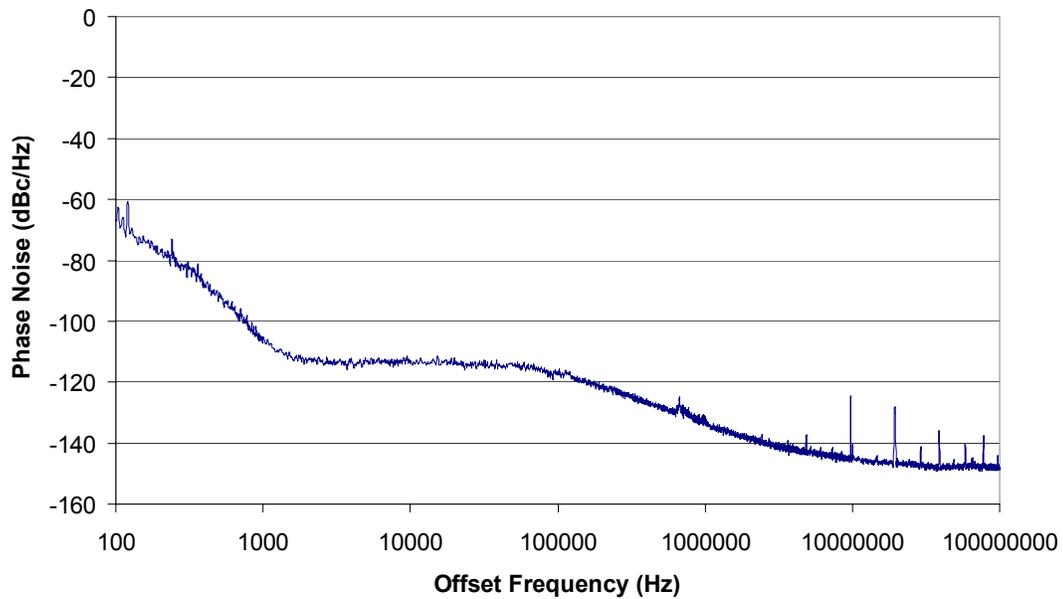


Figure 1. Typical Phase Noise Plot

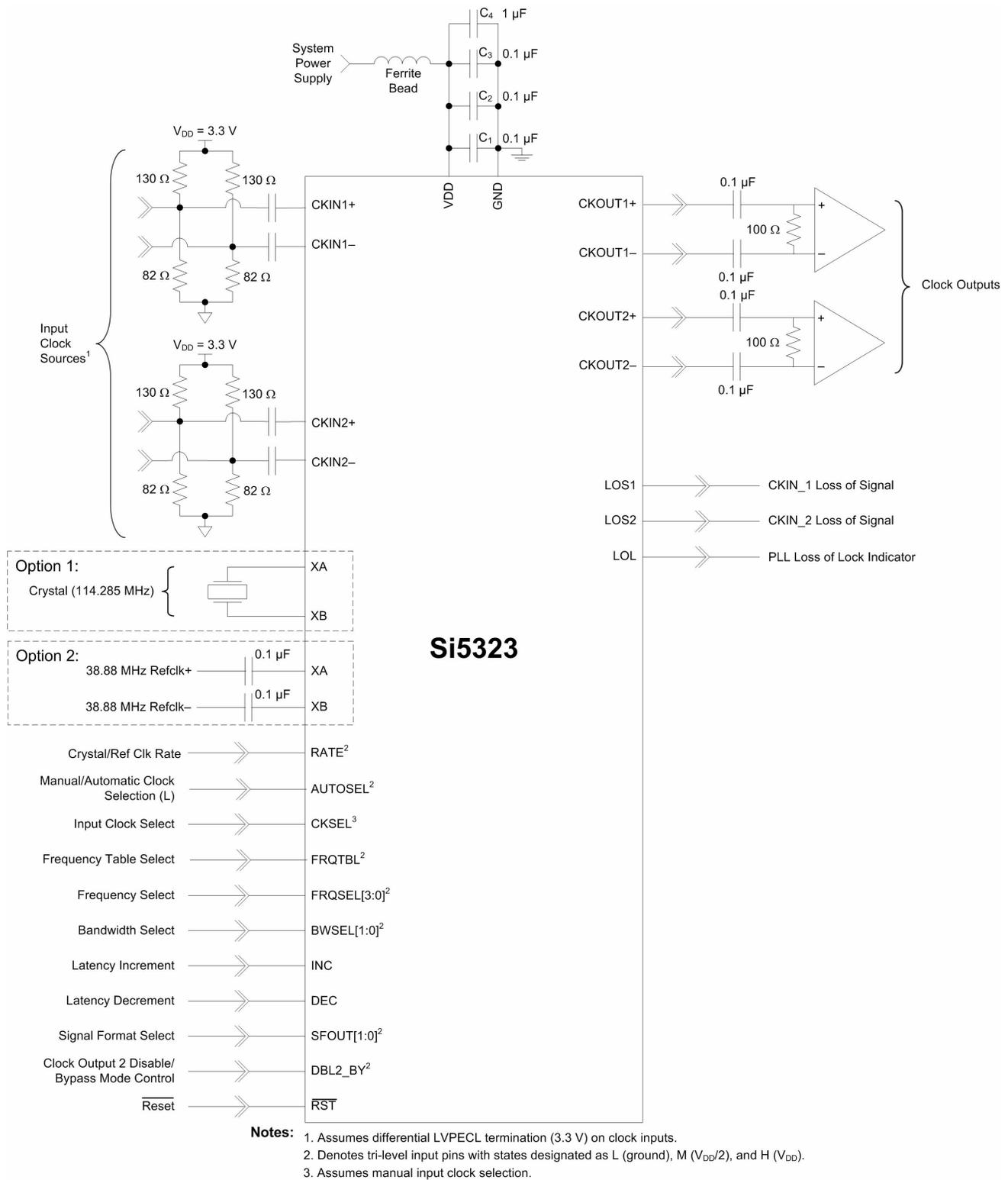


Figure 2. Si5323 Typical Application Circuit

1. Functional Description

The Si5323 is a jitter-attenuating precision clock multiplier for high-speed communication systems, including SONET OC-48/OC-192, Ethernet, and Fibre Channel. The Si5323 accepts dual clock inputs ranging from 8 kHz to 707 MHz and generates two frequency-multiplied clock outputs ranging from 8 kHz to 1050 MHz. The two input clocks are at the same frequency and the two output clocks are at the same frequency. The input clock frequency and clock multiplication ratio are selectable from a table of popular SONET, Ethernet, and Fibre Channel rates. In addition to providing clock multiplication in SONET and datacom applications, the Si5323 supports SONET-to-datacom frequency translations. Silicon Laboratories offers a PC-based software utility, *DSPLLsim*, that can be used to look up valid Si5323 frequency translations. This utility can be downloaded from www.silabs.com/timing. This information is also available in the Any-Rate Precision Clock Family Reference Manual, also available from www.silabs.com/timing.

The Si5323 is based on Silicon Laboratories' 3rd-generation DSPLL[®] technology, which provides any-rate frequency synthesis and jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The Si5323 PLL loop bandwidth is selectable via the BWSEL[1:0] pins and supports a range from 60 Hz to 8.4 kHz. The *DSPLLsim* software utility can be used to calculate valid loop bandwidth settings for a given input clock frequency/clock multiplication ratio.

The Si5323 supports hitless switching between the two input clocks in compliance with GR-253-CORE and GR-1244-CORE that greatly minimizes the propagation of phase transients to the clock outputs during an input clock transition (<200 ps typ). Manual and automatic revertive and non-revertive input clock switching options are available via the AUTOSEL input pin. The Si5323 monitors both input clocks for loss-of-signal and provides a LOS alarm when it detects missing pulses on either input clock. The device monitors the lock status of the PLL. The lock detect algorithm works by continuously monitoring the phase of the input clock in relation to the phase of the feedback clock.

The Si5323 provides a digital hold capability that allows the device to continue generation of a stable output clock when the selected input reference is lost. During digital hold, the DSPLL generates an output frequency based on a historical average that existed a fixed amount of time before the error event occurred, eliminating the effects of phase and frequency transients that may occur immediately preceding digital hold.

The Si5323 has two differential clock outputs. The electrical format of the clock outputs is programmable to support LVPECL, LVDS, CML, or CMOS loads. If not required, the second clock output can be powered down to minimize power consumption. The phase difference between the selected input clock and the output clocks is adjustable in 200 ps increments for system skew control. For system-level debugging, a bypass mode is available which drives the output clock directly from the input clock, bypassing the internal DSPLL. The device is powered by a single 1.8, 2.5, or 3.3 V supply.

1.1. External Reference

An external, 38.88 MHz clock or a low-cost 114.285 MHz 3rd overtone crystal is used as part of a fixed-frequency oscillator within the DSPLL. This external reference is required for the device to perform jitter attenuation. Silicon Laboratories recommends using a high-quality crystal from TXC (www.txc.com.tw), part number 7MA1400014. An external 38.88 MHz clock from a high quality OCXO or TCXO can also be used as a reference for the device.

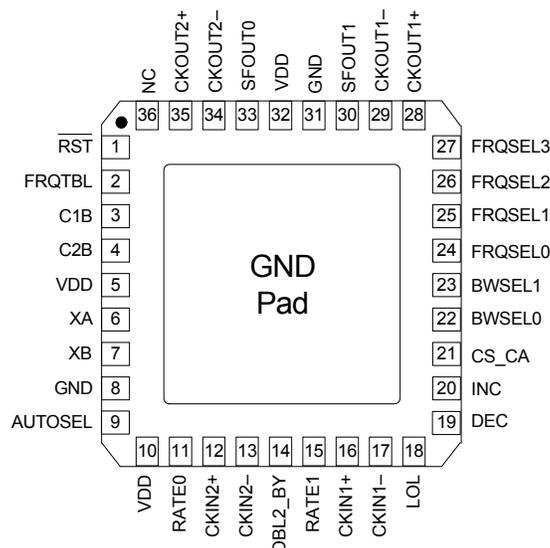
In digital hold, the DSPLL remains locked to this external reference. Any changes in the frequency of this reference when the DSPLL is in digital hold will be tracked by the output of the device. Note that crystals can have temperature sensitivities.

1.2. Further Documentation

Consult the Silicon Laboratories Any-Rate Precision Clock Family Reference Manual (FRM) for more detailed information about the Si5323. The FRM can be downloaded from www.silabs.com/timing.

Silicon Laboratories has developed a PC-based software utility called *DSPLLsim* to simplify device configuration, including frequency planning and loop bandwidth selection. This utility can be downloaded from www.silabs.com/timing.

2. Pin Descriptions: Si5323



Pin assignments are preliminary and subject to change.

Table 3. Si5323 Pin Descriptions

Pin #	Pin Name	I/O	Signal Level	Description
1	$\overline{\text{RST}}$	I	LVC MOS	External Reset. Active low input that performs external hardware reset of device. Resets all internal logic to a known state. Clock outputs are tristated during reset. After rising edge of $\overline{\text{RST}}$ signal, the Si5323 will perform an internal self-calibration. This pin has a weak pull-up.
2	FRQTBL	I	3-Level	Frequency Table Select. Selects SONET/SDH, datacom, or SONET/SDH to datacom frequency table. L = SONET/SDH M = Datacom H = SONET/SDH to Datacom This pin has a weak pull-down.
3	C1B	O	LVC MOS	CKIN1 Loss of Signal. Active high loss-of-signal indicator for CKIN1. Once triggered, the alarm will remain active until CKIN1 is validated. 0 = CKIN1 present 1 = LOS on CKIN1
4	C2B	O	LVC MOS	CKIN2 Loss of Signal. Active high loss-of-signal indicator for CKIN2. Once triggered, the alarm will remain active until CKIN2 is validated. 0 = CKIN2 present 1 = LOS on CKIN2

Table 3. Si5323 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description								
5, 10, 32	V _{DD}	V _{DD}	Supply	<p>Supply.</p> <p>The device operates from a 1.8, 2.5, or 3.3 V supply. Bypass capacitors should be associated with the following V_{DD} pins:</p> <table> <tr> <td>5</td> <td>0.1 μF</td> </tr> <tr> <td>10</td> <td>0.1 μF</td> </tr> <tr> <td>32</td> <td>0.1 μF</td> </tr> </table> <p>A 1.0 μF should be placed as close to device as is practical.</p>	5	0.1 μF	10	0.1 μF	32	0.1 μF		
5	0.1 μF											
10	0.1 μF											
32	0.1 μF											
7 6	XB XA	I	Analog	<p>External Crystal or Reference Clock.</p> <p>External crystal should be connected to these pins to use internal oscillator based reference. If external reference is used, apply reference clock to XA input and leave XB pin floating. External reference must be from a high-quality clock source (TCXO, OCXO). Frequency of crystal or external clock is set by the RATE pin.</p>								
8, 31	GND	GND	Supply	<p>Ground.</p> <p>Must be connected to system ground. Minimize the ground path impedance for optimal performance of this device.</p>								
9	AUTOSEL	I	3-Level	<p>Manual/Automatic Clock Selection.</p> <p>Three level input that selects the method of input clock selection to be used.</p> <p>L = Manual M = Automatic non-revertive H = Automatic revertive</p>								
11 15	RATE0 RATE1	I	3-Level	<p>External Crystal or Reference Clock Rate.</p> <p>Three level input that selects the type and rate of external crystal or reference clock to be applied to the XA/XB port.</p> <p><u>RATE[1:0]</u></p> <table> <tr> <td>LM</td> <td>= 38.88 MHz external clock</td> </tr> <tr> <td>MM</td> <td>= 114.285 MHz 3rd OT Crystal</td> </tr> <tr> <td>HH</td> <td>= Converts part to Si5322</td> </tr> <tr> <td>All Others</td> <td>= Reserved</td> </tr> </table>	LM	= 38.88 MHz external clock	MM	= 114.285 MHz 3rd OT Crystal	HH	= Converts part to Si5322	All Others	= Reserved
LM	= 38.88 MHz external clock											
MM	= 114.285 MHz 3rd OT Crystal											
HH	= Converts part to Si5322											
All Others	= Reserved											
12 13	CKIN2+ CKIN2-	I		<p>Clock Input 2.</p> <p>Differential input clock. This input can also be driven with a single-ended signal. Input frequency selected from a table of values. The same frequency must be applied to CKIN1 and CKIN2.</p>								
14	DBL2_BY	I	3-Level	<p>Output 2 Disable/Bypass Mode Control.</p> <p>Controls enable of CKOUT2 divider/output buffer path and PLL bypass mode.</p> <p>L = CKOUT2 enabled M = CKOUT2 disabled H = Bypass mode with CKOUT2 enabled</p>								

Table 3. Si5323 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
16 17	CKIN1+ CKIN1–	I	Multi	Clock Input 1. Differential input clock. This input can also be driven with a single-ended signal. Input frequency selected from a table of values. The same frequency must be applied to CKIN1 and CKIN2.
18	LOL	O	LVC MOS	PLL Loss of Lock Indicator. This pin functions as the active high PLL loss of lock indicator. 0 = PLL locked 1 = PLL unlocked
19	DEC	I	LVC MOS	Latency Decrement. A pulse on this pin decreases the input to output device latency by $1/f_{OSC}$ (approximately 200 ps). There is no limit on the range of latency adjustment by this method. If both INC and DEC are tied high, phase buildout is disabled and the device maintains a fixed-phase relationship between the selected input clock and the output clock during an input clock transition. Detailed operations and timing characteristics for this pin may be found in the Any-Rate Precision Clock Family Reference Manual. This pin has a weak pull-down.
20	INC	I	LVC MOS	Latency Increment. A pulse on this pin increases the input to output device latency by $1/f_{OSC}$ (approximately 200 ps). There is no limit on the range of latency adjustment by this method. If both INC and DEC are tied high, phase buildout is disabled and the device maintains a fixed-phase relationship between the selected input clock and the output clock during an input clock transition. Detailed operations and timing characteristics for this pin may be found in the Any-Rate Precision Clock Family Reference Manual. This pin has a weak pull-down.
21	CS_CA	I/O	LVC MOS	Input Clock Select/Active Clock Indicator. If manual clock selection mode is chosen (AUTOSEL = L), this pin functions as the manual input clock selector. This input is internally deglitched to prevent inadvertent clock switching during changes in the CS input state. 0 = Select CKIN1 1 = Select CKIN2 If automatic clock selection mode is chosen (AUTOSEL = M or H), this pin indicates which of the two input clocks is currently the active clock. If alarms exist on both CKIN1 and CKIN2, indicating that the digital hold state has been entered, CA will indicate the last active clock that was used before entering the hold state. 0 = CKIN1 active input clock 1 = CKIN2 active input clock

Table 3. Si5323 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description																				
23 22	BWSEL1 BWSEL0	I	3-Level	Bandwidth Select. Three level inputs that select the DSPLL closed loop bandwidth. Detailed operations and timing characteristics for these pins may be found in the Any-Rate Precision Clock Family Reference Manual.																				
27 26 25 24	FRQSEL3 FRQSEL2 FRQSEL1 FRQSEL0	I	3-Level	Multiplier Select. Three level inputs that select the input clock and clock multiplication ratio, depending on the FRQTBL setting. Consult the Any-Rate Precision Clock Family Reference Manual or DSPLLsim configuration software for settings, both available for download at www.silabs.com/timing .																				
29 28	CKOUT1– CKOUT1+	O	Multi	Clock Output 1. Differential output clock with a frequency selected from a table of values. Output signal format is selected by SFOUT pins. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.																				
33 30	SFOUT0 SFOUT1	I	3-Level	Signal Format Select. Three level inputs that select the output signal format (common mode voltage and differential swing) for both CKOUT1 and CKOUT2. <table border="1" data-bbox="889 1031 1378 1482"> <thead> <tr> <th>SFOUT[1:0]</th> <th>Signal Format</th> </tr> </thead> <tbody> <tr> <td>HH</td> <td>Reserved</td> </tr> <tr> <td>HM</td> <td>Reserved</td> </tr> <tr> <td>HL</td> <td>CML</td> </tr> <tr> <td>MH</td> <td>LVPECL</td> </tr> <tr> <td>MM</td> <td>Reserved</td> </tr> <tr> <td>ML</td> <td>LVDS</td> </tr> <tr> <td>LH</td> <td>CMOS</td> </tr> <tr> <td>LM</td> <td>Tristate/Sleep</td> </tr> <tr> <td>LL</td> <td>Reserved</td> </tr> </tbody> </table>	SFOUT[1:0]	Signal Format	HH	Reserved	HM	Reserved	HL	CML	MH	LVPECL	MM	Reserved	ML	LVDS	LH	CMOS	LM	Tristate/Sleep	LL	Reserved
SFOUT[1:0]	Signal Format																							
HH	Reserved																							
HM	Reserved																							
HL	CML																							
MH	LVPECL																							
MM	Reserved																							
ML	LVDS																							
LH	CMOS																							
LM	Tristate/Sleep																							
LL	Reserved																							
34 35	CKOUT2– CKOUT2+	O	Multi	Clock Output 2. Differential output clock with a frequency selected from a table of values. Output signal format is selected by SFOUT pins. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.																				
36	NC	—	—	No Connect. These pins must be left unconnected for normal operation.																				
GND PAD	GND	GND	Supply	Ground Pad. The ground pad must provide a low thermal and electrical impedance to a ground plane.																				

3. Ordering Guide

Ordering Part Number	Package	Temperature Range
Si5323-B-GM	36-Lead 6 x 6 mm QFN	-40 to 85 °C

4. Package Outline: 36-Lead QFN

Figure 3 illustrates the package details for the Si5323. Table 4 lists the values for the dimensions shown in the illustration.

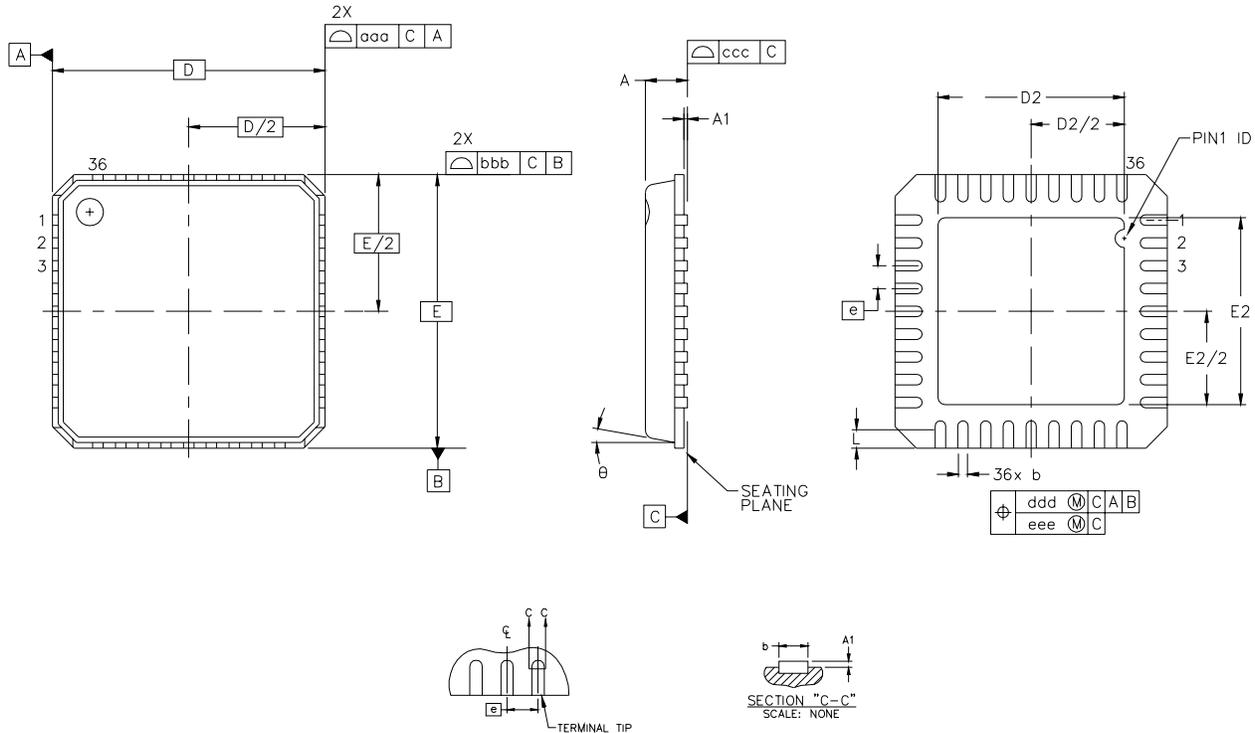


Figure 3. 36-Pin Quad Flat No-lead (QFN)

Table 4. Package Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.01	0.05
b	0.18	0.23	0.30
D	6.00 BSC		
D2	3.95	4.10	4.25
e	0.50 BSC		
E	6.00 BSC		
E2	3.95	4.10	4.25

Symbol	Millimeters		
	Min	Nom	Max
L	0.50	0.60	0.75
θ	—	—	12°
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.05
ddd	—	—	0.10
eee	—	—	0.05

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220, variation VJJD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

5. Recommended PCB Layout

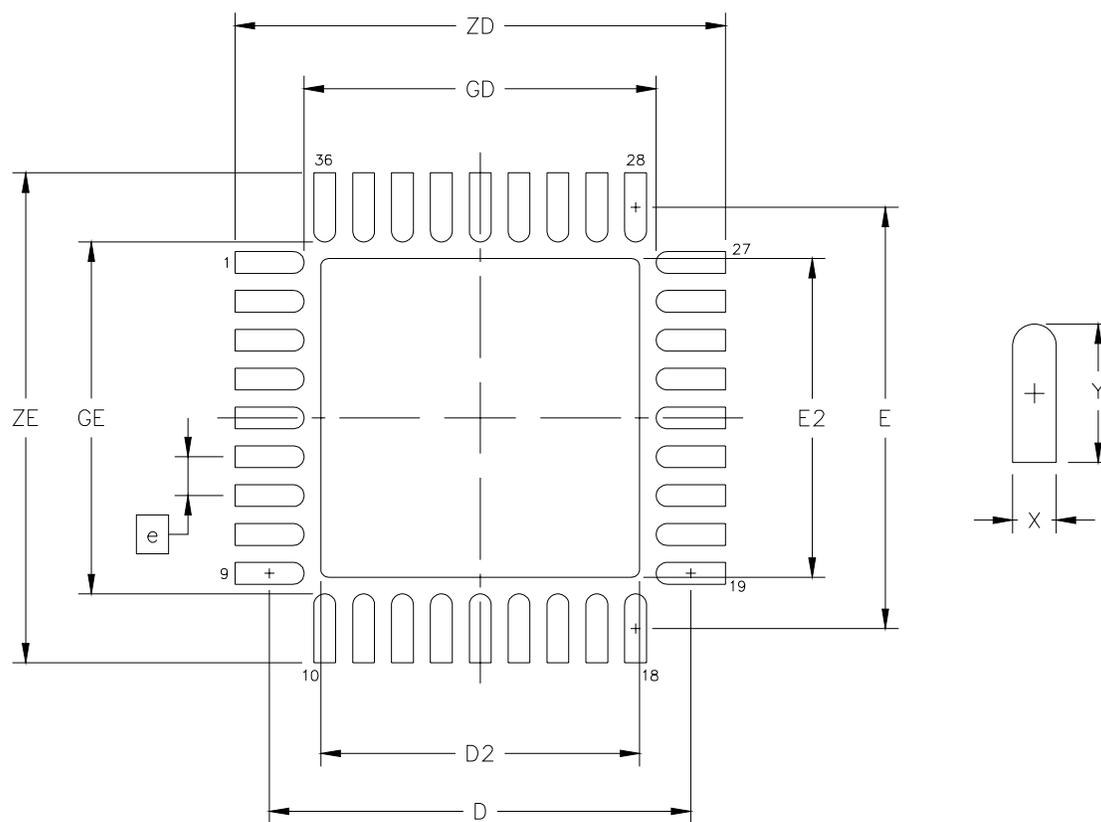


Figure 4. PCB Land Pattern Diagram

Table 5. PCB Land Pattern Dimensions

Dimension	MIN	MAX
e	0.50 BSC.	
E	5.42 REF.	
D	5.42 REF.	
E2	4.00	4.20
D2	4.00	4.20
GE	4.53	—
GD	4.53	—
X	—	0.28
Y	0.89 REF.	
ZE	—	6.31
ZD	—	6.31

Notes (General):

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Notes (Solder Mask Design):

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

Notes (Stencil Design):

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
4. A 4 x 4 array of 0.80 mm square openings on 1.05 mm pitch should be used for the center ground pad.

Notes (Card Assembly):

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

- Changed LVTTTL to LVCMOS in Table 2, “Absolute Maximum Ratings,” on page 3.
- Added Figure 1, “Typical Phase Noise Plot,” on page 4.
- Updated Figure 2, “Si5323 Typical Application Circuit,” on page 5 to show external reference interface.
- Added RATE0 and expanded the RATE[1:0] description in 2. ‘Pin Descriptions: Si5323’.
- Updated 3. “Ordering Guide” on page 11.
- Added 5. ‘Recommended PCB Layout’.

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