RAiO

RA8900

8-Bit Micro-Controller

Revision 1.4

October, 2003

RAiO Technology Inc.

Overview

The RA8900 is an 8-bit downloadable micro-controller. It supports multiple timer/counter sources, versatile interrupt-handling architecture and two built-in DAC's (Digital-to-Analog Converters). It provides a complete speech interface and 32K-bps ADPCM solution that make this chip an excellent choice as the embedded micro-controller for educational speech products.

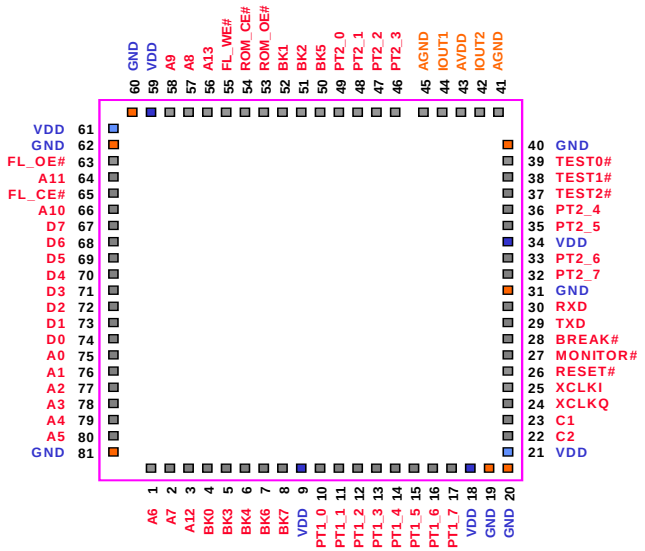
The built-in 4K-bytes ROM support the on-chip RAiO ICE Monitor program which controls the UART and enables the RS232 connection between the RA8900 and a PC host. The RA8900 support the ISP(In-System Programming) and ISD(In-System Debugging) functions. Users can download their programs as well as data from a PC host to the external Flash ROM.

RAiO also support a windows based ICE driver for customers to very easy programming & debugging their program. Using RS232 connection between a speech toy to a PC host running RAiO's download utility program, toy makers are able to implement the Internet Game/Speech download features easily and give the toys multiple attractive characteristics.

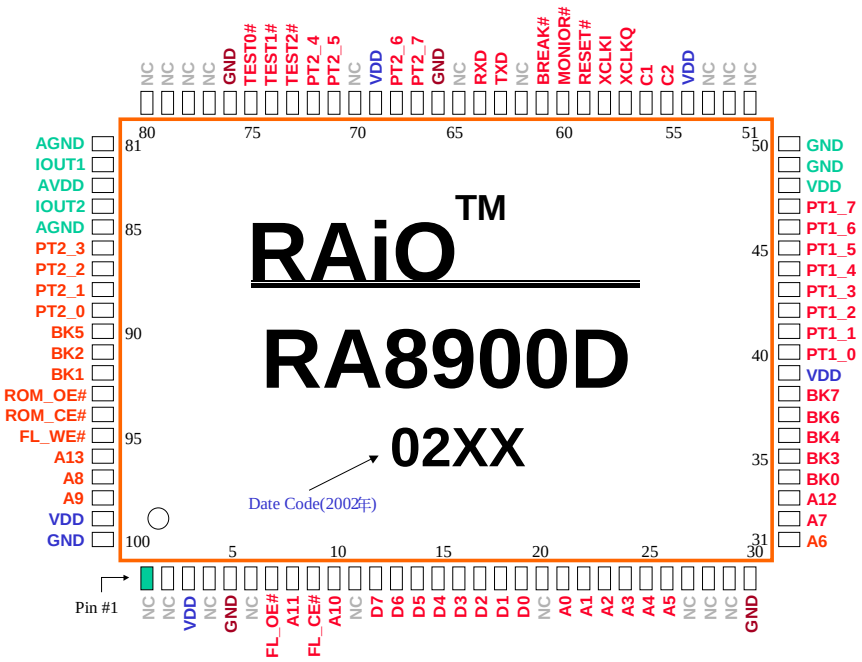
Feature

- 8-bit Micro Processor
- Internal 128-Byte SRAM
- Flexible External Flash Support
- Support LVD (Low Voltage Detector)
- Support External Memory & LCD Interface
- Support PWM Output with 50% or 100% duty select
- Two 8-Bits Programmable I/O Port
- Three 12-Bits Timer and Three Time-Base Options (2KHz, 500Hz, 62Hz)
- One 4-Bits Watch Dog Timer
- One User's UART with Baud Rate Generator, Up to 115200bps
- Two 8-bits Current Mode DAC
- UART Provide IrDA & ASK IR Mode
- Support UART and Timer Wake-Up Mode
- Flexible I/O Interrupt & Wake-Up Mode
- Support Wake-Up Reset Mode
- Support Idle/Sleep Power Saving Mode
- Built in PLL, Only need one 32768Hz X'tal Oscillator can produce system clock 7.3MHz
- On-Chip ICE and ISP (In-System Programming) Supporting Programs.
- Operating Voltage: 2.3V ~ 5.2V
- Package: Die Form or PQFP-100Pin

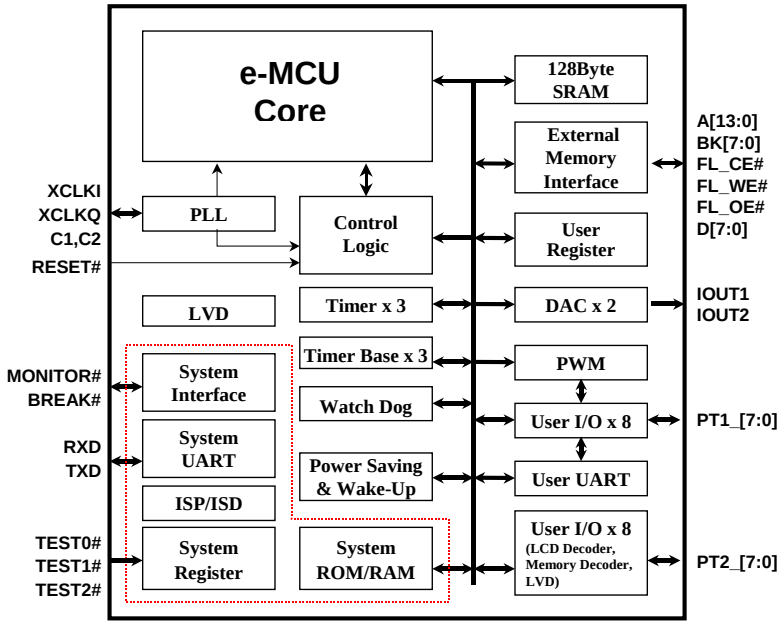
Die Form



Package (PQFP-100Pin)



Block Diagram



PAD X/Y Coordinate

Order	PIN Name	X	Y
1	A6	-989.98	-1220.85
2	A7	-879.98	-1220.85
3	A12	-769.98	-1220.85
4	BK0	-659.98	-1220.85
5	BK3	-549.98	-1220.85
6	BK4	-439.98	-1220.85
7	BK6	-329.98	-1220.85
8	BK7	-219.98	-1220.85
9	VDD	-109.98	-1220.85
10	PT1_0	0.02	-1220.85
11	PT1_1	110.02	-1220.85
12	PT1_2	220.02	-1220.85
13	PT1_3	330.02	-1220.85
14	PT1_4	440.02	-1220.85
15	PT1_5	550.02	-1220.85
16	PT1_6	660.02	-1220.85
17	PT1_7	770.02	-1220.85
18	VDD	880.02	-1220.85
19	GND	990.02	-1220.85
20	GND	1110.87	-1220.85
21	VDD	1110.87	-1100
22	C2	1110.87	-990
23	C1	1110.87	-880
24	XCLKQ	1110.87	-770
25	XCLK	1110.87	-660
26	RESET#	1110.87	-550
27	MONITOR#	1110.87	-440
28	BREAK#	1110.87	-330
29	TXD	1110.87	-220
30	RXD	1110.87	-110
31	GND	1110.87	0
32	PT2_7	1110.87	110
33	PT2_6	1110.87	220
34	VDD	1110.87	330
35	PT2_5	1110.87	440
36	PT2_4	1110.87	550
37	TEST2#	1110.87	660
38	TEST1#	1110.87	770
39	TEST0#	1110.87	880
40	GND	1110.87	990

Order	PIN Name	X	Y
41	AGND	1110.87	1220.85
42	IOUT2	1004.87	1220.85
43	AVDD	898.87	1220.85
44	IOUT1	792.87	1220.85
45	AGND	686.87	1220.85
46	PT2_3	550.02	1220.85
47	PT2_2	440.02	1220.85
48	PT2_1	330.02	1220.85
49	PT2_0	220.02	1220.85
50	ROM_OE#	110.02	1220.85
51	ROM_CE#	0.02	1220.85
52	FL_WE#	-109.98	1220.85
53	BK5	-219.98	1220.85
54	BK2	-329.98	1220.85
55	BK1	-439.98	1220.85
56	A13	-549.98	1220.85
57	A8	-659.98	1220.85
58	A9	-769.98	1220.85
59	VDD	-879.98	1220.85
60	GND	-989.98	1220.85
61	VDD	-1110.83	1100
62	GND	-1110.83	990
63	A11	-1110.83	880
64	FL_OE#	-1110.83	770
65	A10	-1110.83	660
66	FL_CE#	-1110.83	550
67	D7	-1110.83	440
68	D6	-1110.83	330
69	D5	-1110.83	220
70	D4	-1110.83	110
71	D3	-1110.83	0
72	D2	-1110.83	-110
73	D1	-1110.83	-220
74	D0	-1110.83	-330
75	A0	-1110.83	-440
76	A1	-1110.83	-550
77	A2	-1110.83	-660
78	A3	-1110.83	-770
79	A4	-1110.83	-880
80	A5	-1110.83	-990
81	GND	-1110.83	-1100

Pin Description

Signal	Pin#	I/O	Description
RESET#	59	IN	**External Hardware Reset, active low.** This pin is used to reset the system.
BREAK#	61	IN	**User Program Break, active low.** This signal is used to break the user's program from the ISD mode.
MONITOR#	60	IN	**Monitor Program Select, active low.** This signal is used to select the system boot from monitor program (ROM) or user program (Flash). This signal has to pull low when the user wants to download the data from PC or enter the ISP/ISD mode.
PT1_7 PWM1	47	I/O	**Bit-7 of Port 1** This is a programmable pin for general-purpose I/O Port 1. The driving current and pull-high or pull-low can be selected by user register. The PT1_7 is also as the output of PWM. In PWM mode, the pin is always output and 30mA driving current is selected.
PT1_6 PWM2	46	I/O	**Bit-6 of Port 1** This is a programmable pin for general-purpose I/O Port 1. The driving current and pull-high or pull-low can be selected by user register. The PT1_6 is also as the output of PWM. In PWM mode, the pin is always output and 30mA driving current is selected.
PT1_5 TX	45	I/O	**Bit-5 of Port 1** This is a programmable pin for general-purpose I/O Port 1. The driving current and pull-high or pull-low can be selected by user register. The PT1_5 is also as the transmission output of user's UART. In UART mode, the pin is always output except the power saving mode.
PT1_4 RX	44	I/O	**Bit-4 of Port 1** This is a programmable pin for general-purpose I/O Port 1. The driving current and pull-high or pull-low can be selected by user register. The PT1_4 is also as the receive input of user's UART. In UART mode, the pin is always input.
PT1_3	43	I/O	**Bit-3 of Port 1** This is a programmable pin for general-purpose I/O Port 1. The driving current and pull-high or pull-low can be selected by user register.
PT1_2	42	I/O	**Bit-2 of Port 1** This is a programmable pin for general-purpose I/O Port 1. The driving current and pull-high or pull-low can be selected by user register.
PT1_1	41	I/O	**Bit-1 of Port 1** This is a programmable pin for general-purpose I/O Port 1. The driving current and pull-high or pull-low can be selected by user register.
PT1_0	40	I/O	**Bit-0 of Port 1** This is a programmable pin for general-purpose I/O Port 1. The driving current and pull-high or pull-low can be selected by user register.

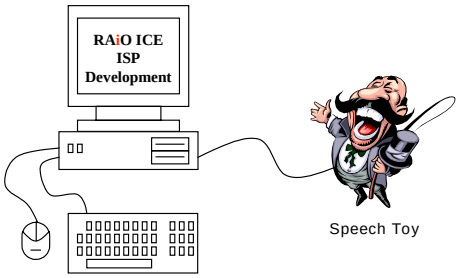
PT2_7 FL_CE2#	67	I/O	**Bit-7 of Port 2** This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register. The PT2_7 is also as the secondary external flash chip select. If the secondary flash is enabled, the pin is always output except the power saving mode.
PT2_6 MEM_CE#	68	I/O	**Bit-6 of Port 2** This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register. The PT2_6 is also as the external memory chip selecting. If the external memory enabled, the pin is always output except the power saving mode.
PT2_5 MEM_OE#	71	I/O	**Bit-5 of Port 2** This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register. The PT2_5 is also as the external memory output enable. If the external memory enabled, the pin is always output except the power saving mode.
PT2_4 MEM_WE#	72	I/O	**Bit-4 of Port 2** This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register. The PT2_4 is also as the external memory write enable. If the external memory enabled, the pin is always output except the power saving mode.
PT2_3 LCD_E	86	I/O	**Bit-3 of Port 2** This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register. The PT2_3 is also as the chip enable of external LCD controller. If the external LCD enabled, the pin is always output except the power saving mode.
PT2_2 LCD_RW	87	I/O	**Bit-2 of Port 2** This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register. The PT2_2 is also as the read/write signal of external LCD controller. If the external LCD enabled, the pin is always output except the power saving mode.
PT2_1 LVD#	88	I/O	**Bit-1 of Port 2** This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register. The PT2_1 is also as the output of LVD. If the LVD enabled, the pin is always output except the power saving mode.
PT2_0 WE25	89	I/O	**Bit-0 of Port 2** This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register. The PT2_0 is also as the write control of register $25. If the write register $25 enabled, the pin is always output except the power saving mode.

IOUT1	84	OUT	**DAC1 Current Output** This pin is the current output of DAC1.
IOUT2	82	OUT	**DAC2 Current Output** This pin is the current output of DAC2.
ADDR[13:0] FL_S0 FL_S1	8,10 21-26 31-33 96-98	OUT	**14-bit Address Bus.** These signal are used for external memory address bus. FL_S0 ↔ A11, FL_S1 ↔ A10 jointly pin.
D[7:0]	12~19	I/O	**8-bit Data Bus.** These signal are used for external memory data bus.
FL_CE#	10	OUT	**Flash Chip Select, active low.** This signal is used for external flash.
FL_WE#	92	OUT	**Flash Write Enable, active low.** This signal is used for external flash.
FL_OE#	8	OUT	**Flash Output Enable, active low.** This signal is used for external flash.
ROM_OE#	90	IN	**Flash Type Select.** This signal is used for external flash.
ROM_CE#	91	IN	**Flash Number 1 or 2 Select.** This signal is used for external flash.
BK[7:0] FL_S2 FL_2# FL_TY	34-38 90-92	OUT	**Flash BANK Select.** This signal is used for external flash. FL_S2 ↔BK1, FL_2# ↔BK2, FL_TY ↔BK5 jointly pin.
XCLKI	58	IN	**Oscillator Input.** This is the input signal of internal PLL.
XCLKQ	57	OUT	**Oscillator Output.** This is the output signal of internal PLL.
C1, C2	56, 55	IN	**Capacitor Input.** These two signals are connected to the external capacitor for internal PLL.
VDD	3, 39, 48, 54, 69, 99	PWR	**Power Supply Voltage.**
AVDD	83	PWR	**Analog Power Supply Voltage.**
GND	5, 30, 49, 50, 66, 76, 100	PWR	**Ground.**
AGND	81,85	PWR	**Analog Ground.**

Development

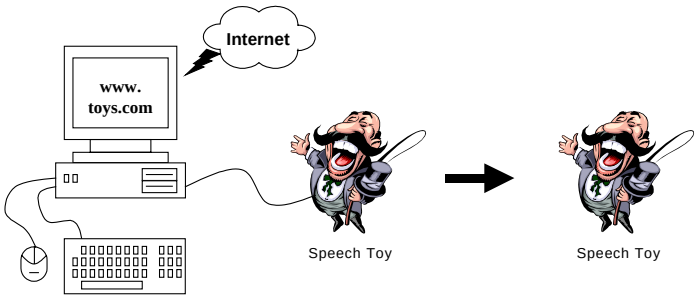
The RA8900 support the ISP(In-System Programming) and ISD(In-System Debugging) functions for customer to develop their system. Users can download their programs as well as data from a PC host to the external Flash ROM.

-ISP/ISD Mode is entered when the MONITOR# pin having been pulled down to ground voltage level. The on-chip Monitor program together with RAiO's ICE(RICE-2000) Utility Program running on a PC will be executed to support ICE debugging and ISP download of user programs from the PC Host.



Develop Program from ISP Mode
(Customers)

-***User Mode*** is entered when the MONITOR# pin has been pulled up to logic high voltage level. User application programs can be executed only in this mode. The end-user can download the application program or data from the customer's website through the PC interface. Because the program/data was stored in the flash so the application device of customer(such as speech toy) will operate independent that after disconnect with the PC.



Down load from Internet
(End-Users)

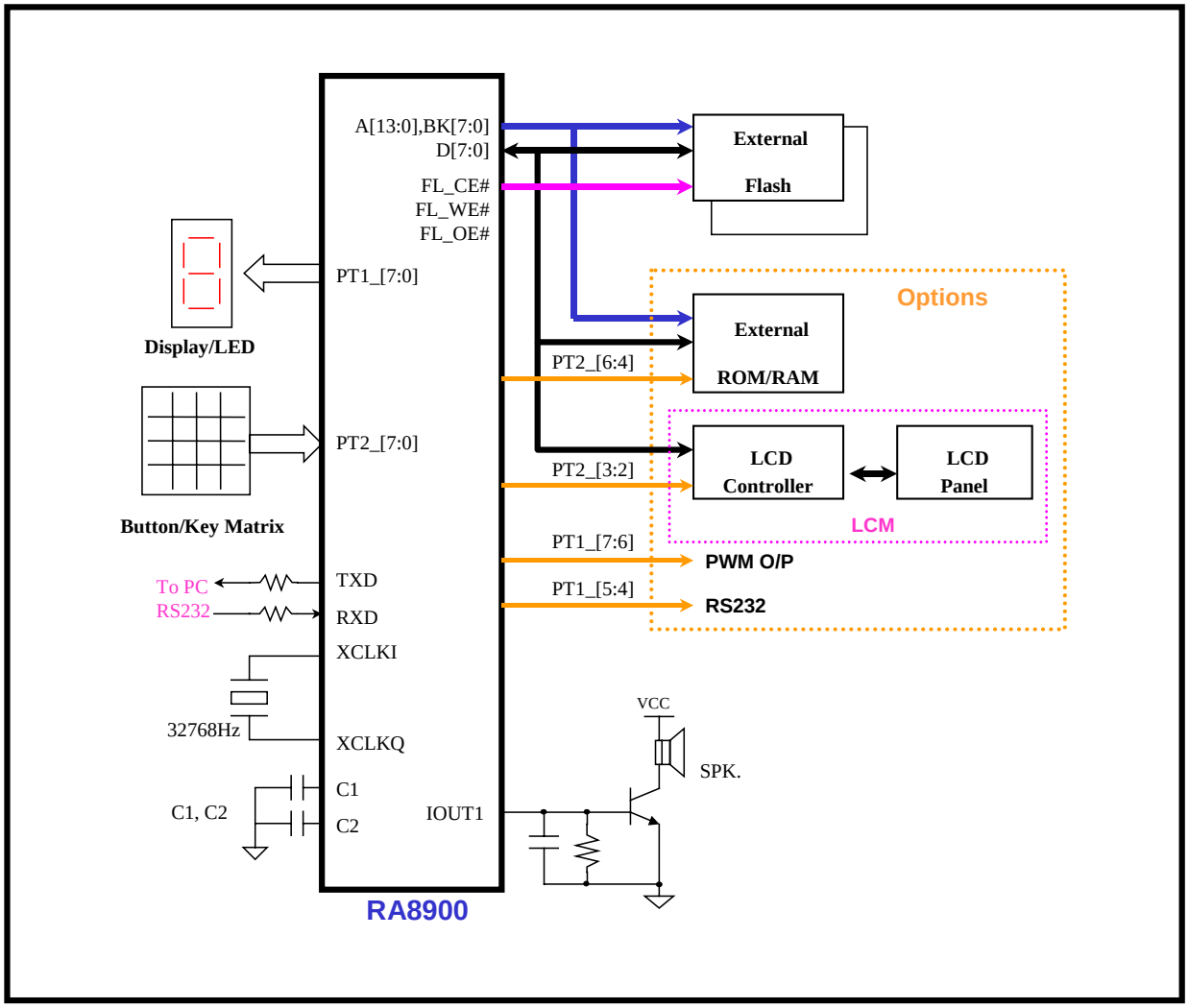
A Portable Speech Toy

RICE-2000 (RICE for short) is a full-completed environment developed by RAiO especially for RA89XX series. The major reason for developing RICE is give fully convenience to program designers who are using RA89XX IC, and let them enjoy consistent and friendly design environment at planning, designing and debugging. In RICE environment, it saves a great deal of developing time by not only providing Editor for users to do direct coding, but also providing many Hot-Key functions for users to do direct compiling, linking, and downloading. Since RA89XX series carry e-MCU micro-processor and a framework of ISP(In-System-Programming), ISD(In-System Debugging), then this simple and reliable environment of RICE can let program designers to proceed design and debug in Real Chip. Moreover, the mass-production ICs is ready for clients to do planning and designing directly without diverse traits happened between developing time and mass production period.

In the meanwhile, in order to support integrated speech interface, RICE provides a solution of 32K-bps ADPCM for programmers to easily combine programs and speech files. If you want to have more information and program design skills of RA8900, please refer to the user manual of RICE-2000.

Application

The following Block diagram is the basic application circuit of RA8900. We also give three examples on the user manual of RICE-2000 to let users have more understanding of RA8900 and the develop environment of RICE-2000, and then start to proceed program designing and product developing. The examples have one simple I/O control and two speech samples. Please refer to the user manual of RICE-2000 if you needed.


A[13:0],BK[7:0]
D[7:0]
FL_CE#
FL_WE#
FL_OE#
PT1_[7:0]
PT2_[7:0]
TXD
RXD
XCLKI
XCLKQ
C1
C2
IOUT1
RA8900
External
Flash
Options
External
ROM/RAM
PT2_[6:4]
LCD
Controller
LCD
Panel
LCM
PT2_[3:2]
PT1_[7:6]
PWM O/P
PT1_[5:4]
RS232
Display/LED
Button/Key Matrix
To PC
RS232
32768Hz
C1, C2
VCC
SPK.