MediaClock™ Mini Disc Clock Generator

Features

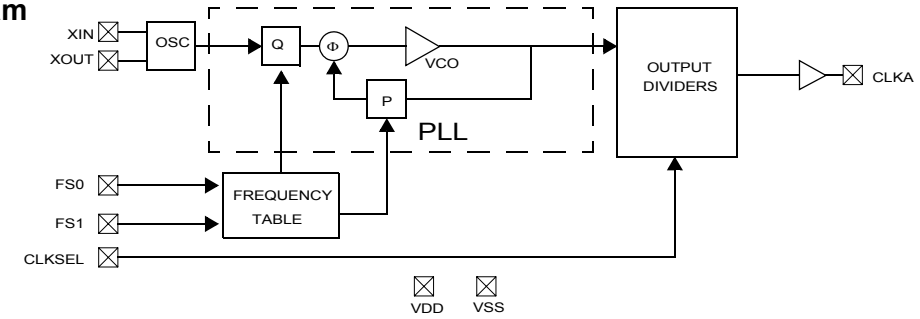
- Integrated phase-locked loop (PLL)
- Low-jitter, high-accuracy outputs
- 3.3V operation
- 8-pin SOIC package

Benefits

- High-performance PLL tailored for mini disc applications
- Meets critical timing requirements in complex system designs
- Enables application compatibility
- Industry standard package saves on board space

Part Number	Outputs	Input Frequency Range	Output Frequencies
CY24115-1	1	1 MHz–30 MHz	45.1584 MHz/90.3168 MHz (selectable)
CY24115-2	1	1 MHz–30 MHz	90.3168 MHz/180.6336 MHz (selectable)

Logic Block Diagram



Pin Configurations

CY24115
8-pin SOIC

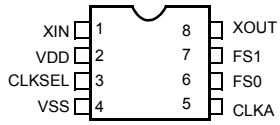


Table 1. CLKSEL Function CY24115-1

CLKSEL	CLKA	Unit	PPM Error
0	45.1584	MHz	0
1	90.3168	MHz	0

Table 2. CLKSEL Function, CY24115-2

CLKSEL	CLKA	Unit	PPM Error
0	90.3168	MHz	0
1	180.6336	MHz	0

Table 3. Input Frequency Function, CY24115-1 and CY24115-2

FS1	FS0	Xtal Input	Unit
0	0	2.8224	MHz
0	1	5.6448	MHz
1	0	11.2896	MHz
1	1	22.5792	MHz

Pin Summary

Pin Name	Pin Number	Pin Description
X_{IN}	1	Reference input (crystal or external input)
V_{DD}	2	3.3V voltage supply
CLKSEL	3	CLKA Select Line For 24115-1, see *Table 1* for output values For 24115-2, see *Table 2* for output values
V_{SS}	4	Ground
CLKA	5	24115-1: 45.1584 MHz/90.3168 MHz (frequency selectable). See *Table 1*. 24115-2: 90.3168 MHz/180.6336 MHz (frequency selectable). See *Table 2*.
FS0	6	Input Frequency FS0. See *Table 3*.
FS1	7	Input Frequency FS1. See *Table 3*.
X_{OUT}[1]	8	Reference Output

Absolute Maximum Conditions

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	–0.5	7.0	V
T_S	Storage Temperature[2]	–65	125	°C
T_J	Junction Temperature		125	°C
	Digital Inputs	V_{SS} – 0.3	V_{DD} + 0.3	V
	Digital Outputs Referred to V_{DD}	V_{SS} – 0.3	V_{DD} + 0.3	V
	Electrostatic Discharge	2		kV

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	3.14	3.3	3.47	V
T_A	Ambient Temperature	0		70	°C
C_{LOAD}	Max. Load Capacitance			15	pF
f_{REF}	Reference Frequency	2.8224		22.5792	MHz
t_1	Driven Reference Edge Rate	0.8			V/ns
DC_{IN}	Driven Reference Duty Cycle	40		60	%
C_{IN}	X_{IN}, X_{OUT} capacitance		12		pF
t_{PU}	Power-up time for all VDD's to reach minimum specified voltage (power ramps must be monotonic)	0.05		500	ms

DC Electrical Characteristics

Parameter	Name	Description	Min.	Typ.	Max.	Unit
I_{OH}	Output High Current	$V_{OH} = V_{DD} – 0.5$, V_{DD} = 3.3V (source)	12	24		mA
I_{OL}	Output Low Current	V_{OL} = 0.5, V_{DD} = 3.3V (sink)	12	24		mA
C_{IN}	Input Capacitance	CLKSEL, FS0, FS1, excludes XIN, XOUT			7	pF
V_{IL}	Input Low Voltage				30	% of V_{DD}
V_{IH}	Input High Voltage		70			% of V_{DD}
I_{IZ}	Input Leakage Current			5		μA
I_{DD}	Supply Current	Sum of Core and Output Current			35	mA

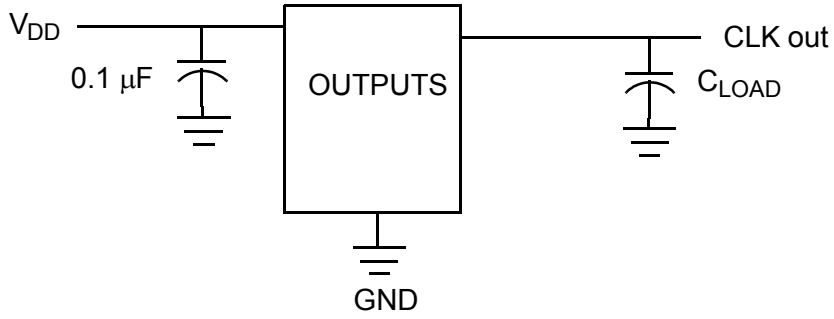
Notes:
1. Float X_{OUT} if X_{IN} is externally driven.
2. Rated for 10 years.

AC Electrical Characteristics (V_{DD} = 3.3V)

Parameter[3]	Name	Description	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	Duty Cycle is defined in Figure 1, 50% of V_{DD}	45	50	55	%
t_3	Rising Edge Slew Rate	Output Clock Rise Time, 20%–80% of V_{DD}	0.8	1.4		V/ns
t_4	Falling Edge Slew Rate	Output Clock Fall Time, 80%–20% of V_{DD}	0.8	1.4		V/ns
t_9	Clock Jitter	Peak to Peak period jitter			350	ps
t_{10}	PLL Lock Time				3	ms

Notes:
3. Not 100% tested.

Test Circuit



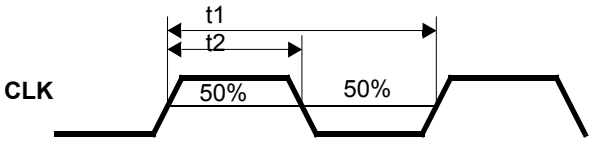


Figure 1. Duty Cycle Definition; DC = t2/t1

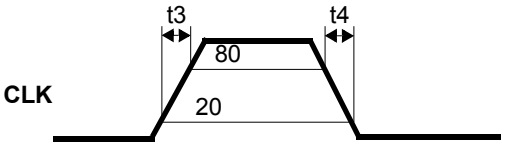


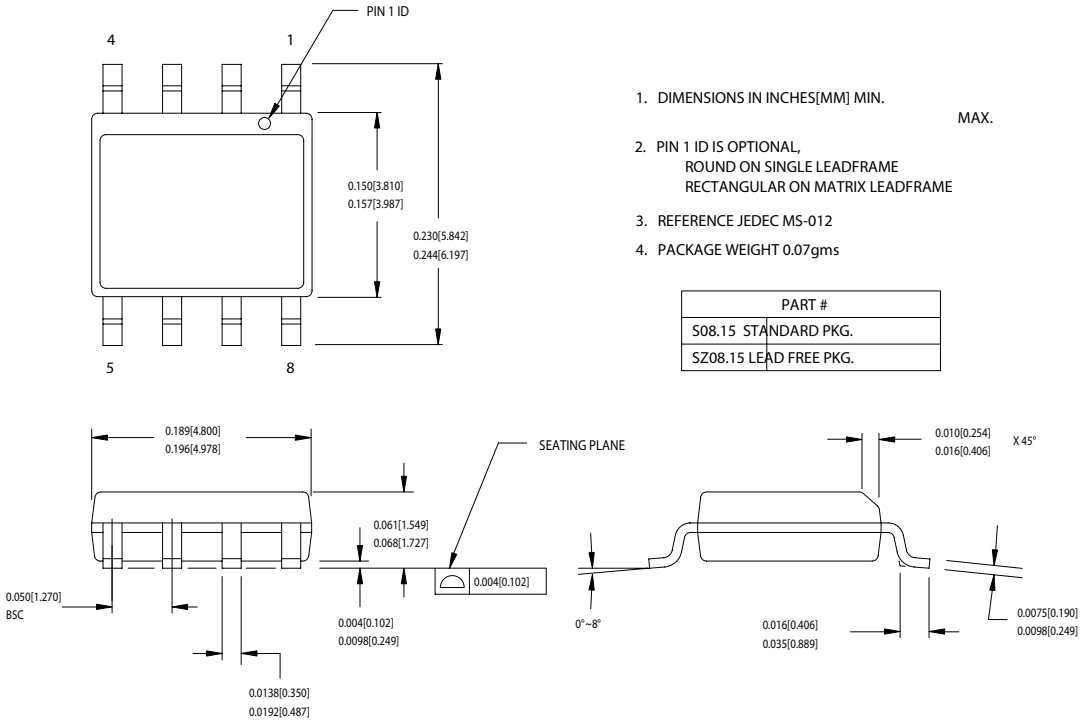
Figure 2. Rise and Fall Time Definitions

Ordering Information

Ordering Code	Package Type	Operating Range	Operating Voltage
CY24115SC-1	8-pin SOIC	Commercial	3.3V
CY24115SC-1T	8-pin SOIC - Tape and Reel	Commercial	3.3V
CY24115SC-2	8-pin SOIC	Commercial	3.3V
CY24115SC-2T	8-pin SOIC - Tape and Reel	Commercial	3.3V
Lead Free			
CY24115SXC-1	8-pin SOIC	Commercial	3.3V
CY24115SXC-1T	8-pin SOIC - Tape and Reel	Commercial	3.3V
CY24115SXC-2	8-pin SOIC	Commercial	3.3V
CY24115SXC-2T	8-pin SOIC - Tape and Reel	Commercial	3.3V

Package Drawing and Dimensions

8-lead (150-Mil) SOIC S8



1. DIMENSIONS IN INCHES[MM] MIN.
   MAX.
2. PIN 1 ID IS OPTIONAL,
   ROUND ON SINGLE LEADFRAME
   RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

PART #
S08.15 STANDARD PKG.
SZ08.15 LEAD FREE PKG.

51-85066-*C

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REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110767	02/06/02	CKN	New Data Sheet
*A	113515	04/30/02	CKN	Changed from Preliminary to Final P. 2 in Electrical Characteristics table added (source) to row 1 and (sink) to row 2
*B	121884	12/14/02	RBI	Power up requirements added to Operating Conditions Information
*C	252154	See ECN	RGL	Added Lead Devices