# 30-40GHz Medium Power Amplifier

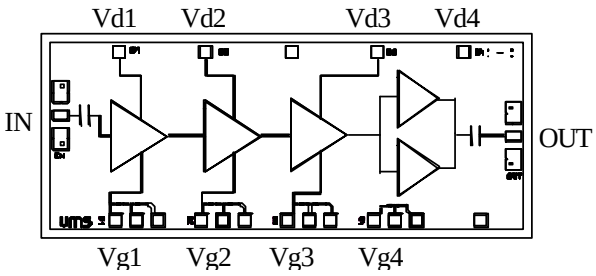
## GaAs Monolithic Microwave IC

preliminary

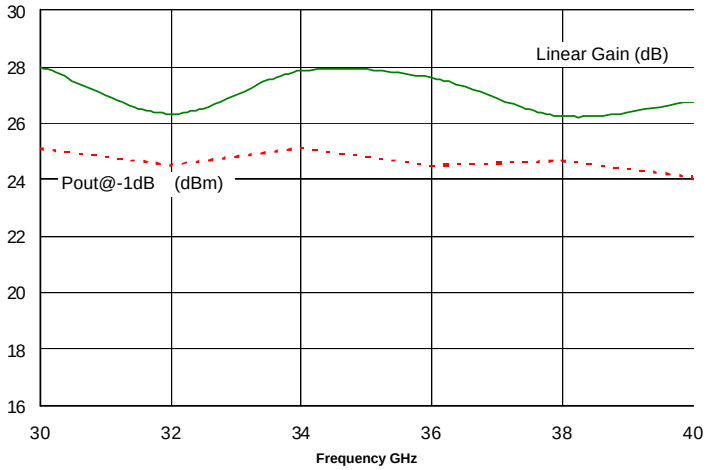
## Description

The CHA5294 is a high gain four-stage monolithic medium power amplifier. It is designed for a wide range of applications, from military to commercial communication systems. The backside of the chip is both RF and DC grounded. This helps to simplify the assembly process.

The circuit is manufactured with a PM-HEMT process, 0.15µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is available in chip form.




**Typical on jig Measurements**




## Main Features

- Performances : 30-40GHz
- 24dBm output power @ 1dB comp.
- 26 dB gain
- DC power consumption, 500mA @ 4V
- Chip size : 4.10 x 1.42 x 0.07 mm

## Main Characteristics

Tamb. = 25°C

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Fop | Operating frequency range | 30 | | 40 | GHz |
| G | Small signal gain | | 26 | | dB |
| P1dB | Output power at 1dB gain compression | | 24 | | dBm |
| Id | Bias current | | 500 | | mA |

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !



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## Electrical Characteristics on wafer

Tamb = +25°C

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| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Fop | Operating frequency range (1) | 30 | | 40 | GHz |
| G | Small signal gain (1) | | 24 | | dB |
| ΔG | Small signal gain flatness (1) | | ±1.5 | | dB |
| Is | Reverse isolation | | 40 | | dB |
| P1dB | Pulsed output power at 1dB compression (1) | | 24 | | dBm |
| P03 | Output power at 3dB gain compression (1) | | 25 | | dBm |
| IP3 | Output Intercept point 3rd order | | 32 | | dBm |
| VSWRin | Input VSWR (1) | | 2.0:1 | | |
| VSWRout | Output VSWR(1) | | 4.0:1 | | |
| Vd | Drain bias DC voltage | | 4 | | V |
| Id | Bias current @ small signal | | 500 | 650 | mA |

(1) These values are representative for pulsed on-wafer measurements that are made without bonding wires at the RF ports.

## Absolute Maximum Ratings

Tamb. = 25°C (1)

| Symbol | Parameter | Values | Unit |
|---|---|---|---|
| Vd | Maximum Drain bias voltage with Pin max=0dBm | +4.5 | V |
| Id | Drain bias current with Vd=4V | 750 | mA |
| Vg | Gate bias voltage | -2 to +0.4 | V |
| Vdg | Maximum drain to gate voltage (Vd - Vg) | +6.0 | V |
| Pin | Maximum input power overdrive (2) | +3.0 | dBm |
| Tch | Maximum channel temperature | +175 | °C |
| Ta | Operating temperature range | -40 to +80 | °C |
| Tstg | Storage temperature range | -55 to +125 | °C |

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) Duration < 1s.



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## Typical on Jig Measurements

Bias conditions: Vd=4V, Vg tuned for Id = 500mA

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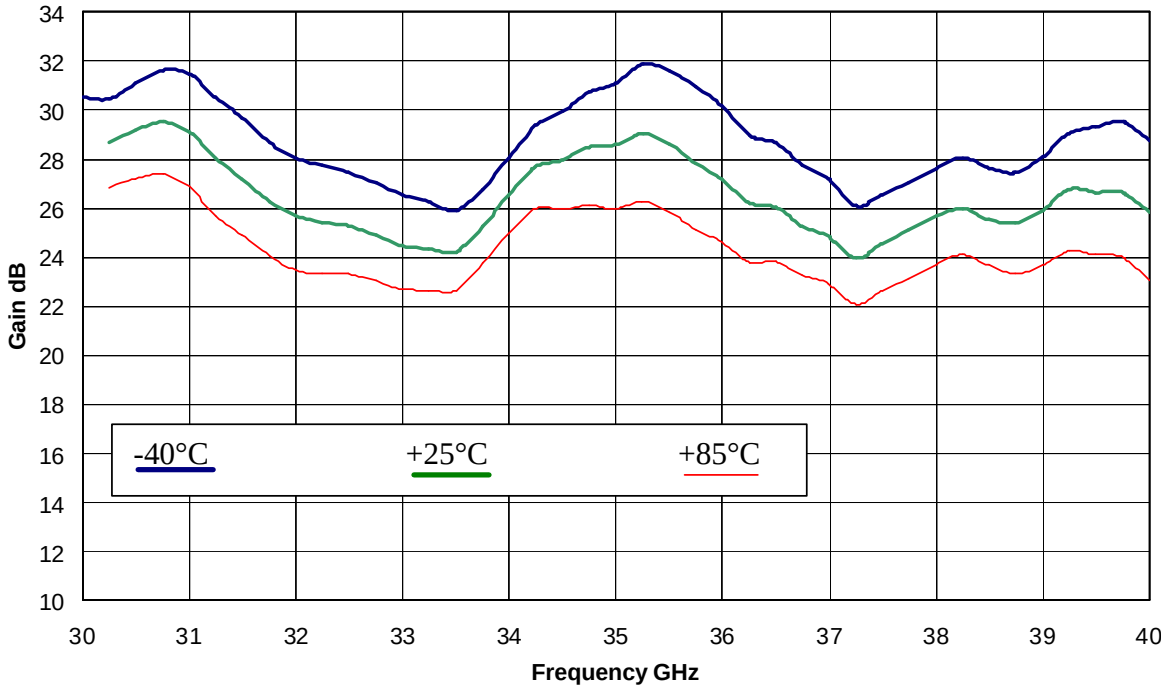
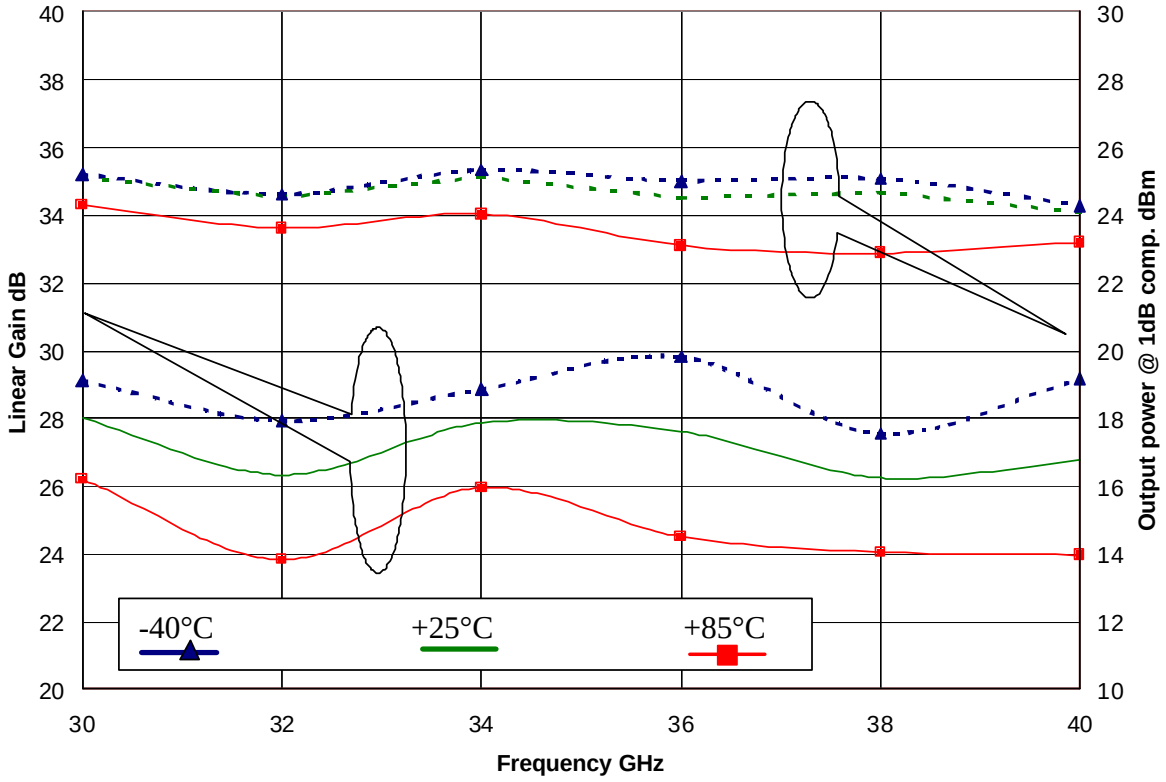
### Linear Gain versus frequency & temperature




### Linear Gain & Output power at 1dB compression vs frequency & temperature



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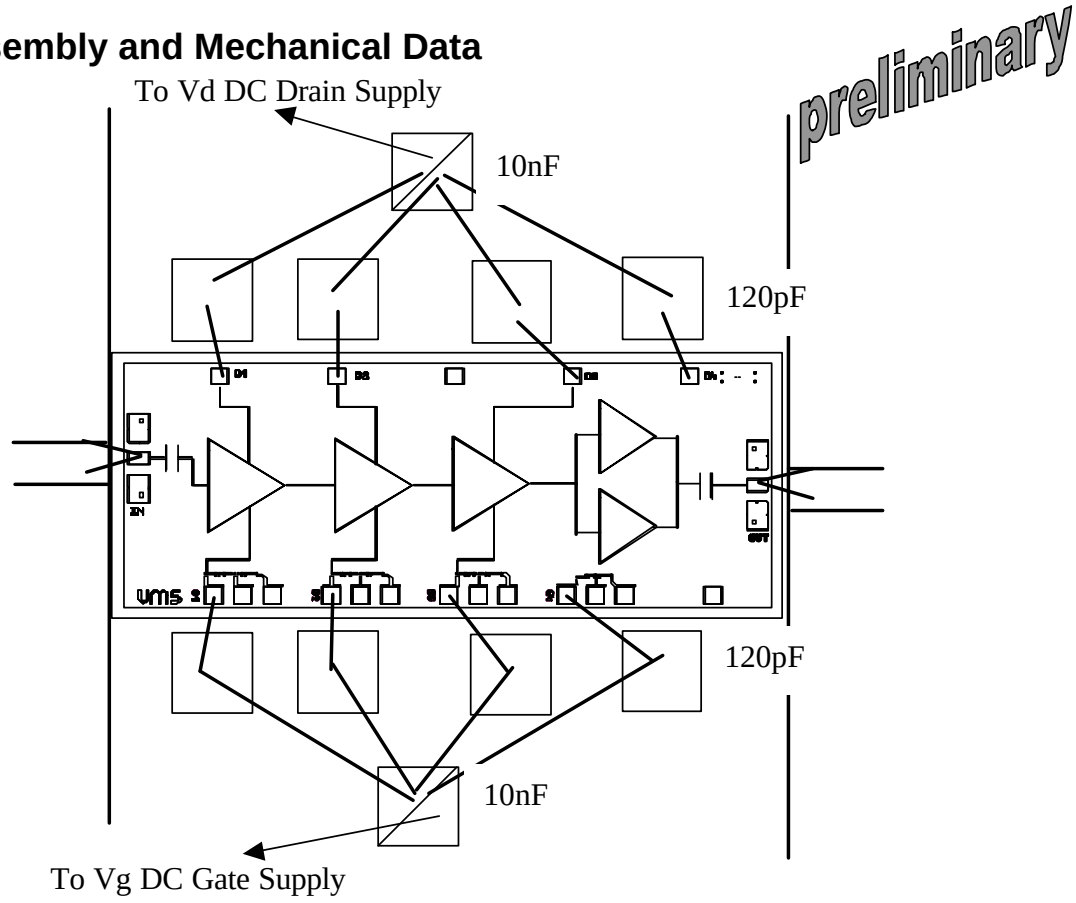
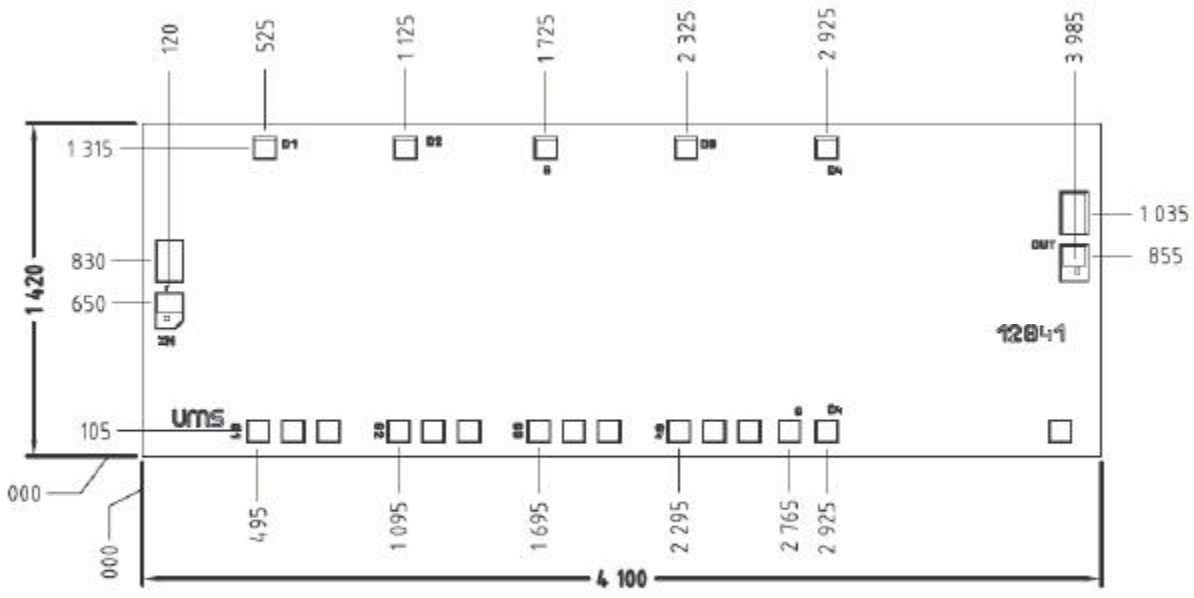
## Chip Assembly and Mechanical Data




Note : Supply feed should be capacitively bypassed. 25µm diameter gold wire is to be prefered.




UNITS : µm
Tol : ±35µm

**Bonding pad positions.**
( Chip thickness : 70µm)



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## Application note

Bias operation sequence:

ON: Supply Gate voltage
Supply Drain voltage
OFF: Cut off Drain voltage
Cut off Gate voltage

Due to 70µm thickness, specific care is requested for the handling and assembly.



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## Ordering Information

Chip form : CHA5294-99F/00





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