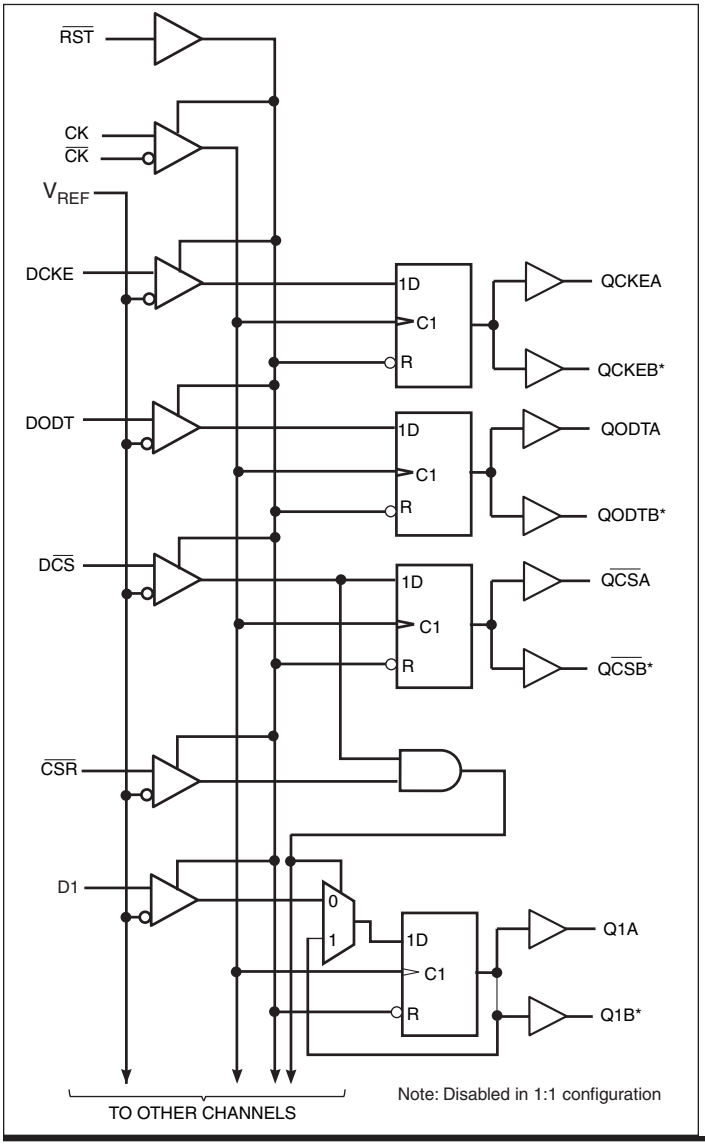
25-Bit 1:1 or 14-Bit 1:2 Configurable Registered Buffer

Features

- Designed for low-voltage operation: V_{DD} = 1.8V
- Supports Low Power Standby Operation
- Enhanced Signal Integrity for 1 and 2 Rank Modules
- All Inputs are SSTL_18 compatible, except $\overline{RST}$, C0, C1, which are LVCMOS.
- Output drivers are optimized to drive DDR2 DIMM loads
- Packaging (Pb-free & Green available): 96-Ball LFBGA (NB)
- Used in DDR2-400/533/667 memory applications

Block Diagram 1:2 Mode (Positive Logic)



Description

Pericom Semiconductor's PI74SSTUA32864 is a 25-Bit 1:1 or 14-Bit 1:2 configurable registered buffer and designed for 1.7V to 1.9V V_{DD} operation.

All clock and data inputs are compatible with the JEDEC standard for SSTL_18. The control inputs are LVCMOS. All outputs are 1.8V drivers that have been optimized to drive the DDR2 DIMM load, and meet SSTL_18 specifications.

The device operates from a differential clock (CK and $\overline{CK}$). Data is registered at the crossing of CK going high, and $\overline{CK}$ going low.

The C0 input controls the pinout configuration of the 1:2 pinout from A configuration (when LOW) to B configuration (when HIGH). The C1 input controls the pinout configuration for 25-Bit 1:1 (when LOW) to 14-Bit 1:2 (when HIGH).

The device supports low-power standby operation. When the reset input ($\overline{RST}$) is low, the differential input receivers are disabled and undriven (floating) data, clock and reference voltage (V_{REF}) inputs are allowed. In addition , when $\overline{RST}$ is low, all registers are reset, and all outputs are forced low. The LVCMOS $\overline{RST}$ and Cn inputs must always be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{RST}$ must be held in the low state during power up.

In the DDR2 RDIMM application, $\overline{RST}$ is specified to be completely asynchronous with respect to CK and $\overline{CK}$. Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the outputs will be driven low quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers.

As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of $\overline{RST}$ until the input receivers are fully enabled, the design of the registered buffer must ensure that the outputs remain low, thus ensuring no glitches on the output.

The device monitors both $\overline{DCS}$ and $\overline{CSR}$ inputs and will gate the Qn outputs from changing states when both $\overline{DCS}$ and $\overline{CSR}$ inputs are high. If either $\overline{DCS}$ or $\overline{CSR}$ input is low, the Qn outputs will function normally. The $\overline{RST}$ input has priority over the $\overline{DCS}$ and $\overline{CSR}$ control will force the outputs low. If the $\overline{DCS}$ control functionality is not desired, then the $\overline{CSR}$ input can be hardwired to ground, in which case, the set-up time requirement for $\overline{DCS}$ would be the same as for the other D data inputs.

Pin Configuration 1:1 Register (C0 = 0, C1 = 0)

	1	2	3	4	5	6
A	DCKE	NC	V_{REF}	V_{DD}	QCKE	NC
B	D2	D15	GND	GND	Q2	Q15
C	D3	D16	V_{DD}	V_{DD}	Q3	Q16
D	DODT	NC	GND	GND	QODT	NC
E	D5	D17	V_{DD}	V_{DD}	Q5	Q17
F	D6	D18	GND	GND	Q6	Q18
G	NC	$\overline{RST}$	V_{DD}	V_{DD}	C1	C0
H	CK	D$\overline{CS}$	GND	GND	Q$\overline{CS}$	NC
J	$\overline{CK}$	$\overline{CSR}$	V_{DD}	V_{DD}	ZOH	ZOL
K	D8	D19	GND	GND	Q8	Q19
L	D9	D20	V_{DD}	V_{DD}	Q9	Q20
M	D10	D21	GND	GND	Q10	Q21
N	D11	D22	V_{DD}	V_{DD}	Q11	Q22
P	D12	D23	GND	GND	Q12	Q23
R	D13	D24	V_{DD}	V_{DD}	Q13	Q24
T	D14	D25	V_{REF}	V_{DD}	Q14	Q25

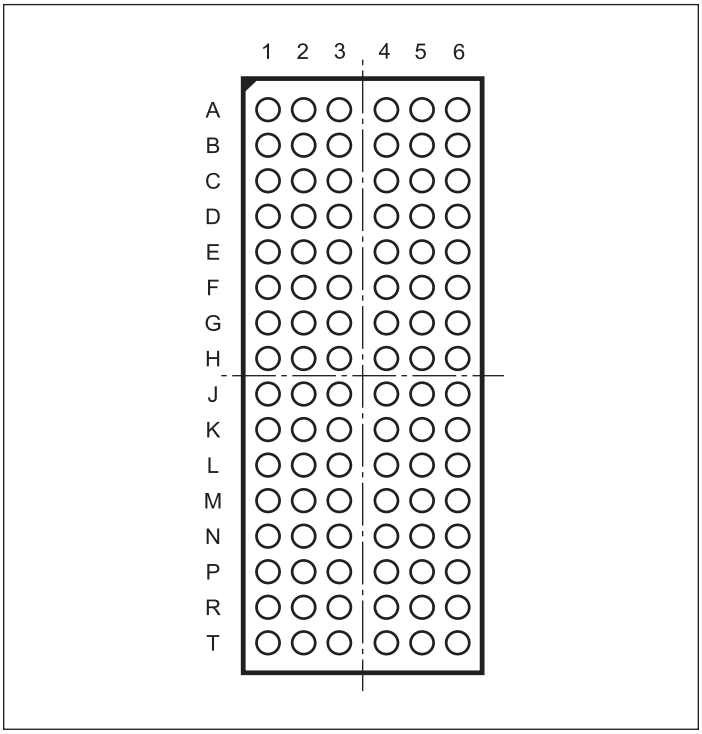
Pin Configuration 1:2 Register (C0 = 0, C1 = 1)

	1	2	3	4	5	6
A	DCKE	NC	V_{REF}	V_{DD}	QCKEA	QCKEB
B	D2	NC	GND	GND	Q2A	Q2B
C	D3	NC	V_{DD}	V_{DD}	Q3A	Q3B
D	DODT	NC	GND	GND	QODTA	QODTB
E	D5	NC	V_{DD}	V_{DD}	Q5A	Q5B
F	D6	NC	GND	GND	Q6A	Q6B
G	NC	$\overline{RST}$	V_{DD}	V_{DD}	C1	C0
H	CK	D$\overline{CS}$	GND	GND	Q$\overline{CS}$A	Q$\overline{CS}$B
J	$\overline{CK}$	$\overline{CSR}$	V_{DD}	V_{DD}	ZOH	ZOL
K	D8	NC	GND	GND	Q8A	Q8B
L	D9	NC	V_{DD}	V_{DD}	Q9A	Q9B
M	D10	NC	GND	GND	Q10A	Q10B
N	D11	NC	V_{DD}	V_{DD}	Q11A	Q11B
P	D12	NC	GND	GND	Q12A	Q12B
R	D13	NC	V_{DD}	V_{DD}	Q13A	Q13B
T	D14	NC	V_{REF}	V_{DD}	Q14A	Q14B

Pin Configuration 1:2 Register (C0 = 1, C1 = 1)

	1	2	3	4	5	6
A	D1	NC	V_{REF}	V_{DD}	Q1A	Q1B
B	D2	NC	GND	GND	Q2A	Q2B
C	D3	NC	V_{DD}	V_{DD}	Q3A	Q3B
D	D4	NC	GND	GND	Q4A	Q4B
E	D5	NC	V_{DD}	V_{DD}	Q5A	Q5B
F	D6	NC	GND	GND	Q6A	Q6B
G	NC	$\overline{RST}$	V_{DD}	V_{DD}	C1	C0
H	CK	D$\overline{CS}$	GND	GND	Q$\overline{CS}$A	Q$\overline{CS}$B
J	$\overline{CK}$	$\overline{CSR}$	V_{DD}	V_{DD}	ZOH	ZOL
K	D8	NC	GND	GND	Q8A	Q8B
L	D9	NC	V_{DD}	V_{DD}	Q9A	Q9B
M	D10	NC	GND	GND	Q10A	Q10B
N	DODT	NC	V_{DD}	V_{DD}	QODTA	QODTB
P	D12	NC	GND	GND	Q12A	Q12B
R	D13	NC	V_{DD}	V_{DD}	Q13A	Q13B
T	DCKE	NC	V_{REF}	V_{DD}	QCKEA	QCKEB

NB, 96-ball LFBGA (MO-205CC)



Terminal Functions

Name	Description	Characteristics
GND	Ground	Ground Input
V_{DD}	Power Supply	1.8V nominal
V_{REF}	Input Reference Voltage	0.9V nominal
Z_{OH}	Reserved for future use	Input
Z_{OL}	Reserved for future use	Input
CK	Positive master clock input	Differential Clock input
$\overline{CK}$	Negative master clock input	Differential Clock input
C0, C1	Configuration control inputs	LVCMOS inputs
$\overline{RST}$	Asynchronous reset input - resets registers and disables V_{REF} data and clock differential - input receivers	LVCMOS inputs
$\overline{CSR}$, $\overline{DCS}$	Chip select inputs disables D1-D24 outputs switching when both inputs are high	SSTL_18 input
D1, D25	Data input - clocked in on the crossing of the rising edge of CK and the falling edge of $\overline{CK}$	SSTL_18 input
DODT	The outputs of this register bit will not be suspended by the $\overline{DCS}$ and $\overline{CSR}$ control	SSTL_18 input
DCKE	The outputs of this register bit will not be suspended by the $\overline{DCS}$ and $\overline{CSR}$ control	SSTL_18 input
Q1-Q25	Data outputs that are suspended by the $\overline{DCS}$ and $\overline{CSR}$ control	1.8V CMOS
$Q\overline{CS}$	Data output that will not be suspended by the $\overline{DCS}$ and $\overline{CSR}$ controll	1.8V CMOS
QODT	Data output that will not be suspended by the $\overline{DCS}$ and $\overline{CSR}$ controll	1.8V CMOS
QCKE	Data output that will not be suspended by the $\overline{DCS}$ and $\overline{CSR}$ controll	1.8V CMOS

Function Table (each flip-flop)

Inputs						Outputs		
$\overline{RST}$	$D\overline{CS}$	$\overline{CSR}$	CK	$\overline{CK}$	Dn, DODT, DCKE	Qn	$Q\overline{CS}$	QODT, QCKE
H	L	L	↑	↓	L	L	L	L
H	L	L	↑	↓	H	H	L	H
H	L	L	L or H	L or H	X	Q0	Q0	Q0
H	L	H	↑	↓	L	L	L	L
H	L	H	↑	↓	H	H	L	H
H	L	H	L or H	L or H	X	Q0	Q0	Q0
H	H	L	↑	↓	L	L	H	L
H	H	L	↑	↓	H	H	H	H
H	H	L	L or H	L or H	X	Q0	Q0	Q0
H	H	H	↑	↓	L	Q0	H	L
H	H	H	↑	↓	H	Q0	H	H
H	H	H	L or H	L or H	X	Q0	Q0	Q0
L	X or floating	X or floating	X or floating	X or floating	X or floating	L	L	L

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Supply Voltage Range, V_{DD}	–0.5V to 2.5V
Input Voltage Range, V_I : (See Notes 2 and 3):	–0.5V to 2.5V
Output Voltage Range, V_O (See Notes 2 and 3)	–0.5V to V_{DD} + 0.5V
Input Clamp Current, I_{IK} (V_I < 0 or V_I = V_{DD})	–50mA
Output Clamp Current, I_{OK} (V_O < 0 or V_O > V_{DD})	±50mA
Continous Output Current, I_O (V_O = 0 to V_{DD})	±50mA
Continous Current through each V_{DD} or GND	±100mA

Notes:

1. Stresses greater than those listed under MAXIMUM RAINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. This value is limited to 2.5V maximum

Recommended Operating Conditions(1)

Parameters	Description		Min.	Nom.	Max.	Units
V_{DD}	Supply Voltage		1.7		1.9	V
V_{REF}	Reference Voltage		0.49 x V_{DD}	0.50 x V_{DD}	0.51 x V_{DD}	
V_{TT}	Termination Voltage		V_{REF} -40mA	V_{REF}	V_{REF} +40mA	
V_I	Input Voltage		0		V_{DD}	
V_{IH}	AC High - Level Input Voltage	Data Inputs	V_{REF} +250mV			
V_{IL}	AC Low- Level Input Voltage				V_{REF} -250mV	
V_{IH}	DC High - Level Input Voltage		V_{REF} +125mV			
V_{IL}	DC Low- Level Input Voltage				V_{REF} -125mV	
V_{IH}	High Level Input Voltage	$\overline{RST}$, CN	0.65 x V_{DD}			
V_{IL}	Low Level Input Voltage				0.35 x V_{DD}	
V_{ICR}	Common-mode input Voltage	CK, $\overline{CK}$	0.675		1.125	
V_{ID}	Differential Input Voltage		600			mV
I_{OH}	High-Level Output Current				-8	mA
I_{OL}	Low-Level Output Current				-8	
T_A	Operating Free-air Temperature		0		70	ºC

Notes:

1. The $\overline{RST}$ and Cn inputs of the device must be held at valid levels (not floating) to ensure proper device operation. The differential inputs must not be floating, unless $\overline{RST}$ is low.

Electrical Characteristics Over Recommended Operating Free Air Temperature range

Parameters	Description	Test Conditions		V_{DD}	Min.	Nom.	Max.	Units
V_{OH}		I_{OH} = -6 mA		1.7V	1.2			V
V_{OL}		I_{OL} = 6 mA		1.7V			0.5	
I_I	All inputs	$V_I = V_{DD}$ or GND					±5	µA
I_{DD}	Static Stand-by	$\overline{RST}$ = GND	I_O = 0	1.9V			100	
	Static Operating	$\overline{RST} = V_{DD}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$					40	mA
I_{DDD}	Dynamic Operating Clock only	$\overline{RST} = V_{DD}$, $V_I = V_{IH(AC)}$, or $V_{IL(AC)}$ CK and $\overline{CK}$ switching 50% duty cycle		1.8V	28			µA/ clock MHz
	Dynamic Operating - per each data input, 1:1 mode	$\overline{RST} = V_{DD}$, $V_I = V_{IH(AC)}$, or $V_{IL(AC)}$ CK and $\overline{CK}$ switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle			36			µA/ clock MHz data input
	Dynamic Operating - per each data input, 1:2 mode	$\overline{RST} = V_{DD}$, $V_I = V_{IH(AC)}$, or $V_{IL(AC)}$ CK and $\overline{CK}$ switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle			36			
C_I	Data inputs	$V_I = V_{REF}$ ±250mV			2.5		3.5	pF
	CK and $\overline{CK}$	V_{ICR} = 0.9V, V_{ID} = 600mV			2		3	
	$\overline{RST}$	$V_I = V_{DD}$ or GND				2.5		

Timing Requirements Over Recommended Operating Free Air Temperature range (See Figure 1)

Parameter	Description		Min.	Max	Units
f_{clock}	Clock frequency			350	MHz
t_W	Pulse Duration, CK, CK, High or low		1		ns
t_{act}(1)	Differential inputs active time(1)			10	
t_{inact}(1)	Differential inputs inactive time(2)			15	
t_{su}	Setup time	DCS before CK↑, CK↓, CSR high	0.7		
		$\overline{DCS}$ before CK↑, $\overline{CK}$↓, $\overline{CSR}$ low	0.5		
		$\overline{ODT}$, CKE and data before CK↑, CK↓	0.5		
th	Hold Time	DCS, ODT, CKE and data before CK↑, CK↓	0.5		

Notes:
1. This parameter is not necessarily production tested.
2. Data and V_{REF} inputs must be a low minimum time of t_{act} max, after $\overline{RST}$ is taken high.
3. Data and clock inputs must be held at valid levels (not floating) a minimum time of t_{inact} max after $\overline{RST}$ is taken low.

Switching Characteristics (Over Recommended Operating Free Air Temperature range)

Parameter	From	To (see Fig. 1)	Min.	Max.	Units
fmax				350	MHz
tpdm	CK and $\overline{CK}$	"Test Point"	1.2	1.90	ns
tpdmss (simultaneous switching)(1,2)	CK and $\overline{CK}$	"Test Point"		2.00	ns
tRPHL	$\overline{RST}$	Q	0	3	ns

Notes:
1. Includes 350ps test load transmission-line delay.
2. This parameter is not necessarily production tested.

Output Edge Rates Over Recommended Operating Free Air Temperature range (See Figure 2)

Parameter	V_{DD} = 1.8V ± 0.1V		Units
	Min.	Max.	
dV/dt_r	1	4	V/ns
dV/dt_f	1	4	
dV/dt(1)		1	

Notes:
1. Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate).

Test Circuit and Switching Waveforms

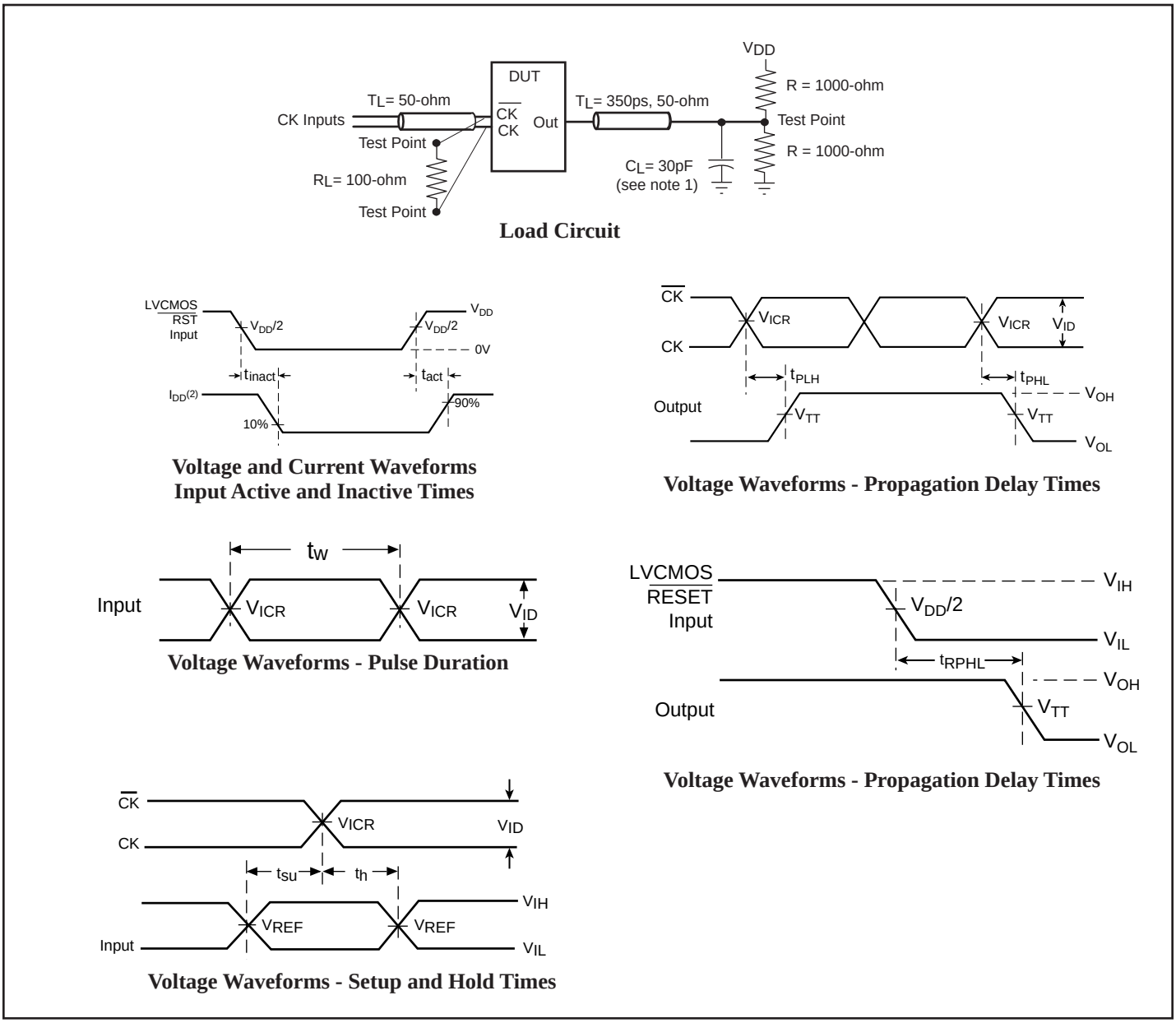
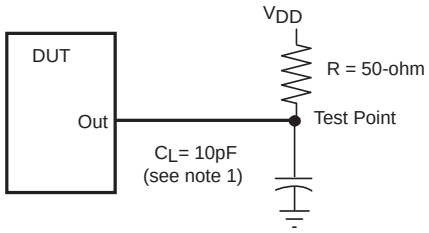
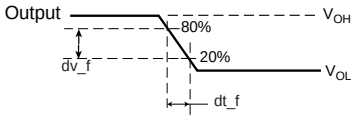


Figure 1. Parameter Measurement Information (V_{DD} = 1.8V ± 0.1V)

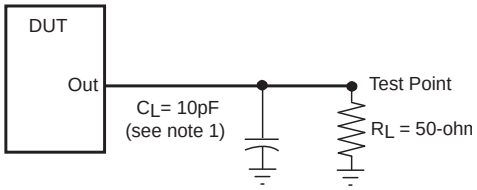
Notes:
1. C_L includes probe and jig capacitance
2. I_{DD} tested with clock and data inputs held at V_{DD} or GND and I_O = 0mA
3. All input pulses are supplied by generators having the following characteristics: Pulse Repertition Rate ≥ 10 MHz, ZO = 50Ω, input slew rate = 1V/ns ± 20% (unless otherwise specified).
4. The outputs are measured one at a time with one transition per measurement.
5. V_{REF} = V_{DD} /2
6. V_{IH} = V_{REF} +250mV (ac voltage levels) for differential inputs. V_{IH} = V_{DD} for LVCMOS input.
7. V_{IL} = V_{REF} -250mV (ac voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.
8. V_{ID} = 600mV
9. t_{PLH} and t_{PHL} are the same as t_{pdm}.



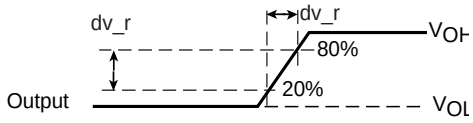
Load Circuit -High -to- Low Slew Rate Measurement



Voltage Waveforms - High -to- Low Slew Rate Measurement



Load Circuit - Low -to- High Slew Rate Measurement

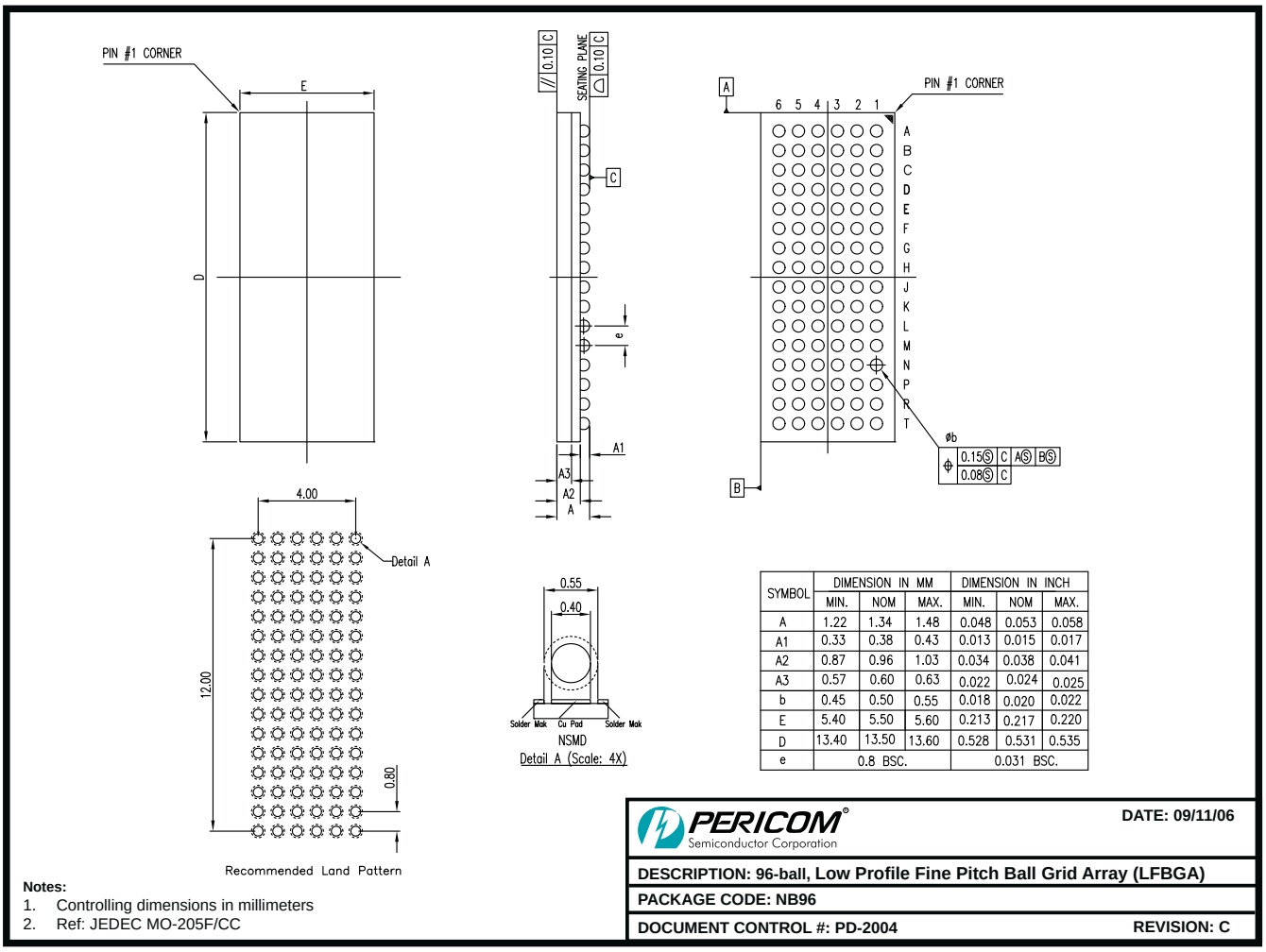


Voltage Waveforms - Low -to- High Slew Rate Measurement

Figure 2. Output Slew-Rate Measurement Information (V_{DD} = 1.8V ± 0.1V)

Notes:
1. C_L includes probe and jig capacitance
2. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10MHz, ZO = 50Ω, input slew rate = 1 V/ns ± 20% (unless otherwise specified).

Packaging Mechanical: 96-ball LFBGA (NB)



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	1.22	1.34	1.48	0.048	0.053	0.058
A1	0.33	0.38	0.43	0.013	0.015	0.017
A2	0.87	0.96	1.03	0.034	0.038	0.041
A3	0.57	0.60	0.63	0.022	0.024	0.025
b	0.45	0.50	0.55	0.018	0.020	0.022
E	5.40	5.50	5.60	0.213	0.217	0.220
D	13.40	13.50	13.60	0.528	0.531	0.535
e	0.8 BSC.			0.031 BSC.		

Notes:
1. Controlling dimensions in millimeters
2. Ref: JEDEC MO-205F/CC

PERICOM Semiconductor Corporation

DATE: 09/11/06

DESCRIPTION: 96-ball, Low Profile Fine Pitch Ball Grid Array (LFBGA)

PACKAGE CODE: NB96

DOCUMENT CONTROL #: PD-2004 **REVISION: C**

06-0735

Ordering Information

Ordering Code	Package Code	Package Description
PI74SSTUA32864NB	NB	96-Ball LFBGA
PI74SSTUA32864NBE	NB	Pb-free & Green, 96-Ball LFBGA

Notes:
1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. Number of Transistors = TBD