CYIA2SC0300AA-BQE

1/3” VGA-Format CMOS Image Sensor

Features

- **VGA Resolution**
- **1/3” Optical Format**
- **Automotive Grade device**
- **120 db Dynamic Range**
- **60 PIN CBGA**
- **Low power dissipation**

Functional Description

Cypress IM103 is Automotive grade CMOS Image Sensor with high dynamic range (120 db). IM103 is built with Autobrite® technology useful for Automotive Vision Systems which produce crisp clear video in visible and near IR wavelengths. Device can be used for Lane departure working, Night Vision, Adaptive Cruise control, driver drowsiness etc.

Introduction

This document describes the automotive grade IM103 1/3” format VGA CMOS image sensor. The description covers:

- **Architecture**
- **Operation**
- **Wide-dynamic-range capture**
- **Register settings**
- **Electrical and electro-optical specifications**

This imager chip can be supplied in several different configurations including:

- **Monochrome or color pixel array**

1 Sensor Architecture

The diagram in *Figure 1* shows the major functional blocks of the imager. These blocks include:

- **Image sensor array**
- **Row control circuitry**
- **Column sense circuitry**
- **Analog-to-digital converters**
- **Timing and control logic**
- **Program registers**
- **Digital-output shift registers**

Sensor array: The sensor array consists of an optically active 482 row X 642 column matrix, with 18 additional dark columns on right side of the array (the array is described more fully in section 3). Each sensing element (pixel) is 8 µm X 8 µm in size.

Timing and control circuitry: The sensor uses two clocks (data strobe or DSTR, and system clock or SCLK). Data strobe controls the timing of the output shift registers, while SCLK controls exposure and data conversion timing. Clocking details are given in section 5.

Column circuitry: The column circuitry includes a column amplifier (with correlated double sampling [CDS] capability) and a 12-bit analog-to-digital converter (ADC). Multiple ADCs operate in parallel across the array.

Output registers: Data from the ADCs are shifted into a parallel-in/serial-out 24-bit-wide row buffer. Data are shifted out to the parallel data I/O from the buffer after each row of data is converted.

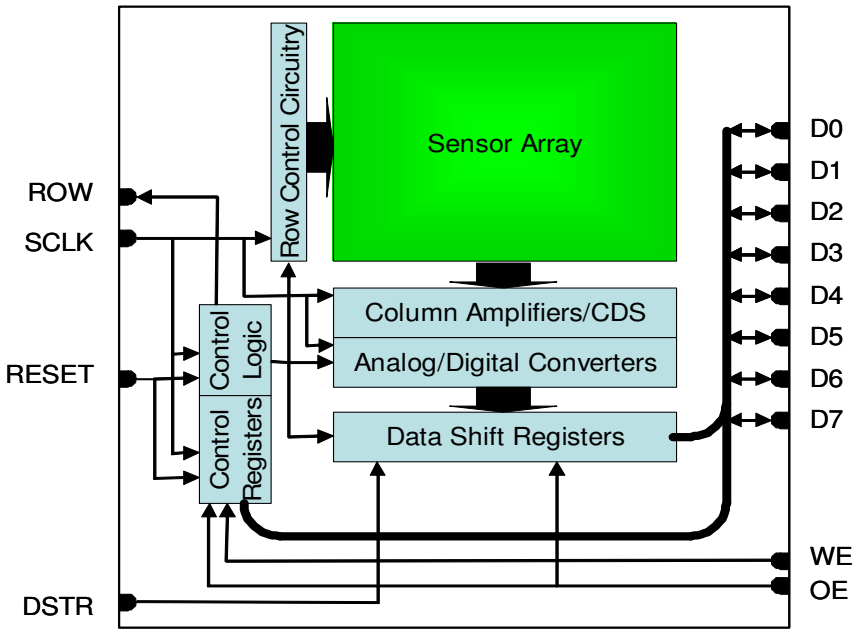


Figure 1. IM103 Image Sensor Block Diagram.

Control registers: Several on-chip programmable registers control exposure timing, digital gain, power, and dynamic range compression. These registers are described in more detail in section 7.

2 Pin Description

The image sensor is packaged in a 60-pin CBGA. Only 41 of the 60 balls are active (*Figure 2*). These active pins are listed in *Table 1*, and include 8 digital I/O lines, 2 clock inputs, 8 power supply pins, 15 ground pins, 3 analog references, a row-synchronization output, a test I/O, an initialization input, and 2 control inputs.

Pinout	1	2	3	4	5	6	7	8	9	10
A		VDDIO	NC	NC	NC	NC	GPIO	VDDA	VDDA	NC
B	VDDIO	GNDIO	NC	NC	NC	NC	NC	GNDA	VDDA	VREFP
C	D5	D7							GNDA	GNDA
D	D4	D6							GNDA	VREFM
E	GNDIO	GNDIO							NC	VCM
F	D3	D2							VDDD	VDDD
G	D1	GNDIO							SCLK	VDDD
H	GNDIO	GNDIO	GNDIO	D0	NC	NC	NC	OE_N	GNDD	GNDD
J	NC	GNDIO	DSTR	NC	ROW	NC	WE_N	GNDD	RESET	NC
				= NC						
				= depopulated						

Figure 2. Pin Diagram for the IM103 VGA-format Image Sensor[1, 2]

Table 1. IM103 Pin Assignments

Pin	Name	Function	Class[3]	Type[4]
A2,B1	VDDIO	I/O Power	P	PWR
C2	D7	Data I/O 7th bit (MSB)	D	I/O
D2	D6	Data I/O 6th bit	D	I/O
C1	D5	Data I/O 5th bit	D	I/O
D1	D4	Data I/O 4th bit	D	I/O
F1	D3	Data I/O 3rd bit	D	I/O
F2	D2	Data I/O 2nd bit	D	I/O
G1	D1	Data I/O 1st bit	D	I/O
H4	D0	Data I/O 0th bit (LSB)	D	I/O
J5	ROW	Row Sync Out	D	O
B2,E1,E2,G2,H1,H2,H3, J2	GNDIO	I/O Ground	P	GND
J3	DSTR	Data Strobe Clock	D	I
H8	OE_N	Output Enable	D	I
J7	WE_N	Write Enable	D	I
J8,H9,H10	GNDD	Digital Ground	P	GND
G9	SCLK	System Clock	D	I
F9,F10,G10	VDDD	Digital Power	P	PWR
J9	RESET	Sensor Reset/Initialization	D	I
A7	GPIO	General-purpose I/O pin. Primarily used for testing	D/A	I/O
E10	VCM	Common-mode Voltage Capacitor	A	O
D10	VREFM	Lower A/D Ref. Voltage Capacitor	A	O

Notes:
1. NC = No Connect.
2. The sensor is seen from the top (glass-lid) side in this view.
3. P = Power/Ground
   D = Digital
   A = Analog
4. PWR = Power Supply
   GND = Ground
   I/O = Bidirectional Input/Output
   I = Input
   O = Output

Table 1. IM103 Pin Assignments(continued)

Pin	Name	Function	Class[3]	Type[4]
B8,C9,C10	GNDA	Analog Ground	P	GND
B10	VREFP	Positive A/D Ref. Voltage Capacitor	A	O
A8,A9,B9	VDDA	Analog Power	P	PWR

The major pin groups are described below:

Digital I/O (D0-D7): These eight pins are bidirectional, tri-stateable digital I/O pins. The state of the pins is determined by WE and OE. In output mode, the eight pins are used to send image data out of the sensor to the system; in input mode, the eight pins are used to receive programming data for the on-chip registers.

Write Enable and Output Enable (WE and OE): These two pins control the digital I/O pins. They determine whether the I/O pins are in programming, output, or high-impedance (tri-state) mode. *Table 2* presents the I/O state as a function of WE and OE settings.

Table 2. Data I/O Table

WE	OE	Data I/O State
HIGH	HIGH	Tri-state
LOW	HIGH	Input (write) enabled
HIGH	LOW	Output (data out) enabled
LOW	LOW	Undefined

Note: To minimize temporal noise the use of tri-state mode should be avoided during active operation of the image sensor. Either (a) active driving of the data bus or (b) use of pull-ups to define a known logic level is recommended during active operation. Tri-state mode can be used when the image sensor is in standby.

RESET: This pin is used to initialize the sensor. It is normally HIGH during operation, and should be brought LOW for at least 100 µs to initialize the sensor and set the default register values.

The RESET signal also may be used as a chip enable. When RESET is LOW, the image sensor goes into sleep mode. Standby power in this situation is <0.5 mW. The sensor is brought out of sleep mode by setting RESET to HIGH.

Data Strobe (DSTR) and System Clock (SCLK): These two clocks control the sensor. DSTR is used primarily to clock data out of the data shift registers. SCLK controls the row, frame, column circuit, and data conversion timings, as well as the program registers. The clocks can be asynchronous, but DSTR frequency must be at least 15X SCLK for 8-bit output format, and at least 22X SCLK for 12-bit output format. Clocking is described in more detail in section 5.

Row Synchronization (ROW): This digital output pin provides a signal that goes HIGH at the end of each row readout. The signal goes LOW at the start of the next row.

GPIO: This pin is used primarily for test purposes during manufacturing. The pin can also be enabled with certain register settings to acquire data for noise correction. If the pin is not being used for noise correction, the recommended configuration is to tie it to ground through a 1-Mohm resistor.

Analog Reference Pins (VREFM, VREFP, VCM): These pins are used to connect bypass capacitors for the three voltage references: negative reference (VREFM), positive reference (VREFP), and analog common-mode (VCM). The recommended bypass circuit is shown in *Figure 3*.

The 3 analog references should be bypassed with at least 0.1-µF ceramic capacitors. Cypress recommends the use of 0402-sized chip capacitors placed as close as possible to the package and sharing GNDA as the common node.

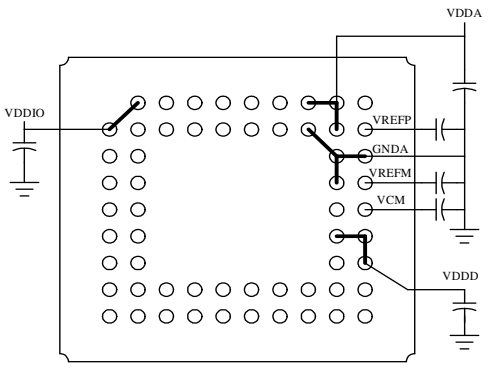


Figure 3. Bypass capacitor circuit for VREFM, VREFP, VCM, VDDIO and VDDA. Recommended bypass capacitor value is 0.1 µF.

Supply pins (VDDD, VDDIO, VDDA): These three pins separately supply power for digital circuitry (VDDD), I/O (VDDIO), and analog circuitry (VDDA). The supplies are run on separate busses on the chip but are connected through ESD blocking diodes. Because of the ESD protection diodes, the three voltages should be kept at the same value.

Grounds (GNDD, GNDIO, GNDA): These three pins separately supply grounds for digital circuitry (GNDD), I/O (GNDIO), and analog circuitry (GNDA). The grounds run separately in metal, but are tied together through the silicon substrate in the circuit.

3 Imager Array Description

Die photograph: A photograph of the IM103 die is shown in *Figure 4*. Major features of interest include:

- Row control circuitry (to the left of the array as shown).
- Column amplifiers/correlated double sample circuits and analog-to-digital converters, arranged above and below the image sensor array.
- Data registers (arranged above/below the analog-to-digital converters).

Image Array "Frame": A schematic representation of the array is shown in *Figure 5*.

Row drivers: As noted above, the row circuitry is located on the left side of the array. This circuitry controls various row-related signals (including the reset signal, the row select signal, and the hard/soft reset signal). Timing for the row drivers is controlled by SCLK.

Column circuitry/ADCs: The column amplifiers/CDS circuits and analog-to-digital converters are located above and below the sensor array. Each column has its own amplifier/CDS circuit, while each ADC is shared between two columns. Timing for column sampling and analog-to-digital conversion is controlled by SCLK.

The location of the column amplifiers and ADCs alternates between the top and bottom of the array, according to which pair of columns is being read out. Columns 0, 1, 4, 5, …, 4n, 4n+1 use amplifiers and ADCs at the bottom of the array, while columns 2, 3, 6, 7, …, 4n+2, 4n+3 use amplifiers and ADCs at the top of the array.

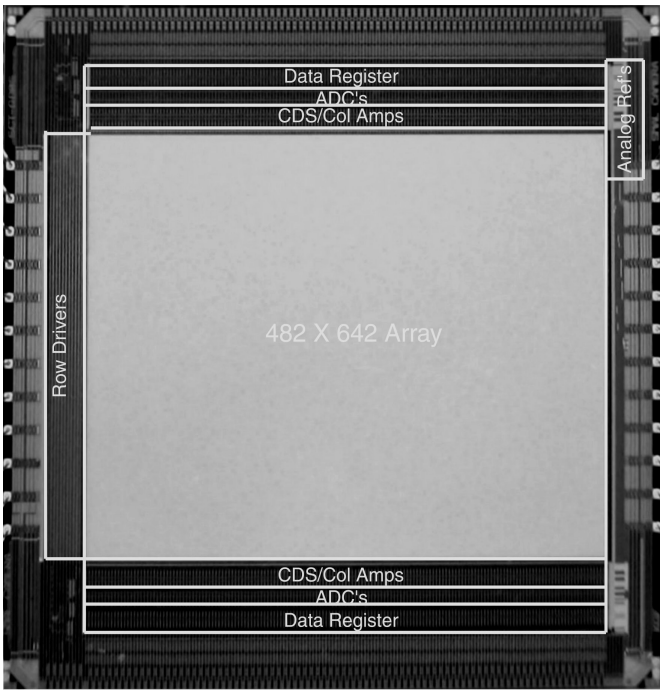


Figure 4. IM103 Die Photograph Showing the Physical Location of Major Functional Blocks

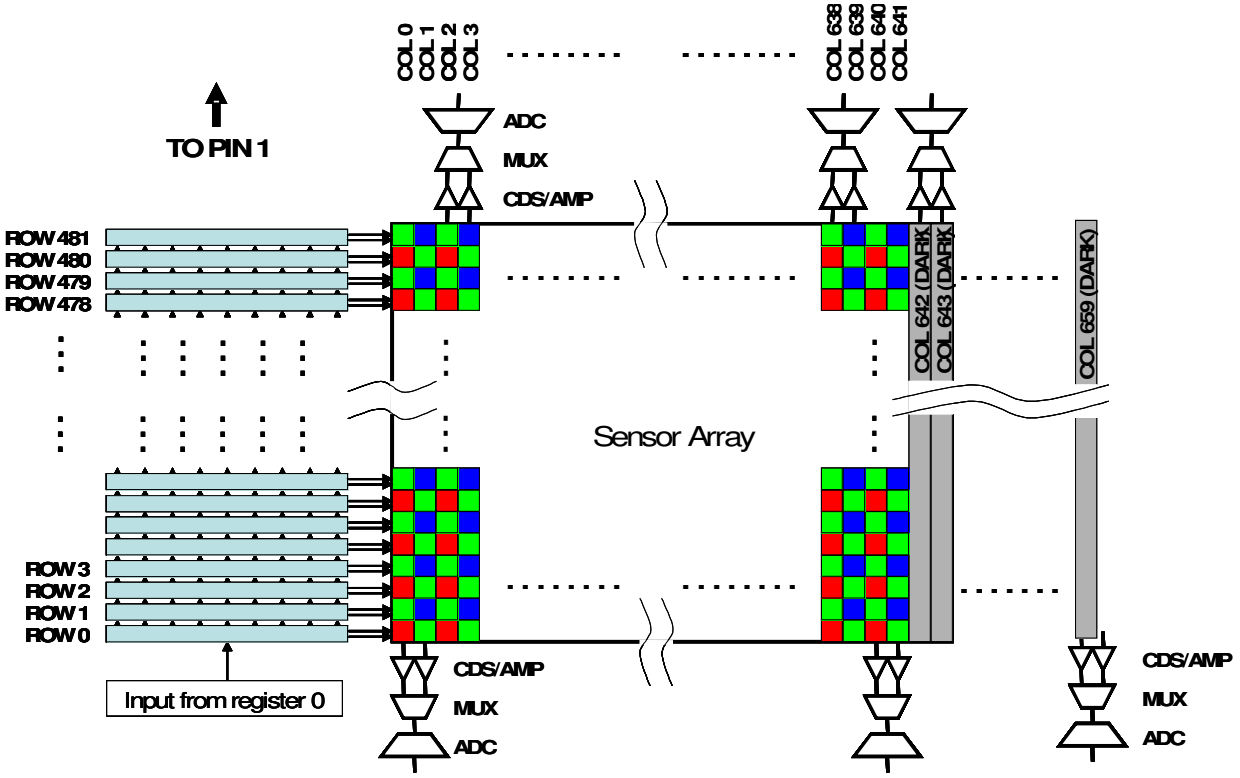


Figure 5. Imager Frame, showing the row control shift register (to the left) and the column amplifiers/MUXes/ADCs (top and bottom)

Data registers: Each ADC is followed by a 24-bit-deep data register which is read in serially. Data from the even columns (0, 2, 4 …) is read in first from MSB to LSB, followed by data from the odd columns, again from MSB to LSB (*Figure 6*). The read-in timing is derived from SCLK.

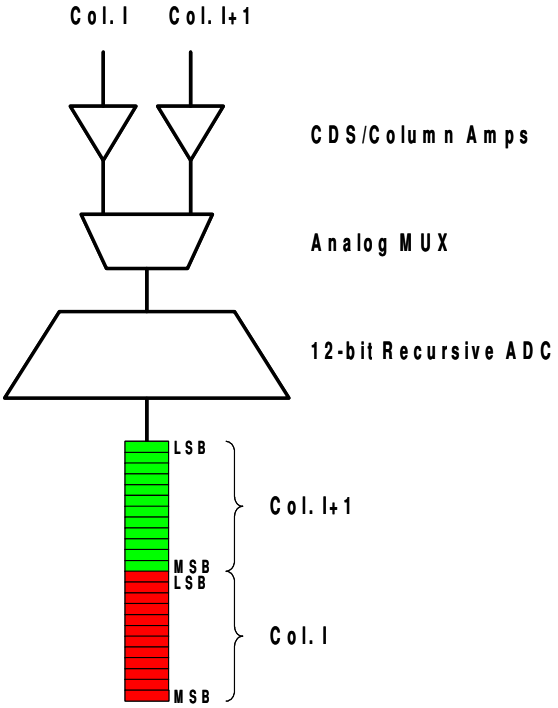


Figure 6. Data Read-in Sequence for the Data Register

Data are shifted out in parallel and then interleaved at the end of the register array to properly sequence odd and even column data from the top and bottom of the array. Data readout timing is controlled by DSTR.

Image Array: The image array (*Figure 7*) contains 482 optically active (light-sensitive) rows and 642 optically-active columns. In addition, 2 “dark” columns are provided on one side of the array.

The array is addressed as shown in *Figure 7*. When package pin 1 is above the array, the dark columns are to the right of the array. Row addressing starts at the bottom of the array, and columns are read out from left to right.

Using this arrangement, the first pixel to be read out during an exposure is at the bottom left of the array, while the last pixel to be read is at the top right.

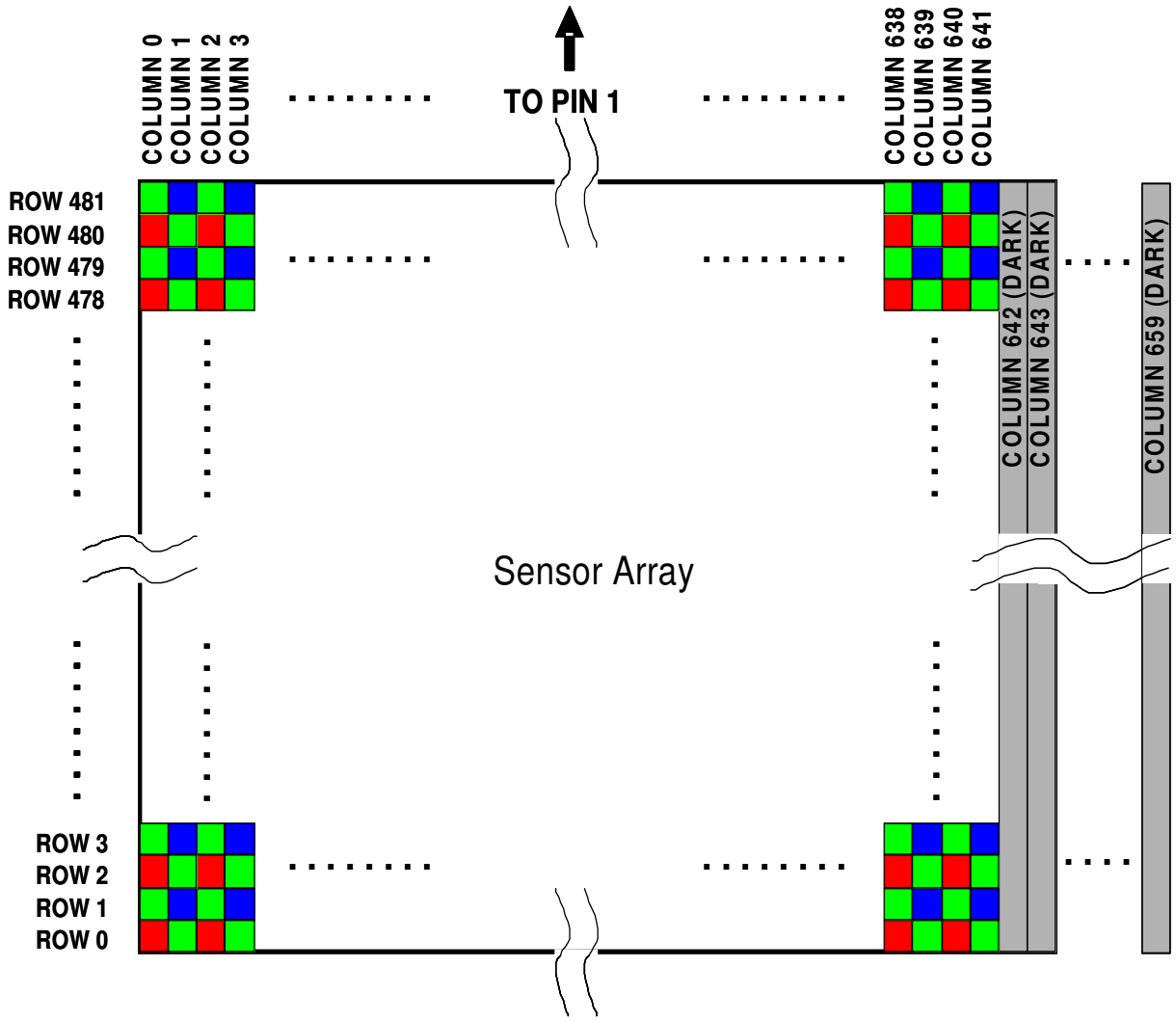


Figure 7. Image Sensor pixel array layout and color filter arrangement on pixel array. The first pixel to be read is a RED pixel. Package pin 1 is to the top, and the Data I/O pins are to the left in this drawing.

NOTE: In a camera application, package pin 1 would be oriented toward the top of the subject, to account for the inverting nature of the optics.

4 Pixel Description and Operation

Pixel Design: The IM103 uses a three-transistor pixel built around an n-well photodiode (*Figure 8*). The pixel is connected by 2 power lines, 2 control lines, and an output line.

The pixel has two operational sections: (1) a sensing section consisting of the reset MOS gate and the n-well photodiode, and (2) a readout section consisting of an MOS source-follower transistor and a row select gate.

The potential of the n-well photodiode can be controlled by applying appropriate signals to the reset MOS gate and the reset Vdd line. These signals are used to reset the photodiode potential to a reference value for the start of integration, and also for wide-dynamic-range operation.

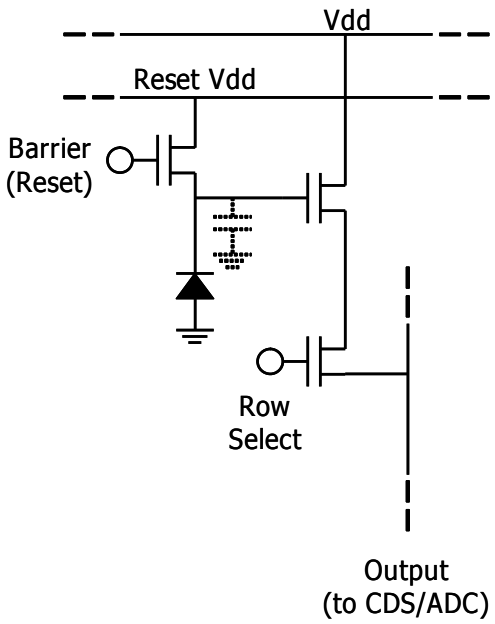


Figure 8. Three-transistor Pixel Design used in the IM103 Sensor Array

The source-follower gate provides a buffer between the relatively small capacitance associated with the photodiode node and the much larger capacitance on the column line. Row Select is used to connect all pixel source followers on a given row to the column line for readout.

Pixel Operation in Linear Mode: Pixel operation in linear mode consists of the following steps:

- The pixel is reset by applying Vdd to the reset gate. This operation brings the photodiode potential to a value near Vdd.
- After reset, photons entering the silicon are converted to photoelectrons and collected on the positively charged photodiode node. As electrons accumulate on the photodiode, the potential of the photodiode relaxes towards ground.
- After a predetermined period (the “integration time”, T_{int}), Row Select is pulsed high and the output transferred onto the column line and sampled by the column amplifier. Row Select is then brought low.
- The pixel is reset, Row Select is pulsed high a second time, and the reset level transferred onto the column line and sampled by the column amplifier. This second readout (a “correlated double sample” or CDS) generates a self-referenced differential signal that eliminates several systematic errors due to device and layout mismatches.

The number of photoelectrons collected by the photodiode is proportional to the intensity of the light hitting the pixel. The well capacitance varies slowly with potential, so that the output voltage change is approximately linear with respect to the number of electrons collected on the photodiode.

A sketch of the time dependence of the pixel voltage is shown for several illumination levels in *Figure 9*. The corresponding output signals are also shown.

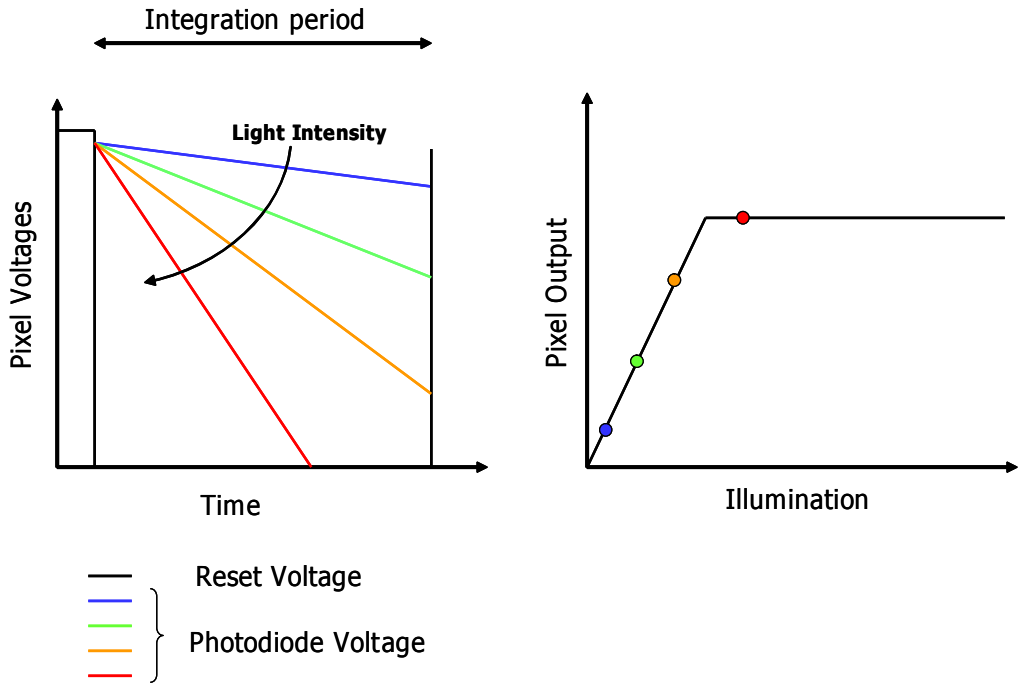


Figure 9. Left: Sketch of photodiode pixel voltage vs. time showing how different light intensities affect this parameter. Right: Sketch of the corresponding sensor ADC output vs illumination. The response is linear with an eventual saturation.

Pixel Operation in Wide-dynamic-range Mode: The pixel response can be made nonlinear by applying Cypress's proprietary variable height multiple reset method (Autobrite®).

The row control circuitry provides 8 variable reset levels (b0 through b7), where b0 is Vdda = reset level, b7 is ground, and b1 through b6 are intermediate levels. Pixel response characteristics can be modified by changing the variable reset voltages and their timing.

More details on implementing wide-dynamic-range operation can be obtained by contacting Cypress.

5 Interfacing to the IM103

Clock Requirements: The imager requires a steady system clock (SCLK) signal. SCLK sets the row rate, which in turn determines the frame rate. *Figure 10* illustrates the relationship between DSTR and SCLK.

There are 48 SCLK periods per row, as shown in *Figure 11*. For 60-fps operation, the circuit requires SCLK to be approximately 1.5 MHz. SCLK is not required to have a 50% duty ratio. The pulse width may be very small compared to the clock period, but the minimum pulse width is 20 ns.

Row Synchronization: The only output from the image sensor besides the data bus is the ROW signal. The ROW signal stays HIGH for one SCLK period during a row time. When ROW goes HIGH, the system must stop reading data from the sensor. The period when ROW is HIGH is a good time to write data to the image sensor program registers (*Figure 14*).

When ROW falls, the most recently converted row of pixels may be read out of the row buffers by the system. The system may read out the data at any rate as long as readout is finished before the next ROW pulse (*Figure 12*). More restrictive data readout conditions that reduce temporal row noise are described below.

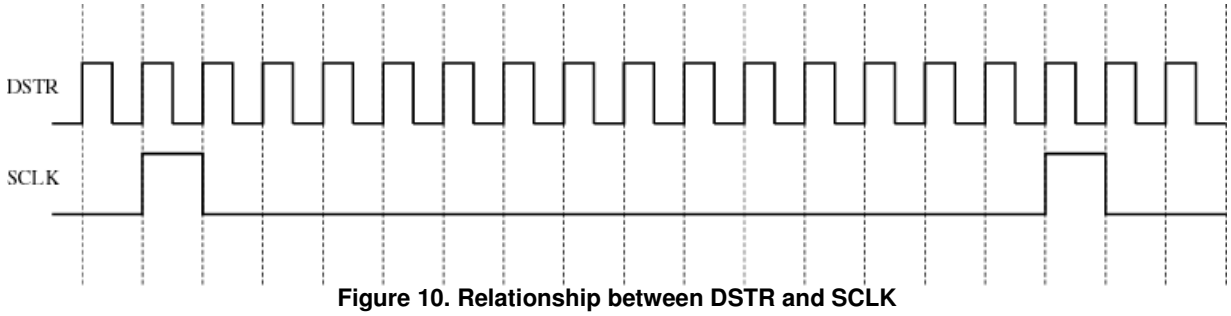


Figure 10. Relationship between DSTR and SCLK

NOTE: The relationship between DSTR and SCLK depends on output-data format. For 12-bit format, f_{DSTR} must be at least 22 X f_{SCLK}. For 8-bit format, f_{DSTR} must be at least 15 X f_{SCLK}, as shown.

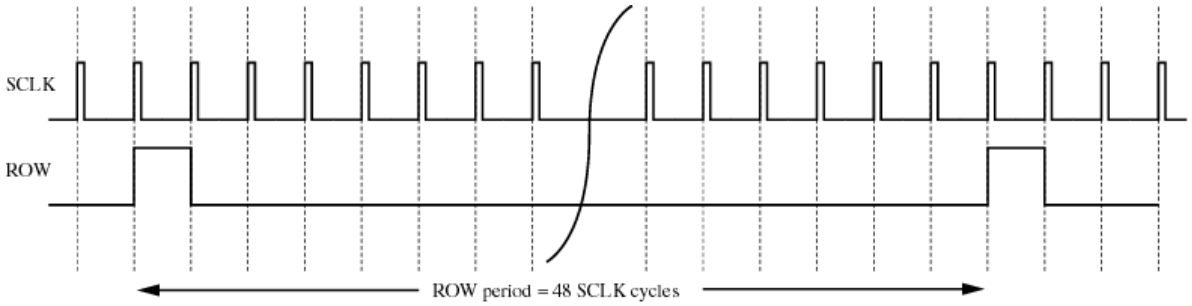


Figure 11. Row Timing Diagram

There are 48 SCLK cycles in each row period.

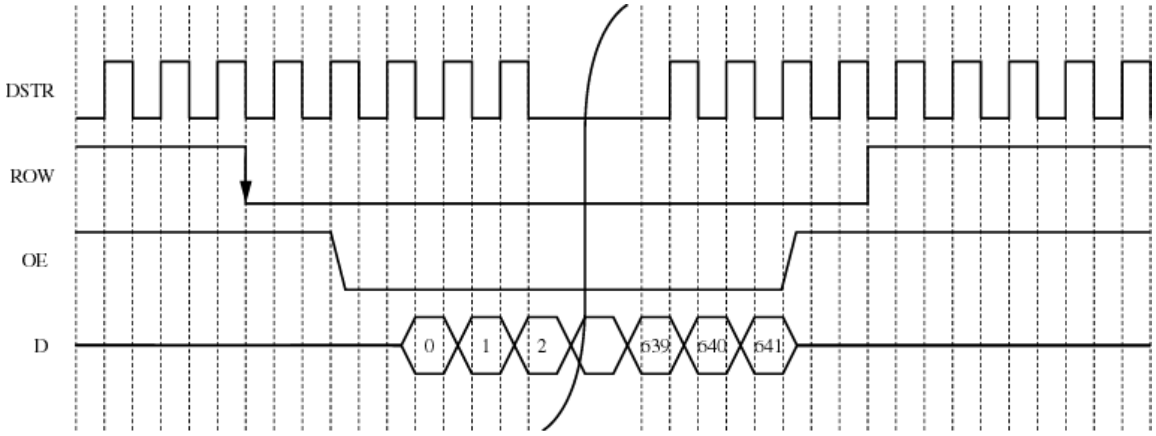


Figure 12. Data Readout Timing

Data is read out while ROW is low and OE is low. Data is ready for readout after the falling edge of ROW. All data must be read out before the rising edge of the next ROW signal. One 8-bit word is read out per DSTR clock cycle. 12-bit/pixel data format requires 3 DSTR clock cycles to read 2 pixels, while 8-bit/pixel data format requires 1 DSTR clock cycle/pixel.

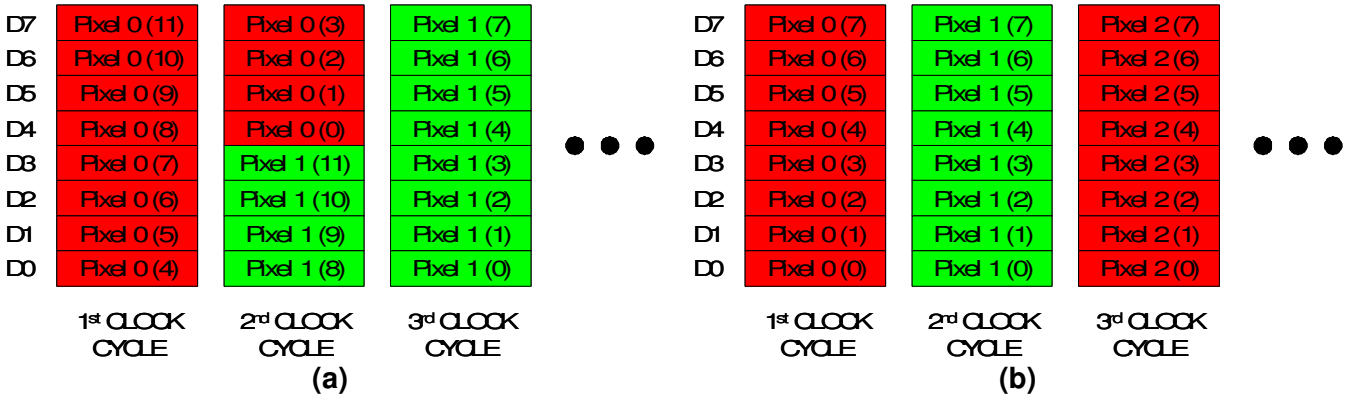


Figure 13. Data Output Format Sequence for (a) 12-bit and (b) 8-bit output-format modes

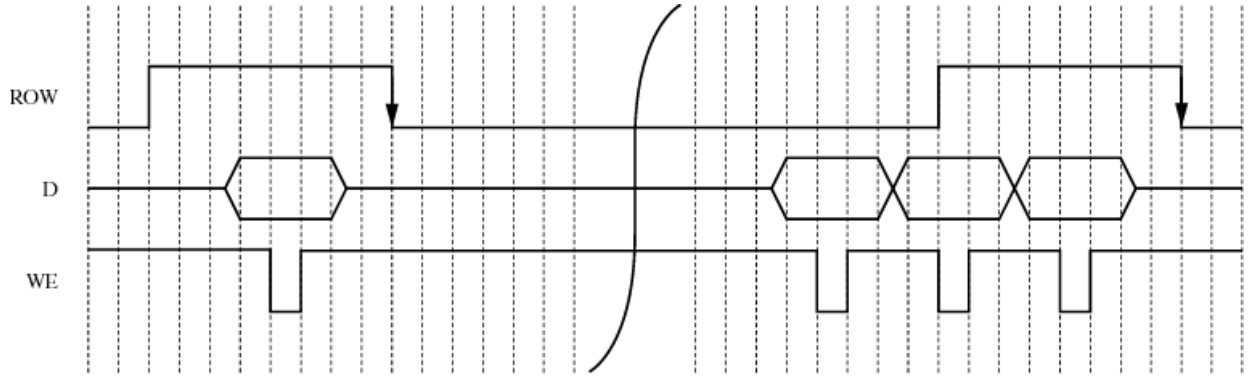


Figure 14. Timing for Writing Data to the On-board Registers through the Data Bus.

Data may be written to the sensor at any time. Data is updated to the registers on the falling edge of ROW.

Data Readout: Data can be read out in different ways. DSTR is used to clock out the data, and it can be a constant clock signal or a strobe. If DSTR is a constant clock, the data is advanced only when OE is brought LOW. If the strobe approach is used, OE should be brought LOW first and then the system can strobe the data. When OE is brought HIGH, other devices like SRAM or FLASH may be active on the bus. OE should be synchronous to DSTR if the continuous clock method is used.

The format of the data is raster. The first valid byte of a row occurs after the rising edge of DSTR. The data output format (12-bit or 8-bit, as set by the user) significantly affects the data stream, as follows (*Figure 13*):

In 12-bit data format mode, pixel data are separated and streamed as 8-bit words. Therefore, 3 cycles of DSTR are required to read out 2 pixels. In 12-bit mode, the first clock cycle reads out the 8 most significant bits of the 1st pixel. The second clock cycle reads out the 4 least significant bits from the 1st pixel as the upper 4 bits of the output, and the 4 most significant bits of the 2nd pixel as the lower 4 bits of the output. On the 3rd cycle, the 8 least significant bits of the 2nd pixel are read out. The sequence repeats on the 4th cycle.

In 8-bit mode, the data come off the bus sequentially as complete pixel words.

Clocking conditions for low temporal noise: Twice during the row period, the image sensor samples the pixel voltage levels of the row being read out. The sensor is most sensitive to noise during these sampling periods. In particular, readout of the data buffers may introduce noise into the circuit and disturb the sensor voltage levels. Such noise usually appears as temporal row noise (i.e., random horizontal line flicker from frame to frame).

To minimize this noise, it is recommended that DSTR be gated so that data readout is avoided during the sampling periods. The sclk periods when sampling occurs are 28-29 and 45 after a row goes high (out of 48 sclk periods).

6 Programming the IM103

The IM103 image sensor has 12 on-board 4-bit programmable registers for controlling its operation. All configuration of the imager is performed over the data bus. To set power, gain, data format, or other functions, the controller/host must write the appropriate words to the program registers.

In order to write data, the data bus pins first must be set to input mode. This is accomplished by setting output enable (OE) high.

The programmable registers are updated when the write enable (WE) input signal goes low. Data on the data bus must be set up before WE is brought low and be held for a short time after WE is brought high (*Figure 14*).

The 8-bit word written to the data I/O lines contains 4 bits of address (the upper 4 bits, ADR(3)-ADR(0)) and 4 bits of program data (the lower 4 bits, P(3)-P(0)) (*Figure 15*).

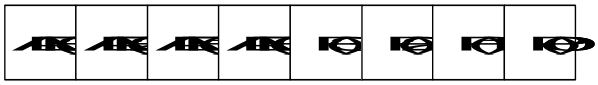


Figure 15. Configuration of the 8-bit Words used to Program the IM-103 On-board Registers

7 Register Descriptions

General descriptions of the 12 on-board registers are listed in *Table 3*. Detailed descriptions of the register bit functions are given in Tables *Table 4* through *Table 15*.

NOTE: The on-board registers are set to the default values in *Table 3* through *Table 15* after a RESET signal.

NOTE: Reserved registers should not be programmed differently from the recommended values. If a reserved register is accidentally programmed differently, the sensor should be reinitialized using the RESET signal.

Table 3.IM103 On-chip Registers

Register	Function	Default Value	Recommended Value
0	Frame start and dynamic range compression	6	-
1	Noise reduction and reset control signals	7	7 (hard reset) or 3 (soft reset)
2	Noise reduction control signals	2	A
3	Noise reduction control signals	3	F (hard reset) or E (soft reset)
4	Reset level, clamp, and test pin analog modes	8	8
5	GPIO pin modes	0	0 (active pixel) or 8 (ADC test)
6	Reverse saturation control modes	1	2
7	Data output format and gain settings	0	-
8	Power setting	2	4
9	Power management	F	D
10	Variable reset level test and control	1	0 or 8 depending on desired compression
11	Dynamic range compression control	8	0

Register 0: This register (*Table 4*) manages the start of frame and variable reset levels.

Table 4.Register 0 Description

Bit	Name	Default	Function
0	b<0>	0	LSB of pixel reset/compression control
1	b<1>	1	2nd bit of pixel reset/compression control
2	b<2>	1	MSB of pixel reset/compression control
3	rs	0	Starts frame capture (synchronous)

b<0>, b<1>, b<2>: These bits determine the variable reset magnitude. Since there are 3 of these bits, 8 different levels are possible. b<0:2> = 000 corresponds to the highest variable reset value (Vdd for reset), and b<0:2> = 111 corresponds to the lowest value (ground). Fine tuning of the voltages that correspond to the variable reset heights can be done with other registers (described below).

rs: This bit is used to start a new frame.

The system initiates a frame by writing a '1' to bit 3 with the pixel reset value in bits 0-2. The 8-bit word is therefore: 00001000 ($_x$08). When ROW (output) falls, the frame starts. Whenever a '1' is written to bit 3, a '0' must be written on the next transition of ROW. A conventional linear image capture (i.e., no dynamic range compression) is programmed by writing 00001000 ($_x$08) followed by 00000111 ($_x$07) to the program register. Autobrite® compressed images are programmed by writing additional words to register 0 after 00000111 ($_x$07). (See the examples at the end of this section for more details.)

Note: A new frame can also be started by applying a RESET signal. The difference between a register 0 frame start and a RESET frame start is that the register 0 frame start is synchronous. Use of the register 0 approach maintains a consistent integration interval from frame to frame.

Register 1: This register (*Table 5*) controls noise cancellation circuitry for pixel-reset/row-select signals and enables hard reset operation.

Table 5.Register 1 Description

Bit	Name	Default	Function
0	enfreset	1	When HIGH: Enables pixel reset signal noise reduction
1	enrdrop	1	When HIGH: Enables row select signal noise reduction
2	envdrop	1	When HIGH: Enables hard reset operation
3	reserved	0	Bit must be kept LOW

ENFRESET and ENRDROP: Bits 0 and 1 enable noise reduction circuitry essential to effective operation of the imager. Both of these bits should be set equal to 1 at all times.

ENVDROP: Bit 2 on register 1 controls how the pixels are reset. The voltage level to which a pixel settles after being reset (V_o) can vary both spatially and temporally. Some of this variability arises from pixel-to-pixel differences in transistor thresholds etc. which contributes to fixed pattern noise. There is also a random component to V_o originating ultimately from thermal noise. This noise component is commonly referred to as (*kT/C*) or reset noise.

Reset noise depends on how the reset transistor is operated. A “hard” reset occurs when this transistor is driven above threshold on pixel reset. Under these conditions it can be shown that the thermal noise associated with pixel reset is proportional to $\sqrt{kT/C}$ where *C* is the sense node capacitance, *k* is Boltzmann’s constant, and *T* is the temperature in degrees Kelvin.

A “soft” reset occurs when the reset transistor is operated in sub-threshold on pixel reset. Under these conditions the reset noise is ~$\sqrt{kT/2C}$.

Provided pixel reset noise is a considerable noise source, this discussion suggests that “soft” reset operation has significantly less noise than “hard” reset operation. In the IM103 imager, the dark temporal noise is typically ~3LSB (12-bit) in “soft” reset mode and ~4.5LSB (12-bit) in “hard” reset mode (25 fps, T=33°C, full-frame integration).

“Soft” reset mode has more image lag than “hard” reset mode. Lag occurs when the reset value of a pixel is dependent on its previous value. Because there is a limited settling time and the reset transistor is never driven above threshold, lag is more prevalent in “soft” reset mode. A trade-off between less noise or less image lag must therefore be made when deciding whether to use “soft” or “hard” reset mode.

Register 2: This register (*Table 6*) enables various noise reduction and reset modes.

Table 6.Register 2 Description

Bit	Name	Default	Function
0	reserved	0	Bit must be kept LOW.
1	reserved	1	Bit must be kept HIGH.
2	reserved	0	Bit must be kept LOW.
3	enshort	0	When HIGH: Enables circuitry to minimize column noise. sen (register 9, bit 1) should be set low when enshort is set high.

ENSHORT: Enshort enables circuitry that minimizes column line noise.

Register 3: This register (*Table 7*) enables various noise reduction and reset features.

Table 7.Register 3 Description

Bit	Name	Default	Function
0	enrdropdrop	1	When HIGH: Enables hard reset noise reduction circuitry.
1	encdsload	1	When HIGH: Reduces CDS amplifier noise.
2	reserved	0	Bit must be kept HIGH.
3	reserved	0	Bit must be kept HIGH.

ENRDROPDROP: This bit enables noise reduction circuitry used in hard reset mode. It should be set high whenever the imager is operated in hard reset mode, and low in soft reset mode.

ENCDSLOAD This register reduces noise in the column circuit prior to the ADCs. Typically, 1dB of noise reduction will occur in low light illumination when this bit is set high.

Register 4: This register (*Table 8*) controls the GPIO pin output and enables a feature that minimizes reverse saturation of the pixel signals.

Table 8. Register 4 Description

Bit	Name	Default	Function
0	a<0>	0	Hard reset level bit OR analog test selection bit 0 (see text)
1	a<1>	0	Hard reset level bit OR analog test selection bit 1 (see text)
2	a<2>	0	Hard reset level bit OR analog test selection bit 2 (see text)
3	enclamp	1	When HIGH: Enables circuitry that minimizes “reverse” saturation effects.

a<0>, a<1>, a<2>: These registers are used for two separate functions. When aten (register 5, bit 0) = 0 and envdrop = 1, a<0:2> select how far above threshold the reset transistor is driven during hard reset. For this function the recommended setting is a<0:2> = 000.

When aten (register 5, bit 0) is high, a<0:2> selects analog voltages for test purposes.

ENCLAMP: This register enables circuitry that prevents “reverse saturation” of pixel signals under high illumination. This register should be set high during normal imager operation.

Register 5: This register (*Table 9*) controls the GPIO pin output and enables ADC test mode.

Table 9.Register 5 Description

Bit	Name	Default	Function
0	aten	0	When HIGH: Enables analog voltage test output on GPIO pin.
1	reserved	0	Bit must be kept LOW.
2	reserved	0	Bit must be kept LOW.
3	vten	0	When HIGH: Enables voltage input on GPIO pin for testing ADC and CDS circuits. Also very useful in minimizing column fixed pattern noise.

ATEN: This register enables the GPIO pin for analog output.

VTEN: ADC test mode is enabled by setting vten = 1. In this mode a voltage signal can be sent to the CDS/ADC block through the GPIO pin. Column fixed pattern noise arising from mismatches between the ADCs can be corrected by operating the imager in this mode, saving the resulting column means, and subsequently correcting image data.

Register 6: This register (*Table 10*) is currently not in use. Bits on this register should not be changed from their default settings.

Table 10.Register 6 Description

Bit	Name	Default	Function
0	reserved	0	Clamp Level Control
1	reserved	0	Clamp Level Control
2	reserved	1	Clamp Level Control
3	reserved	0	Clamp Level Control

Register 7: This register (*Table 11*) controls the data format (12 bit or 8 bit) and gain (for 8-bit format only).

Table 11.Register 7 Description

Bit	Name	Default	Function
0	g(0)	0	Gain bit 0
1	g(1)	0	Gain bit 1
2	g(2)	0	Gain bit 2
3	fmode	0	When HIGH: Output is in 12-bit mode. When LOW: Output is in 8-bit mode and gain is enabled.

FMODE: When fmode (bit 3) is HIGH, data is output from the sensor at 12 bits/pixel. When fmode is LOW, data is output at 8 bits/pixel, and digital gain is enabled.

g<0>, g<1>, and g<2>: Gain can be set from 1X to 16X in powers of 2. The gain is given by:

$$GAIN = 2^G$$

where G is the 3-bit number determined from register 7, bits 0-2. The maximum gain is 16X, or G = 100. Valid settings for G are 000, 001, 010, 011, and 100, for GAIN = 1, 2, 4, 8, and 16X, respectively.

Register 8: This register (*Table 12*) controls the analog power on the sensor by setting the analog currents.

Table 12.Register 8 Description

Bit	Name	Default	Function
0	p(0)	0	LSB of power setting.
1	p(1)	1	2nd bit of power setting.
2	p(2)	0	3rd bit of power setting.
3	p(3)	0	MSB of power setting.

p<0>, p<1>, p<2>: The analog current is related to the register 8 setting by the following (approximate) relation:

Analog Current = 0.5 mA + (CurrSet)*1.25 mA

where CurrSet is the 4-bit number programmed into register 8. The minimum analog current is approximately 0.5 mA, at ($_x$80). The maximum analog current is approximately 19.25 mA, at ($_x$8F). A minimum power setting of 4 (p<0:3> = 100) is recommended.

NOTE: Although analog power dissipation is a major component of total power dissipation, other factors such as frame rate influence the total device power dissipation.

Register 9: This register (*Table 13*) controls the state of various internal analog current sources.

Table 13.Register 9 Description

Bit	Name	Default	Function
0	bgen	1	When HIGH: Bandgap reference current source is enabled. When LOW, bandgap reference is disabled (imager will not function)
1	sen	1	When HIGH, column source-follower current source is enabled. When LOW, column source-follower current source is disabled.
2	adcen	1	When HIGH, analog/digital converter is enabled. When LOW, analog/digital converter is disabled (imager will not function).
3	cdsen	1	When HIGH, column amplifier is enabled. When LOW, column amplifier is disabled (imager will not function).

BGEN, ADCEN, AND CDSEN: These bits enable various analog current source circuits that are essential to the operation of the imager. They should only be disabled to conserve power when the imager is in stand-by mode.

SEN: Column line current sources are activated when sen = 1. When enshort = 1, sen should be set LOW

Register 10: This register (*Table 14*) is used for test purposes and control of variable reset voltage levels.

Table 14.Register 10 Description

Bit	Name	Default	Function
0	reserved	1	reserved
1	reserved	0	reserved
2	reserved	0	reserved
3	b1sel	0	Shifts variable reset voltage levels

B1SEL This bit changes the voltage level of variable reset levels 1-6. Enabling b1sel reduces the overall amount of compression in Autobrite mode.

Register 11: This register (*Table 15*) controls dynamic range compression when digital gain is used.

Table 15.Register 11 Description

Bit	Name	Default	Function
0	squ<0>	0	LSB for manual gain compensation.
1	squ<1>	0	2nd bit for manual gain compensation.
2	squ<2>	0	MSB for manual gain compensation.
3	autosquash	1	When HIGH: Enables automatic gain compensation. When LOW: Enables manual gain compensation.

squ<0>, squ<1>, squ<2>: These bits adjust the variable reset levels to compensate for any gain that is applied when operating in 8-bit mode (fmode=0). When the gain is 2X or greater, pixels will saturate an 8-bit scale at lower illumination levels than 1X gain mode. This in turn will progressively make the least compressive variable reset levels ineffective. To

compensate for this effect, the variable reset levels can be shifted by enabling these bits. To perform this procedure manually, the autosquash bit must be set to 0.

Note: Setting squ<0:2> to values higher than 100 will produce variable reset levels equivalent to squ<0:2> = 100.

AUTOSQUASH: When this bit is set to 0 the variable reset levels can be adjusted manually with squ<2:0>. When it is set to 1 the variable reset levels are adjusted by the gain settings on register 7, g<0:2>.

8 Example: Programming the IM103 for Linear-mode Image Capture

The following example describes how to program the IM103 to capture images in the conventional linear mode. In this mode pixel output is linearly proportional to input illumination; no on-chip dynamic range compression is used.

There are 482 active rows in the sensor. Once a frame has started, at least 482 ROW signals must pass before a new frame is started. A convenient approach is to let the frame contain 512 (2^9) ROW signals. Such a frame will contain 30 blank rows. These 30 extra row times can be used as a vertical blanking period or as a time to calculate the next exposure and process data.

When capturing an image, the controller should keep track of the row count. At row count 0, the start of frame instruction is written to the sensor. This is done by writing $_x$08 over the data bus. At row count 1, the controller must write a new value to address $_x$0 to turn off the frame start signal. This can be done by writing $_x$07 or another value depending on the exposure time. When ready to integrate, the controller writes $_x$00 to the sensor followed by $_x$07.

The integration (or exposure) time is determined by the number of row periods remaining in the frame after the integration signal is written (see *Figure 16*):

$$T_{int} = ((Rows - IntStart)/Rows) * 1/FrameRate$$

where:

Rows = total rows in frame (including virtual rows).

IntStart = the number of rows that pass before writing the integration word to the sensor.

FrameRate = sclk/(Rows)/48.

To set exposure, the system controller determines the appropriate exposure time and tells the imager to start integrating at IntStart.

For example, if a shutter speed equal to half of the frame rate is desired, the following sequence of words would be written to the sensor:

Table 16.Example Programming for Shutter Speed Equal to ½ Frame Rate

Rowcount	Databus
0	$_x$08
1	$_x$07
255	$_x$00
256	$_x$07
0 (next frame)	$_x$08

The following tables give additional examples of exposure control:

Table 17.Example Programming for Shutter Speed Equal to 511/512 Frame Rate

Rowcount	Databus	Note
0	$_x$08	
1	$_x$07	511/512 frametime
0 (next frame)	$_x$08	

Table 18.Example Programming for Shutter Speed Equal to 384/512 Frame Rate

Rowcount	Databus	Note
0	$_x$08	
1	$_x$07	
128	$_x$00	384/512 frametime
129	$_x$07	
0 (next frame)	$_x$08	

Table 19.Example Programming for Shutter Speed Equal to 1/512 Frame Rate

Rowcount	Databus	Note
0	$_x$08	
1	$_x$07	
510	$_x$00	1/512 frametime
511	$_x$07	
0 (next frame)	$_x$08	

When exposure is set to full integration and more brightness is required, gain may be used in 8-bit mode (by setting register 7). The system controller would then need to control both gain and integration.

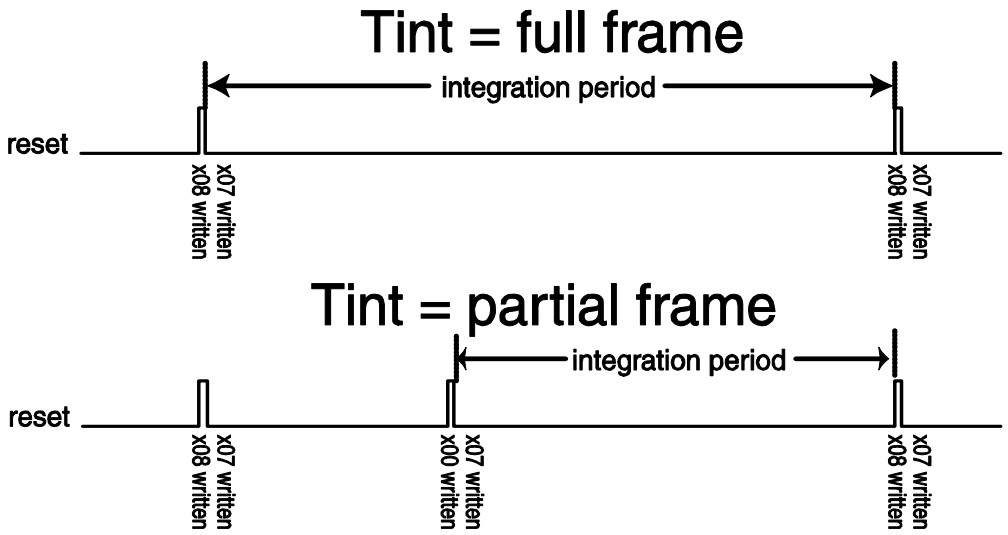
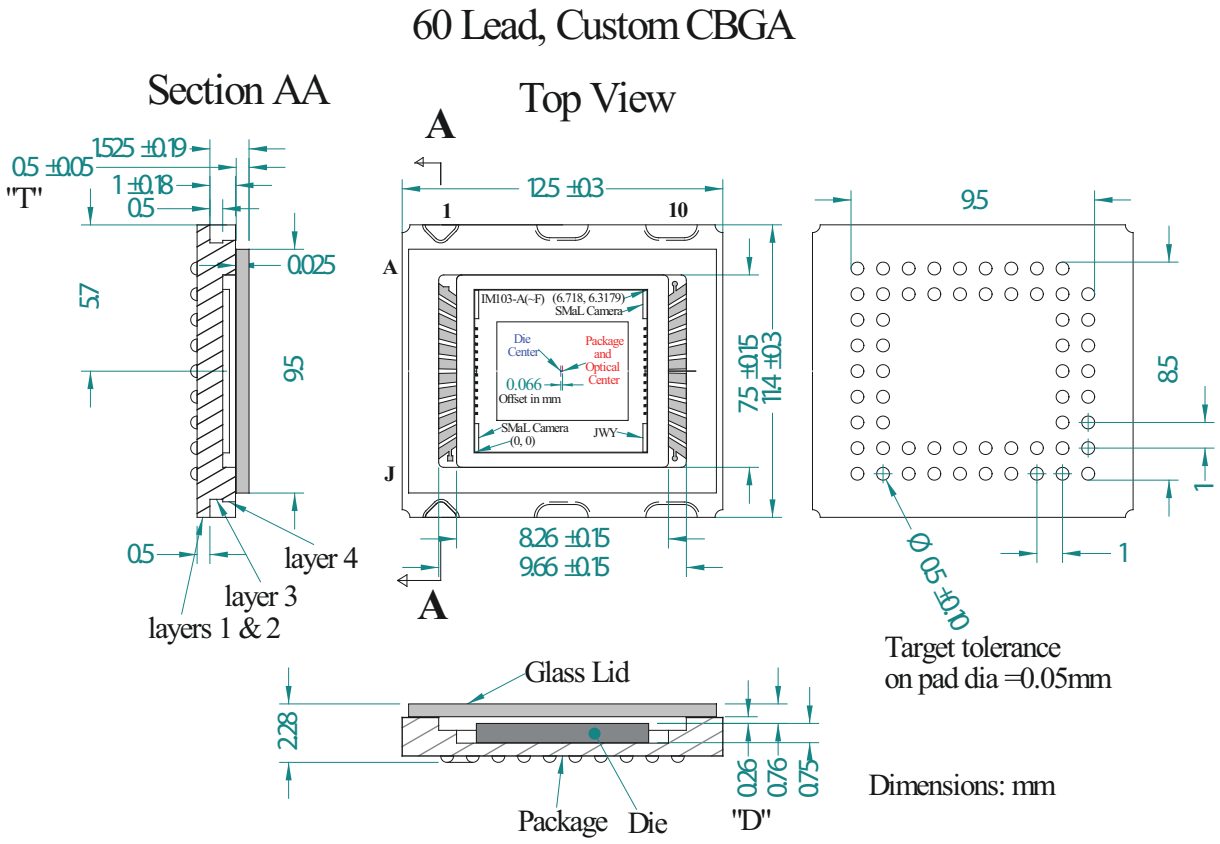


Figure 16. Timing of Program Register Instructions for Linear-response Mode

The sensor is initially programmed to $_{x}$08 at RowCount = 0 (setting start of frame). At RowCount = 1 (next ROW pulse), $_{x}$07 is written to the sensor. At RowCount = n (equivalent to IntStart in the text) integration is initiated by writing $_{x}$00 followed by $_{x}$07 at RowCount = n+1. The sequence repeats at the start of the next frame.

9 Schematic of the Package

The schematic of the package of the imager is as shown below.



10 Optical Window

Question: What is the thickness (T) of the optical window?

Answer: The optical window thickness (T) is 0.5mm thick.

Question: What is the distance (D) between the upper surface of the die and lower (internal) surface of the optical window?

Answer: The distance (D) between the upper surface of the die and the lower (internal) surface of the optical window is 0.26 mm and this includes a 0.03 mm bond line.

Question: Depending on the former dimensions (if T+D>0.4_0.5 mm): would it be possible to have the imager without the optical window in our development phase (and in more general during the production phase)?

Answer: a) Total distance between the image plane (top of sensor) and the top of the glass is 0.76 mm.

b) No.

i) The window provides two critical functions

1. Protects the optical path from particles that will be imaged

2. Protects the wire bonds

c. Option is provide die in wafer form

Question: What are the recommendations to handle the image without the optical window

Answer: Standard practise for packaging image sensors is to singulate the wafer and immediately package the sensors into a package or camera module within a class 100 or better clean room. Extreme care and appropriate processing is required to “seal” the optical path within 0.5mm of the image plane so that particle does not create dark defects in the image.

Question: Could the imager qualification be compromised from the optical removal window?

Answer: a. Yes, Silicon sensor reliability in the field depends on how it is packaged. Cypress has not qualified an open package for the reasons stated above. The options are:

i. Buy the sensor in a qualified package.

ii. Buy sensor in die from (generally wafer) in which case the customer receives qualified silicon but customer must manage the reliability of the sensor in their package or system

Document History Page

Document Title: 1/3” VGA-Format CMOS Image Sensor Document Number: 001-11358				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	503768	See ECN	QGS	New Datasheet