CY28354-400

210 MHz 24 Output Buffer for 4-DDR DIMMS for VIA Chipsets Support

Features

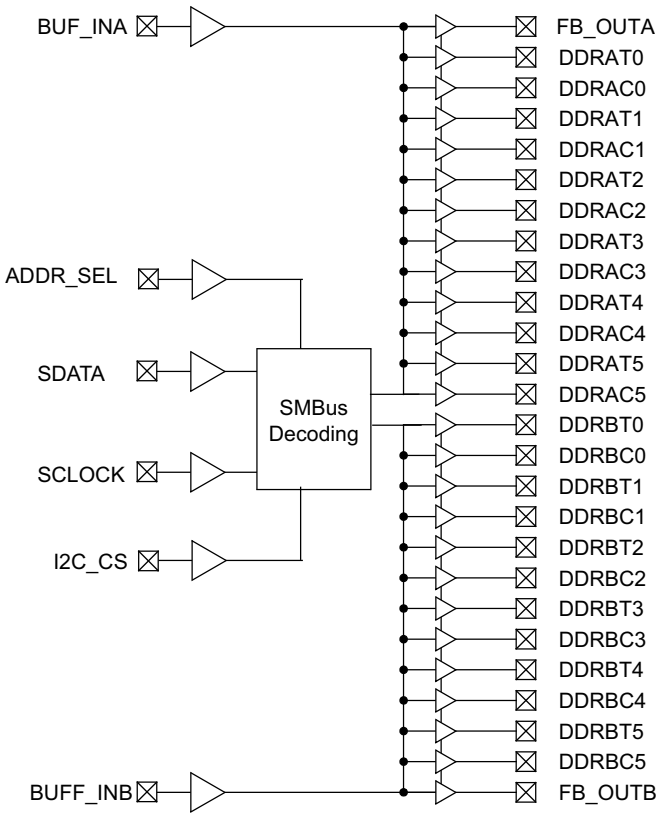
- **Supports VIA PRO 266, KT266 and P4x266**
- **Dual 1- to 12-output buffer/driver**
- **Supports up to four DDR DIMMs**
- **Low-skew outputs (< 75 ps)**
- **Supports 266-MHz, 333-MHz and 400-MHz DDR SDRAM**
- **SMBus Read and Write support**
- **Space-saving 48-pin SSOP package**

Functional Description

The CY28354-400 is a 2.5V buffer designed to distribute high-speed clocks in PC applications. The part has 24 outputs to support four unbuffered DDR DIMMS. The CY28354-400 can be used in conjunction with CY28326 similar clock synthesizer for the PTT880 and KTT880 chipsets.

The CY28354-400 also includes an SMBus interface which can enable or disable each output clock. On power-up, all output clocks are enabled.

Block Diagram



Pin Configuration

SSOP
Top View

VDD2.5	1	48	VDD2.5
GND	2	47	GND
FB_OUTB	3	46	ADDR_SEL
BUFF_INB	4	45	I2C_CS
DDRBT0	5	44	DDRBT2
DDRBC0	6	43	DDRBC2
DDRBT1	7	42	DDRBT3
DDRBC1	8	41	DDRBC3
GND	9	40	GND
VDD2.5	10	39	VDD2.5
DDRAT0	11	38	DDRAT4
DDRAC0	12	37	DDRAC4
DDRAT1	13	36	DDRAT5
DDRAC1	14	35	DDRAC5
GND	15	34	GND
VDD2.5	16	33	VDD2.5
FB_OUTA	17	32	DDRBT4
BUF_INA	18	31	DDRBC4
DDRAT2	19	30	DDRBT5
DDRAC2	20	29	DDRBC5
DDRAT3	21	28	VDD2.5
DDRAC3	22	27	GND
VDD2.5	23	26	SDATA
GND	24	25	SCLK

2200 Laurelwood Road, Santa Clara, CA 95054 Tel:(408) 855-0555 Fax:(408) 855-0550 www.SpectraLinear.com

Pin Description

Pin	Name	PWR	I/O	Description
11, 13, 19, 21, 38, 36, 5, 7, 44, 42, 32, 30	DDRA[0:5]T DDRB[0:5]T	VDD2.5	O	**Clock outputs**. These outputs provide copies of BUF_INA and BUF_INB, respectively.
12, 14, 20, 22, 37, 35, 6, 8, 43, 41, 31, 29	DDRA[0:5]C DDRB[0:5]C	VDD2.5	O	**Clock outputs**. These outputs provide complementary copies of BUF_INA and BUF_INB, respectively.
18, 4	BUF_INA, BUF_INB	VDD2.5	I PD	**Reference input from chipset**. 2.5V input. Internal pull-down
17, 3	FB_OUTA FB_OUTB	VDD2.5	O	**Feedback clock for chipset**.
45	I2C_CS	VDD2.5	I PD	**CS for I2C allows for multiple devices to be connected with the same I2C address**. Internal pull-down. See *Table 1*.
46	ADDR_SEL	VDD2.5	I PD	**Selects I2C Address D2/DC**. Internal Pull-down
25	SCLK	VDD2.5	I PU	**SMBus clock input**. Internal Pull-up
26	SDATA	VDD2.5	I/O PU	**SMBus data input**. Internal Pull-up
1, 10, 16, 23, 28, 33, 39, 48	VDD2.5			**2.5V voltage supply**
2, 9, 15, 24, 27, 34, 40, 47	GND			**Ground**

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions such as individual clock output buffers, etc., can be individually enabled or disabled. The registers associated with the Serial Data Interface initializes to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts Byte Write, Byte Read, Block Write, and Block Read operation from the controller. For Block Write/Read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For Byte Write and Byte Read operations, the system controller can access individual indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 1*. The Block Write and Block Read protocol is outlined in *Table 2*.The slave receiver address is D2/DC depending on the state of the ADDRSEL pin.

Table 1. Command Code Definition

Bit	Description
7	0 = Block Read or Block Write operation 1 = Byte Read or Byte Write operation
(6:5)	01 to address chip when I2C_CS = 0 10 to address chip when I2C_CS = 1
(4:0)	Byte offset for Byte Read or Byte Write operation. For Block Read or Block Write operations, these bits should be '00000'

Table 2. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address – 7 bits	2:8	Slave address – 7 bits
9	Write = 0	9	Write = 0
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code – 8 bits '00000000' stands for block operation	11:18	Command Code – 8 bits '00000000' stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count from master – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29:36	Data byte 0 from master – 8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 1 from master – 8 bits	30:37	Byte count from slave – 8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data bytes from master/Acknowledge	39:46	Data byte 0 from slave – 8 bits
....	Data Byte N – 8 bits	47	Acknowledge
....	Acknowledge from slave	48:55	Data byte 1 from slave – 8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave/Acknowledge
		....	Data byte N from slave – 8 bits
		....	Not Acknowledge
		....	Stop

Serial Configuration Map

- The Serial bits will be read by the clock driver in the following order.

  Byte 0 – Bits 7, 6, 5, 4, 3, 2, 1, 0
  Byte 1 – Bits 7, 6, 5, 4, 3, 2, 1, 0
  Byte N – Bits 7, 6, 5, 4, 3, 2, 1, 0

- Reserved and unused bits should be programmed to “0”
- SMBus Address for the CY28354 is as follows.

	A6	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**R/W**
SEL ADDR = 1	1	1	0	1	0	0	1	—
SEL ADDR = 0	1	1	0	1	1	1	0	—

Byte 22: Outputs Active/Inactive Register (1 = Active, 0 = Inactive), Default (Hi-z) = Active

Bit	@Pup	Pin #	Description
Bit 7	0		Input Threshold Control 00: Normal (1.25V) 01: 1.20V 10: 1.15V 11: 1.10V
Bit 6	0		
Bit 5	0	17	FBOUTA Control, 0 = Enable, 1 = Disable
Bit 4	0	3	FBOUTB Control, 0 = Enable, 1 = Disable
Bit 3	1	30, 29	DDRBT5, DDRBC5
Bit 2	1	32, 31	DDRBT4, DDRBC4
Bit 1	1	42, 41	DDRBT3, DDRBC3
Bit 0	1	44, 43	DDRBT2, DDRBC2

Byte 23: Outputs Active/Inactive Register (1 = Active, 0 = Inactive), Default = Active

Bit	@Pup	Pin #	Description
Bit 7	1	7, 8	DDRBT1, DDRBC1
Bit 6	1	5, 6	DDRBT0, DDRBC0
Bit 5	1	36, 35	DDRAT5, DDRAC5
Bit 4	1	38, 37	DDRAT4, DDRAC4
Bit 3	1	21, 22	DDRAT3, DDRAC3
Bit 2	1	19, 20	DDRAT2, DDRAC2
Bit 1	1	13, 14	DDRAT1, DDRAC1
Bit 0	1	11, 12	DDRAT0, DDRAC0

Absolute Maximum Conditions[1]

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage to Ground Potential	–0.5	4.6	V
V_{in}	DC Input Voltage (except BUFF_IN)	–0.3	V_{DD}+0.3	V
V_{out}	Output Voltage	1.1	V_{DD}–0.4	V
T_s	Temperature, Storage	–65	+150	°C
T_a	Temperature, Operating Ambient	0	85	°C
$Ø_{JC}$	Dissipation, Junction to Case (Mil-Spec 883E Method 1012.1)	36.39		°C/W
$Ø_{JA}$	Dissipation, Junction to Ambient (JEDEC (JESD 51)	77.99		°C/W
ESD_h	ESD Protection (Human Body Model)	–	2000	V

DC Electrical Specifications

Parameter	Description	Min.	Typ.	Max.	Unit
$V_{DD2.5}$	Supply Voltage	2.3	–	2.7	V
C_{OUT}	Output Capacitance	–	6	–	pF
C_{IN}	Input Capacitance	–	5	–	pF

AC Electrical Specifications

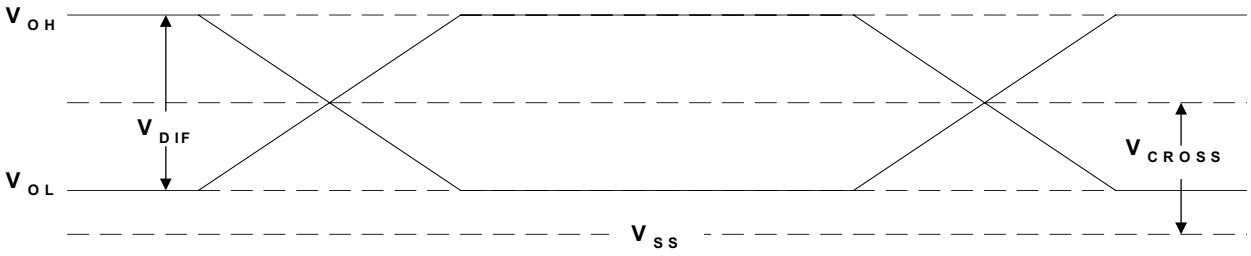
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input LOW Voltage	For all pins except SMBus	0.3	–	0.7	V
V_{IH}	Input HIGH Voltage		1.7	–	V_{DD} + 0.3	V
I_{OH}	Output HIGH Current	V_{DD} = 2.375V, V_{OUT} = 1V	–	–	–12	mA
I_{OL}	Output LOW Current	V_{DD} = 2.375V, V_{OUT} = 1.2V	–	–	12	mA
V_{OL}	Output LOW Voltage[2]	I_{OL} = 12 mA, V_{DD} = 2.375V	–	–	0.5	V
V_{OH}	Output HIGH Voltage[2]	I_{OH} = –12 mA, V_{DD} = 2.375V	1.7	–	–	V
I_{DD}	Supply Current[2]	Unloaded outputs, 133 MHz	–	–	400	mA
I_{DD}	Supply Current	Loaded outputs, 133 MHz	–	–	500	mA
I_{DDPD}	Supply Current	All outputs off	–	–	2	mA
V_{OUT}	Output Voltage Swing	See Test Circuity. See *Figure 1*	0.7	–	V_{DD} + 0.6	V
V_{OC}	Output Crossing Voltage		V_{DD}/2–0.3	V_{DD}/2	V_{DD}/2+0.3	V
IN_{DC}	Input Clock Duty Cycle		40	–	60	%

Switching Characteristics[3]

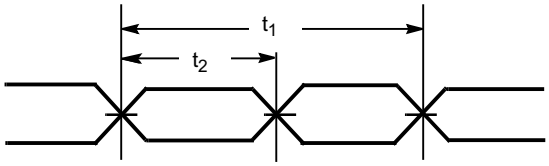
Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
–	Operating Frequency		60		210	MHz
–	Duty Cycle[2, 4] = $t_2 \div t_1$	Measured differentially at V_{CROSS}	IN_{DC} –2%	–	IN_{DC} +2%	%
t_{3d}	DDR Rising Edge Rate[2]	Measured single ended at 20% to 80% of V_{DIF}	1.0	2.0	5.0	V/ns
t_{4d}	DDR Falling Edge Rate[2]	Measured single ended at 80% to 20% of V_{DIF}	1.0	2.0	5.0	V/ns
t_5	Output to Output Skew for DDR[2]	All outputs equally loaded. See *Figure 1*.	–	–	75	ps
t_6	Input to Output Propagation delay	At output load of 15 pFn	–	–	6	ns

Notes:
1. Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.
3. All parameters specified with loaded outputs.
4. Duty cycle of input clock is 50%. Rising and falling edge rate is greater than 1 V/ns.

Switching Waveforms



Duty Cycle Timing



Output-Output Skew

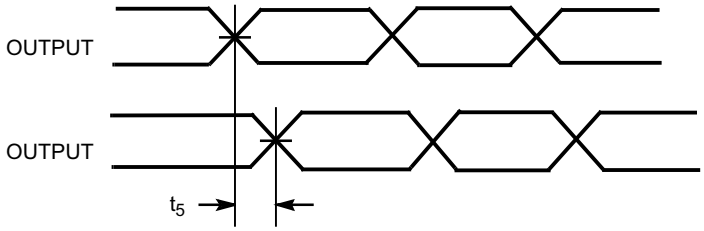


Figure 1 shows the differential clock directly terminated by a 120Ω resistor.

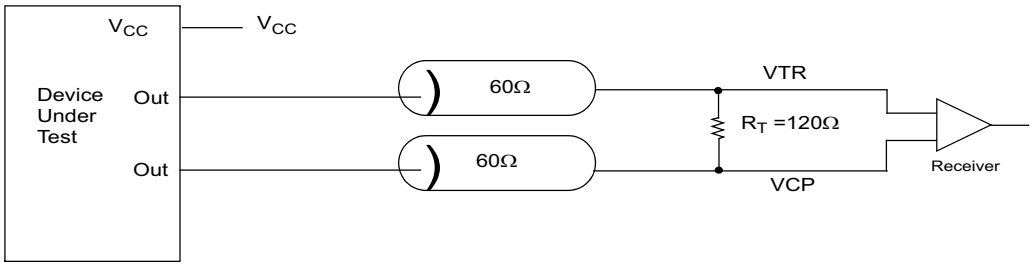
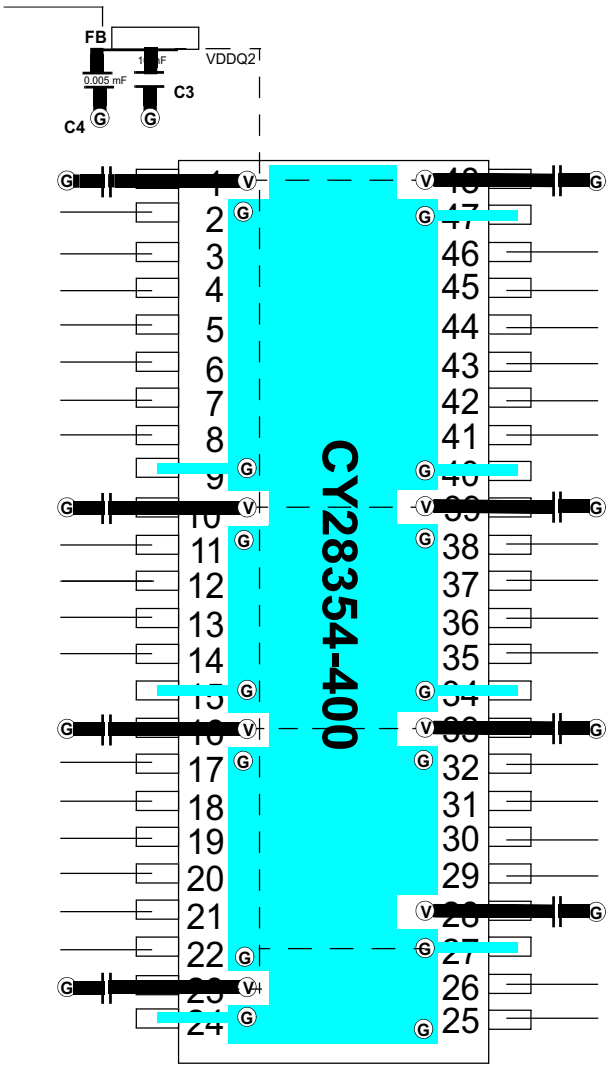


Figure 1. Differential Signal Using Direct Termination Resistor

Layout Example for DDR 2.5V



FB = Dale ILB1206 - 300 (300Ω @ 100 MHz) or TDK ACB 2012L-120
Ceramic Caps C3 = 10–22 µF C4 = 0.005 µF

Ⓖ = VIA to GND plane layer Ⓥ =VIA to respective supply plane layer

Note: Each supply plane or strip should have a **ferrite bead and capacitors**
All bypass caps = 0.1 µF ceramic

Ordering Information

Ordering Code	Package Type	Operating Range
Lead Free		
CY28354OXC–400	48-pin SSOP	Commercial, 0°C to 85 °C
CY28354OXC–400T	48-pin SSOP – Tape and Reel	Commercial, 0°C to 85 °C

Package Drawing and Dimension

48-Lead Shrunk Small Outline Package O48