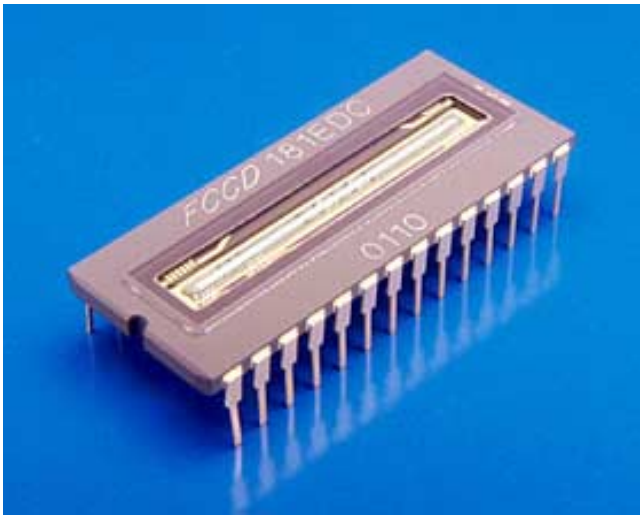
CCD 181
Variable-Element High-Speed Linear Image Sensor

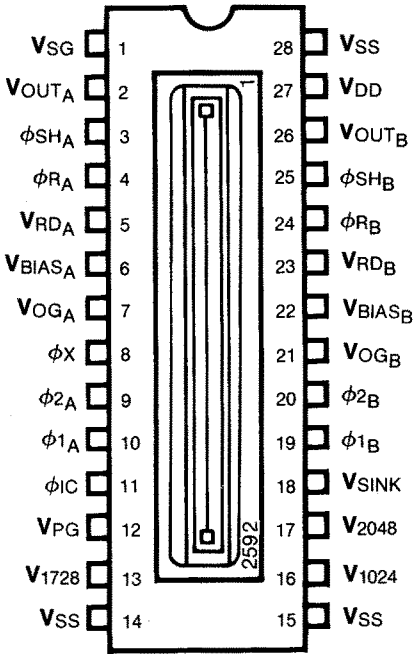
FEATURES

- 2592 x 1 photosite array
- 10 µm x 10µm photosites on 10µm pitch
- Anti-blooming and integration control
- Voltage-selectable array lengths:
  - 2592 Elements
  - 2048 elements
  - 1728 elements
  - 1024 elements
- Enhanced spectral response (particularly in the blue region)
- Excellent low-light-level performance
- Low dark signal
- High responsivity
- High speed operation
- Dynamic range typical: 7500:1
- Over 1 V peak-to-peak outputs
- Dark references contained in sampled-and-held outputs
- Special selection available - consult factory



PIN NAME	DESCRIPTION
V_{SG}	Amplifier Signal Ground
V_{OUT_A}	Output Amplifier A Source
ϕSH_A	Sample and Hold Gate A
ϕR_A	Reset Gate A
V_{RD_A}	Reset Drain A
V_{BIAS_A}	Output Amplifier A Bias
V_{OG_A}	Output Gate A
ϕX	Transfer Clock
$\phi 2_A$, $\phi 2_B$	Transport Clocks
$\phi 1_A$, $\phi 1_B$	Transport Clocks
ϕIC	Integration Control Clock
V_{PG}	Photogate
V_{1728}	1728 Active Pixels Switch
V_{SS}	Substrate Ground
V_{1024}	1024 Active Pixels Switch
V_{2048}	2048 Active Pixels Switch
V_{SINK}	Anti-Blooming Sink
V_{OG_B}	Output Gate B
V_{BIAS_B}	Amplifier B Bias
V_{RD_B}	Output Amplifier B Bias
ϕR_B	Reset Gate B
ϕSH_B	Sample and Hold Gate B
V_{OUT_B}	Output Amplifier B Source
V_{DD}	Output Amplifier Drain

PIN CONNECTION DIAGRAM
(TOP VIEW)



Fairchild Imaging, Inc., 1801 McCarthy Blvd., Milpitas, CA 95035 • (800)325-6975 • (408) 433-2500

GENERAL DESCRIPTION

The CCD181 is a 2592-element line image sensor designed for industrial measurement, telecine, and document scanning applications which require high resolution, high sensitivity and high data rate. Incorporation of on-chip anti-blooming and integration controls allow the CCD181 to be extremely useful in an industrial measurement and control environment or in environments where lighting conditions are difficult to control.

The CCD181 is equipped with special gates which allow the user to select 4 effective array lengths:

2592 elements: 300-lines/inch across 8.5 inch wide document
2048 elements: 240-lines/inch across 8.5 inch wide document
1728 elements: 200-lines/inch across 8.5 inch wide document
1024 elements: 120-lines/inch across 8.5 inch wide document

The CCD181 is a third generation device having an overall improved performance compared with first and second generation devices, including enhanced blue response and excellent low light level performance, and high-speed operation up to 20 MHz.

The photoelement size is 10µm (0.39 mils) x 10µm (0.39 mils) on 10µm (0.39 mils) centers. The device is manufactured using Fairchild Imaging's advanced charge-coupled device n-channel isoplanar buried-channel technology.

FUNCTIONAL DESCRIPTION

The CCD191 consists of the following functional elements illustrated in the Block Diagram and Circuit Diagram (see Fig. 1A).

Photosites — A row of 2592 image sensor elements separated by a diffused channel stop and covered by a silicon dioxide surface passivation layer. Image photons pass through the transparent silicon creating hole-electron pairs. The photon generated electrons are accumulated in the photosites. The amount of charge accumulated in each photosite is a linear function of the incident illumination intensity and the integration period. The output signal will vary in an analog manner from a thermally generated background level at zero illumination to a maximum at saturation under bright illumination.

Two Transfer Gate — Gate structures adjacent to the row of image sensor elements. The charge packets accumulated in the photosites are transferred in parallel via the transfer gates (ϕX) to the transport shift registers whenever the transfer gate voltages go high. Alternate charge packets are transferred to the A and B transport registers.

Two Analog Shift Registers — The transport shift registers are used to move the light generated charge packets delivered by the transfer gates. ($\phi 1A$, $\phi 1B$, $\phi 2A$, $\phi 2B$) serially to the charge detector/amplifier. The complementary phase relationship of the last elements of the two transport registers provides for alternate delivery of charge packets at the output amplifiers.

A Gated Charge Detector/Amplifier — Charge packets are transported to a precharge capacitor whose potential changes linearly in response to the quantity of the signal charge delivered. This potential is applied to the input gate of the two-stage NMOS amplifiers producing a signal at the output "V_{OUT}" pin. Before each charge packet is sensed, a reset clock (ϕRA, ϕRB) recharges the input node capacitor to a fixed voltage (V_{RDA}, V_{RDB})

Integration and Anti-Blooming Controls — In many applications the dynamic range in parts of the image is larger than the dynamic range of the CCD, which may cause more electrons to be generated in the photosite area than can be stored in the CCD shift register. This is particularly common in industrial inspection and satellite applications. The excess electrons generated by bright illumination tend to "bloom" or "spill over" to neighboring pixels along the shift register, thus "smearing" the information. This smearing can be eliminated using two methods:

Anti-Blooming Operation:

A DC voltage applied to the integration control gate (approximately 5 to 7 volts) will cause excess charge generated in the photosites to be diverted to the anti-blooming sink (V_{SINK}) instead of to the shift registers. This acts as a "clipping circuit" for the CCD output. (see Fig. 2)

Fig 1A BLOCK DIAGRAM

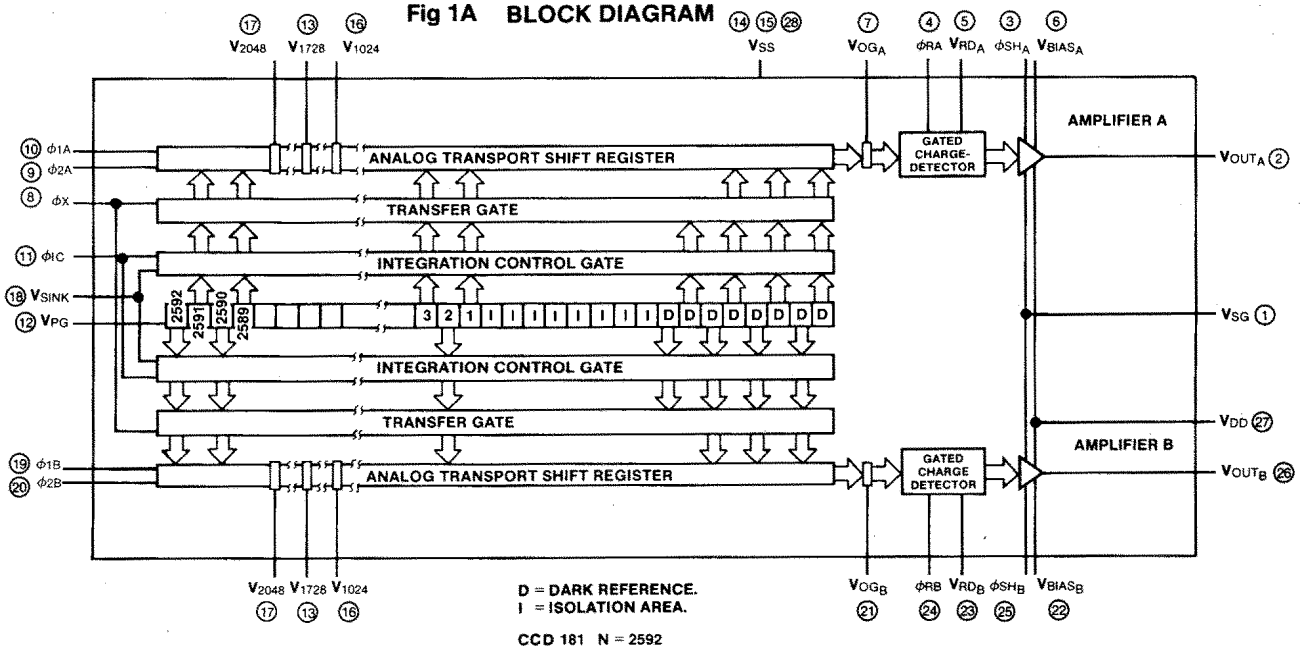


Fig. 1B CIRCUIT DIAGRAM NEAR PIXEL #1024

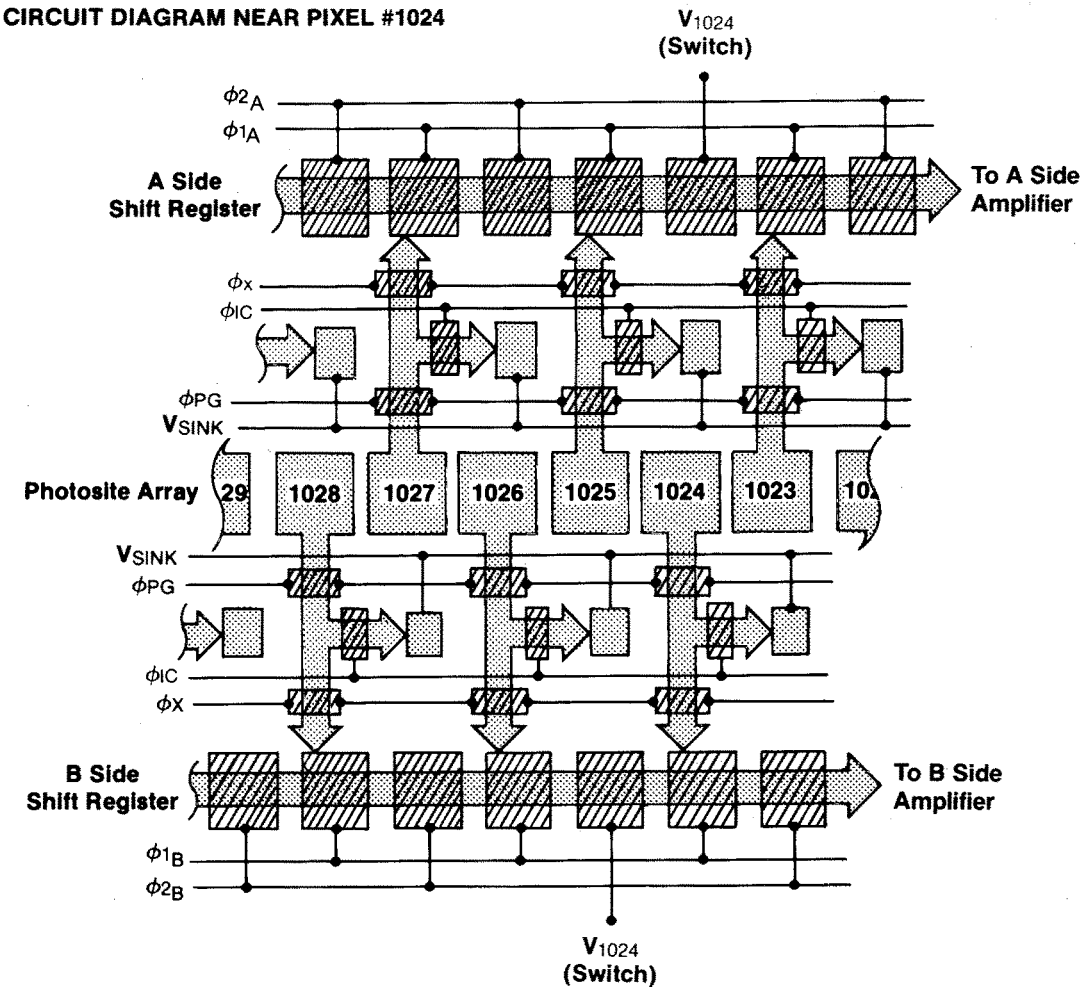
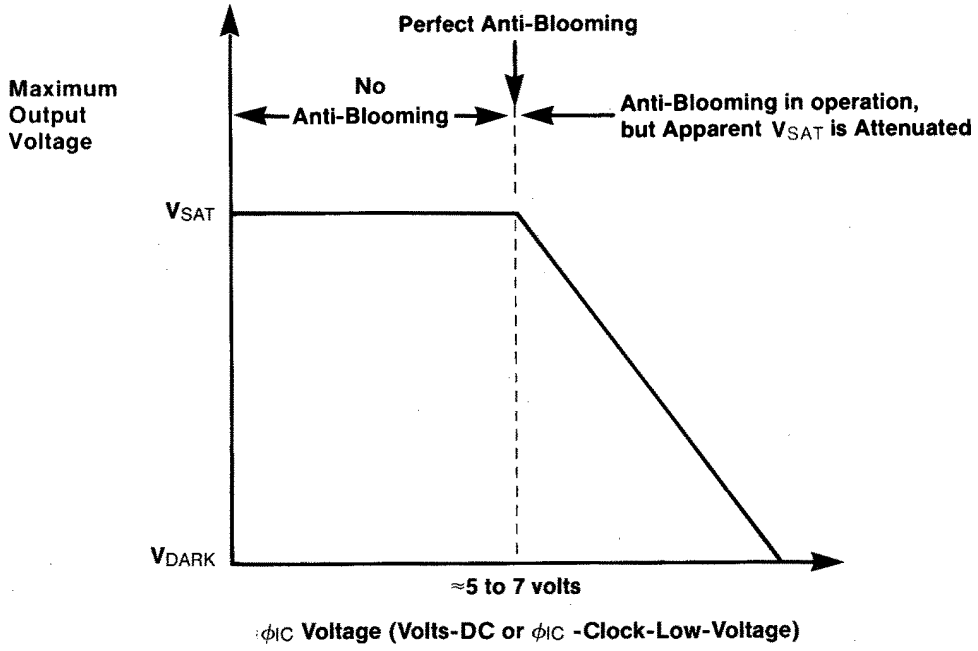
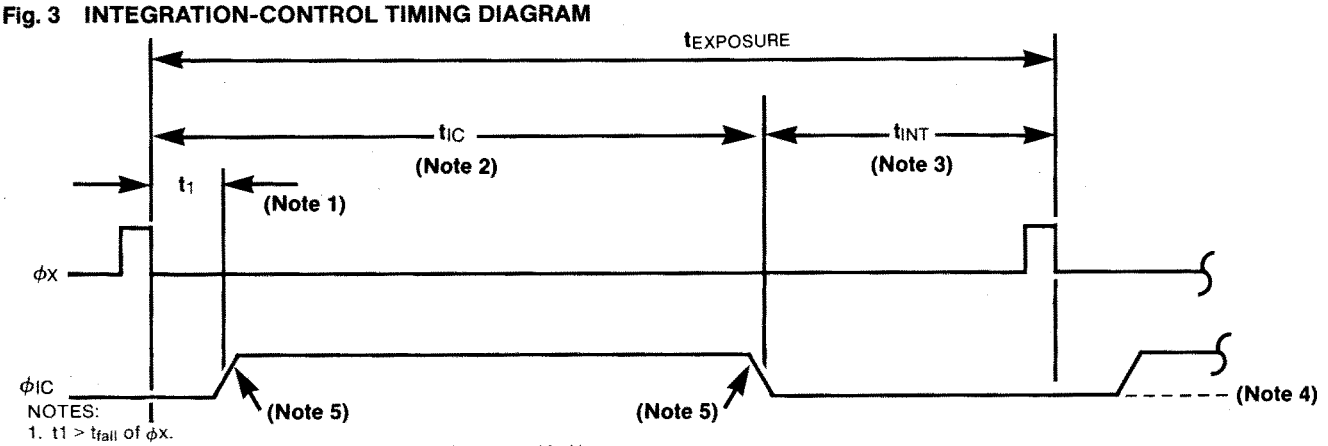


Fig. 2 MAXIMUM OUTPUT VOLTAGE vs. ϕ_{IC} Voltage



Fairchild Imaging, Inc., 1801 McCarthy Blvd., Milpitas, CA 95035 • (800)325-6975 • (408) 433-2500

Fig. 3 INTEGRATION-CONTROL TIMING DIAGRAM



NOTES:
1. t1 > t_{fall} of φx.
2. All charge generated in photosites during t_{IC} is dumped in V_{SINK}.
3. All charge generated in photosites < Q_{SAT} during t_{INT} is transferred into the shift registers during φx clock-high period. Photosite charge > Q_{SAT} generated during t_{INT} goes into V_{SINK} if anti-blooming voltage is optimized.
4. φIC clock-low ≈ 5 to 7 volts will give best anti-blooming operation.
5. φIC t_{rise} & t_{fall} > 4 μs to minimize clock coupling of φIC into V_{OUT}.
6. To eliminate integration control, but retain anti-blooming φIC ≈ +5 VDC.
7. To eliminate both integration control and anti-blooming, φIC = 0VDC or V_{SS}(−2V).
8. To use integration control without anti-blooming, use φIC clock-low = 0.0 to 0.7 volts and φIC clock-high = same range as φ1 clock-high voltage.

Integration Control Operation:

Variable integration times which are less than the CCD exposure time may be attained by supplying a clock to the integration control gate. Clocking φIC reduces the integration time from tEXPOSURE to tINT (Fig. 3). This reduces the photosite signal in all photosites by the ratio EXPOSURE to tINT. Greater than 10:1 reduction in average photosite signal can be achieved with integration control.

The integration-control and anti-blooming features can be implemented simultaneously. This is done by setting the φIC, clock-low level to approximately 5 to 7 volts.

DEFINITION OF TERMS

Charge-Coupled Device — A Charge-coupled device is a semiconductor device in which finite isolated charge-packets are transported from one position in the semiconductor to an adjacent position by sequential clocking of an array of gates. The charge-packets are minority carriers with respect to the semiconductor substrate.

Sample -and Hold Clock (φSHA, φSHB) **—** The voltage waveform applied to the sample-and-hold gates in the output amplifiers to create a continuous sampled video signal at the output. The sample-and-hold feature may be defeated by connecting φSHA and φSHB to V_{DD}.

Dark Reference — Video output level generated from sensing elements covered with opaque metallization which provides a reference voltage equivalent to device operation in the dark. This permits use of external DC restoration circuitry.

Isolation Cell — This is a site on-chip producing an element in the video output that serves as a buffer between valid video data and dark reference signals. The output from an isolation cell contains no valid information and should be ignored.

Dynamic Range — The saturation exposure divided by the RMS temporal noise equivalent exposure. Dynamic range is sometimes defined in terms of peak-to-peak noise. To compare the two definitions a factor of four to six is generally appropriate in that peak-to-peak noise is approximately equal to four to six times RMS noise.

RMS Noise Equivalent Exposure — The exposure level that gives an output signal to the RMS noise level at the output in the dark.

Saturation Exposure — The minimum exposure level that will provide a saturation output signal. Exposure is equal to the light intensity times the photosites integration time.

Charge Transfer Efficiency — Percentage of valid charge information that is transferred between each successive stage of the transport registers.

Responsivity — The output signal voltage per unit exposure for a specified spectral type of radiation. Responsivity equals output voltage divided by exposure.

Total Photoresponse Non-uniformity — The difference of the response levels of the most and the least sensitive element under uniform illumination. Measurement of PRNU excludes first and last elements.

Dark Signal — The output signal in the dark caused by thermally generated electrons that is a linear function of the integration time and highly sensitive to temperature.

Saturation Output Voltage — The maximum usable signal output voltage. Charge transfer efficiency decreases sharply when the saturation output voltage is exceeded.

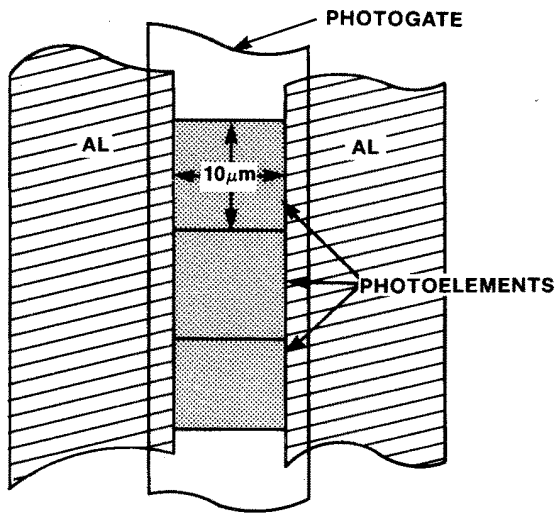
Integration Time — The time interval between the falling edge of any two successive transfer pulses (φx). The integration is the time allowed for the photosites to collect charge.

Exposure Time - The time interval between the falling edge of the two transfer pulses (φx) shown in the timing diagram. The exposure time is the time between transfers of signal charge from the photosites into the transport registers.

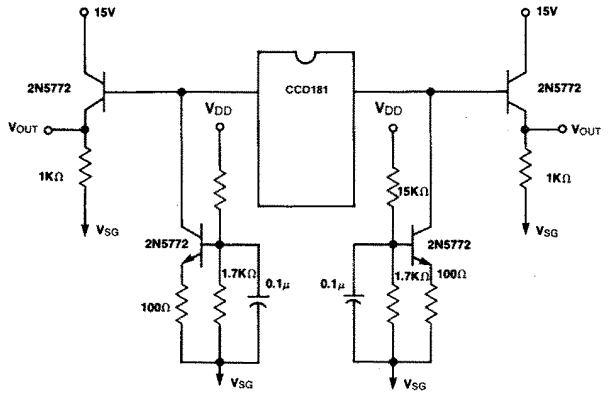
Pixel - A picture element (photosite).

Fairchild Imaging, Inc., 1801 McCarthy Blvd., Milpitas, CA 95035 • (800)325-6975 • (408) 433-2500

Fig. 4: PHOTOELEMENT DIMENSIONS



TEST LOAD CONFIGURATION



ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Storage Temperature	-25° C to +125° C
Operating Temperature	-25° C to +70° C
CCD 181: Pins 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 27	-0.3V to +18V
Pin 1	0V
Pins 14, 15, 28	-3.0V to 0V
Pins 2, 26	See Caution Note

CAUTION NOTE:
These devices have limited built-in gate protection. It is recommended that static discharge be controlled and minimized. Care must be taken to avoid shorting pins $V_{OUT_{A+B}}$ to V_{SS} or V_{DD} during operation of the devices. Shorting these pins temporarily to V_{SS} or V_{DD} may destroy the output amplifiers.

DC CHARACTERISTICS: $T_P = 25°C$ (Note 1)

SYMBOL	CHARACTERISTIC	RANGE			UNIT	CONDITION
		MIN	TYP	MAX		
V_{DD}	Output Amplifier Drain Supply Voltage	13.5	14.0	14.5	V	
$V_{RD\ (A+B)}$	Output Reset Drain Supply Voltages	13.5	14.0	14.5	V	
V_{SINK}	Anti-Blooming Sink Voltage	13.5	14.0	14.5	V	
V_{PG}	Photogate Bias Voltage	5.5	6.0	6.5	V	
$V_{OG\ (A+B)}$	Output Gate Bias Voltages	5.5	6.0	6.5	V	
$V_{BIAS\ (A+B)}$	Amplifier Bias Voltages	2.5	3.0	3.5	V	
V_{SG}	Amplifier Signal Ground	0.0	0.3	0.5	V	
V_{SS}	Substrate Ground	-3.0	-2.0	-1.0	V	Note 2
I_{DD}	Output Amplifier Drain Supply Current	6.0	10.0	15.0	mA	

Fairchild Imaging, Inc., 1801 McCarthy Blvd., Milpitas, CA 95035 • (800)325-6975 • (408) 433-2500

CLOCK CHARACTERISTICS: $T_P = 25°C$ (Note 1)

SYMBOL	CHARACTERISTIC	RANGE			UNIT	CONDITIONS
		MIN	TYP	MAX		
$V\phi X$ HIGH	Transfer Clock HIGH	11.0	11.5	12.0	V	Note 3
$V\phi 1$ HIGH (A+B) $V\phi 2$ HIGH (A+B)	Transport Clock HIGH	9.5	10.0	10.5	V	Note 3
$V\phi R$ HIGH (A+B)	Reset Clock HIGH	11.0	11.5	12.0	V	Note 3
$V\phi SH$ HIGH (A+B)	Sample/Hold Clock HIGH	11.0	11.5	12.0	V	Note 3
$V\phi 1024$ HIGH	Select 1024 Elements Clock HIGH	9.5	10.0	10.5	V	Note 3
$V\phi 1728$ HIGH	Select 1728 Elements Clock HIGH	9.5	10.0	10.5	V	Note 3
$V\phi 2048$ HIGH	Select 2048 Elements Clock HIGH	9.5	10.0	10.5	V	Note 3
$V\phi IC$ HIGH	Integration Control Clock HIGH		10.0		V	Note 3
$V\phi IC$ LOW	Integration Control Clock LOW		6.0		V	Note 2, 3
$V\phi X$ LOW	Transfer Clock LOW	0.0	0.3	0.7	V	Note 2, 3
$V\phi 1$ LOW (A+B)	Transport Clock LOW	0.0	0.3	0.7	V	Note 2, 3
$V\phi 2$ LOW (A+B)	Transport Clock LOW	0.0	0.3	0.7	V	Note 2, 3
$V\phi R$ LOW (A+B)	Reset Clock LOW	0.0	0.3	0.7	V	Note 2, 3
$V\phi SH$ LOW (A+B)	Sample/Hold Clock LOW	0.0	0.3	0.7	V	Note 2, 3
$V\phi 1024$ LOW	Select 1024 Elements Clock LOW	0.0	0.3	0.7	V	Note 2, 3, 5
$V\phi 1728$ LOW	Select 1728 Elements Clock LOW	0.0	0.3	0.7	V	Note 2, 3, 5
$V\phi 2048$ LOW	Select 2048 Elements Clock LOW	0.0	0.3	0.7	V	Note 2, 3, 5
f_{data} max	Maximum Output Data Rate	10.0	20.0		MHz	Note 6

AC CHARACTERISTICS: $T_P = 25°C$, (Note 1, 7), $f_{data} = 3.0MHz$, $t_{int} = 1.0$ ms, Light Source = 2854°K + 2.0mm thick Schott BG-38 and OCLI WBHM Filters (Note 4).

SYMBOL	CHARACTERISTIC	RANGE			UNIT	CONDITIONS
		MIN	TYP	MAX		
DR	Dynamic Range (relative to peak-to-peak noise) (relative to rms noise)		 1500:1 7500:1			
NEE	RMS Noise Equivalent Exposure		 50×10^{-6}		 $\mu J/cm^2$	
SE	Saturation Exposure		0.3		$\mu J/cm^2$	
CTE	Charge Transfer Efficiency	.99996	.99999			Note 8
V_O	Output DC Level	4.0	9.5	11	V	
Z	Output Impedance		1		K Ω	
P	On-Chip Power Dissipation: Amplifiers		 159	 200	 mW	
N	Peak-to-Peak Temporal Noise		0.7		mV	

Fairchild Imaging, Inc., 1801 McCarthy Blvd., Milpitas, CA 95035 • (800)325-6975 • (408) 433-2500

PERFORMANCE CHARACTERISTICS: $T_P = 25°C$ (Note 1, 7), $f_{data} = 3.0MHz$, $t_{int} = 1.0ms$, Light Source = 2854°K + 2.0mm thick Schott BG-38 and OCLI WBHM filters (Note 4).

SYMBOL	CHARACTERISTIC	RANGE			UNIT	CONDITION
		MIN	TYP	MAX		
PRNU*	Photoresponse Non-uniformity					
	Peak-to-Peak		60	160	mV	
	Peak-to-Peak without single pixel and Positive and Negative Pulses		40		mV	
	Single-pixel Positive Pulses		35		mV	
	Single-pixel Negative Pulses		35		mV	
M Video	Video Mismatch		50	150	mV	Note 9
M DC	DC Mismatch		0.5	2.0	V	Note 10
DS	Dark Signal:					Notes 11, 12
	DC Component		1	2	mV	
	Low Frequency Component		1	2	mV	
SPDSNU	Single Pixel DS Non-Uniformity		1	2	mV	Note 12
R	Responsivity		4.0		$V/\mu J/cm^2$	
V_{SAT}	Saturation Output Voltage	0.7	1.0	1.8	V	

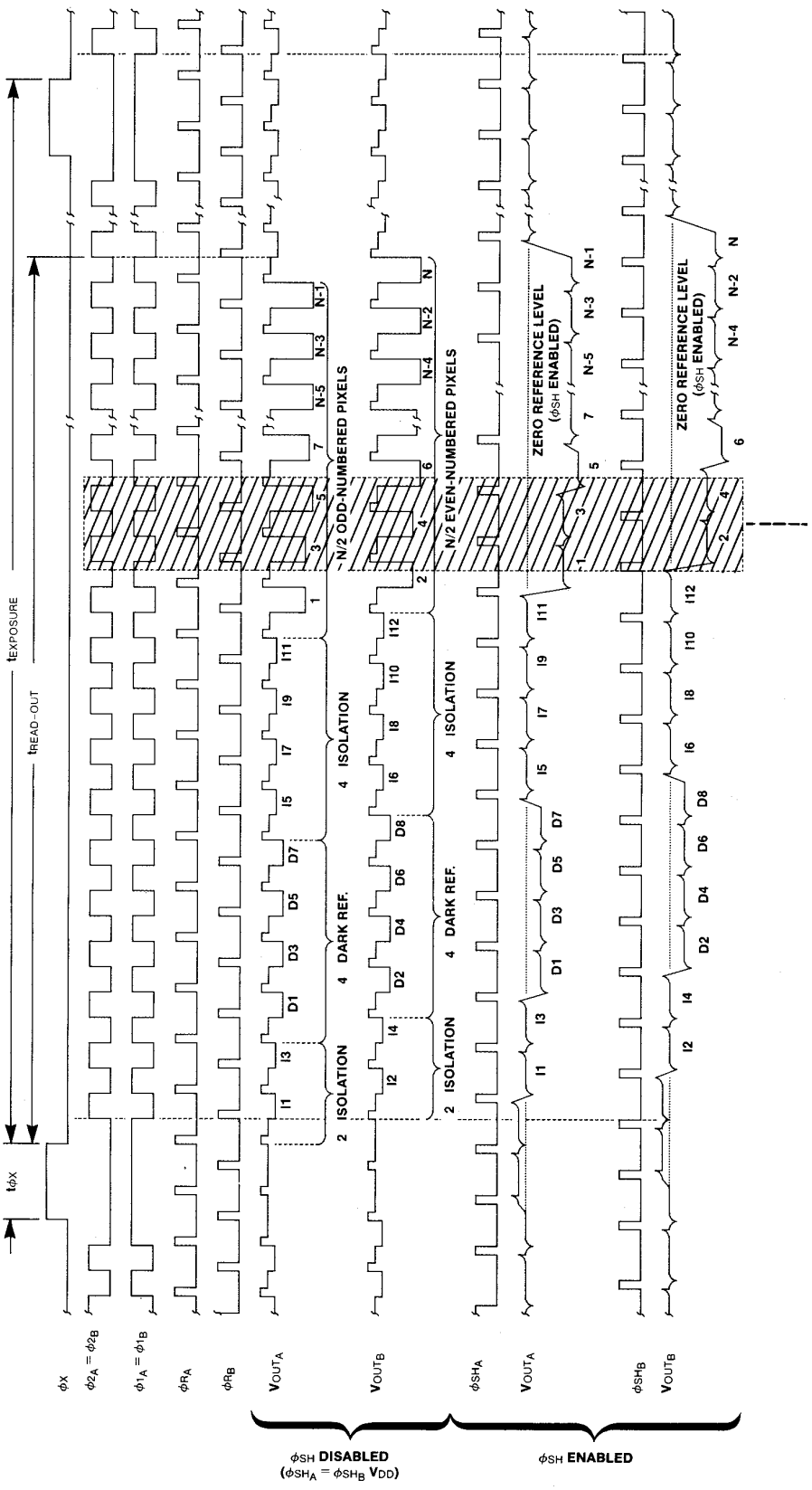
* All PRNU measurements are taken at an 800 mvolt output level using an f/5.0 lens and exclude the outputs from the first and last elements of the array. The "f" number is defined as the distance from the lens to the array divided by the diameter of the lens aperture. As the "f" number increases, the resulting more highly collimated light causes the package window imperfections to dominate and increase PRNU. A lower "f" number results in less collimated light causing device photosite blemishes to dominate the PRNU.

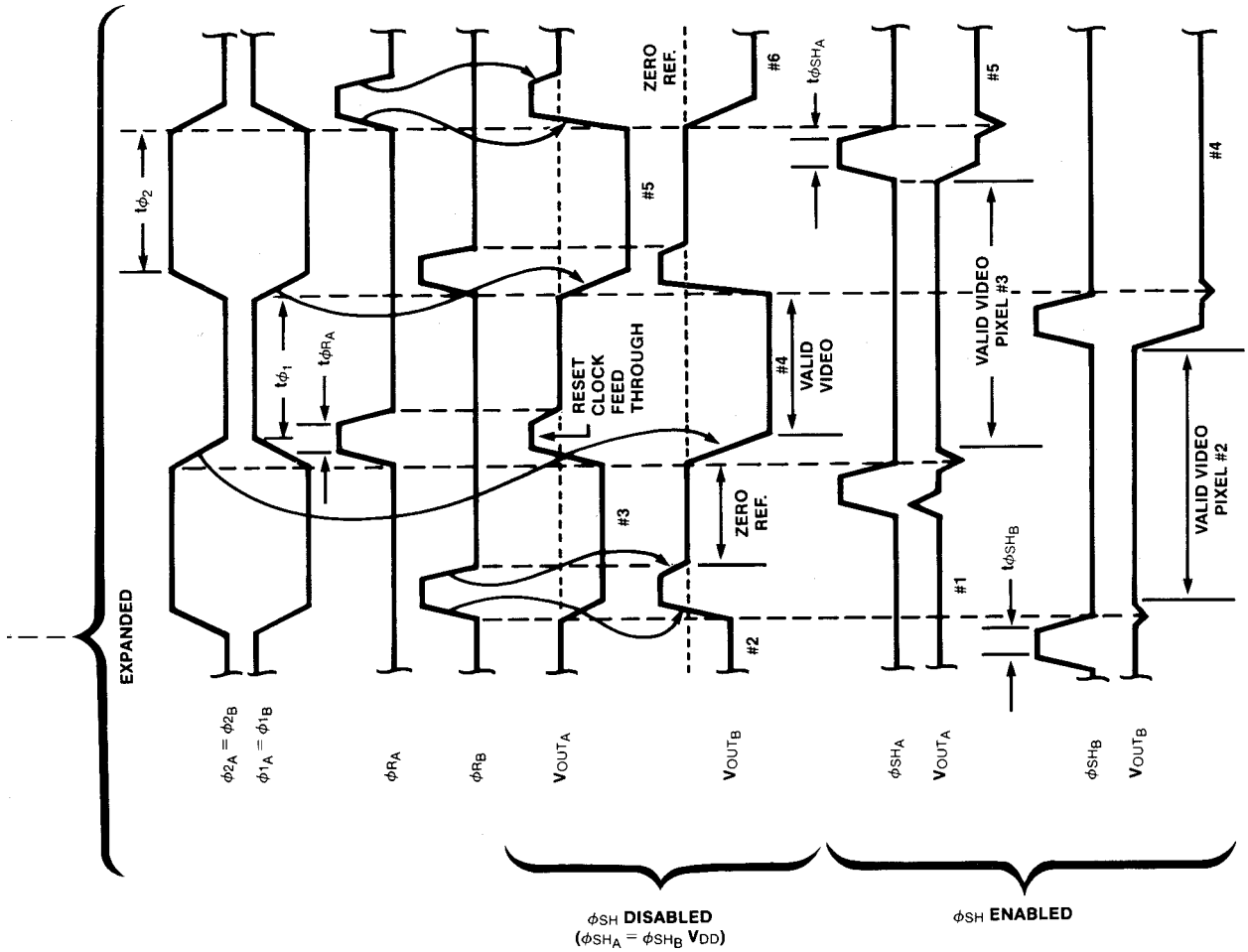
NOTES:

1. T_P is defined as the package temperature measured on a copper block in good thermal contact with the entire backside of the package.
2. Negative transients on any clock pin going below 0.0 volts may cause charge injection, which results in an increase in apparent DS. Adjusting V_{SS} to a more negative voltage than the clock low voltages will reduce charge injection, if present.
3. $C\phi_X = 150pF$, $C\phi_{EC} = 250pF$, $C\phi_{1A} = C\phi_{1B} = C\phi_{2A} = C\phi_{2B} = 300pF$
   $C\phi_{RA} = C\phi_{RB} = C\phi_{SHA} = C\phi_{SHB} = 5pF$, $V_{1024} = V_{1728} = V_{2048} = 50pF$
4. OCLI WBHM = Optical Coating Laboratory, Inc. Wide Band Hot Mirror.
5. Pixel Length Selection
   (a) To use the device with 2592 active pixel elements:
   Connect V_{1024}, V_{1728}, and V_{2048} to the ϕ_2 (A or B) clock.
   (b) To use the device with 2048 active pixel elements:
   Connect V_{1024}, V_{1728} to the ϕ_2 (A or B) clock.
   Connect V_{2048} to V_{SS}
   (c) To use the device with 1728 active pixel elements:
   Connect V_{1024} and V_{2048} to the ϕ_2 (A or B) clock.
   Connect V_{1728} to V_{SS}
   (d) To use the device with 1024 active pixel elements:
   Connect V_{1728} and V_{2048} to the ϕ_2 (A or B) clock.
   Connect V_{1024} to V_{SS}
6. The minimum clock frequency is limited by increases in dark signal.
7. Measurements made with sample and hold enabled.
8. CTE is the measurement for a one-stage transfer.
9. Video mismatch is the difference in AC amplitudes between V_{OUT} A and V_{OUT} B under uniform illumination. it can be eliminated by attenuation/amplification of one of the video outputs.
10. DC mismatch is the difference in DC output level V_O between V_{OUT} and V_{OUT} B.
11. Dark signal component approximately doubles for every 5 to 15°C in T_P.
12. Each SPDSNU is measured from the DS level adjacent to the base of the SPDSNU. The SPDSNU approximatley doubles for every 5 to 15°C increase in T_P.

Fairchild Imaging, Inc., 1801 McCarthy Blvd., Milpitas, CA 95035 • (800)325-6975 • (408) 433-2500

CCD181 TIMING DIAGRAM





NOTES:

1. Timing requirements for ϕ_1 and ϕ_2:
   a. 50 ± 10% duty cycle, ~180° out of phase (See 1b).
   b. ϕ_1 and ϕ_2 clocks must cross at ≥4V.
      (Both ϕ_1 and ϕ_2 must not be <4V simultaneously.)
   c. $(0.1 \cdot t\phi_2) \leq (t_{rise} = t_{fall}) < (0.4 \cdot t\phi_2)$
2. Timing requirements for ϕR_A and ϕR_{2B}:
   a. $20ns \leq (t_{rise} = t_{fall}) < (0.3 \cdot t\phi_R)$
   b. $30ns < (t\phi R_A = t\phi R_B) < t\phi_2$
   c. t_{fall} time of ϕR_A must not overlap t_{rise} of ϕR_A
   d. t_{fall} time of ϕR_B must not overlap t_{rise} of ϕR_B
3. Timing requirements for ϕSH_A and ϕSH_B:
   a. $20ns \leq (t_{rise} = t_{fall}) < (0.3 \cdot t\phi_2)$
   b. $(t\phi SH_A = t\phi SH_B) \geq 80ns$
   c. t_{fall} time of ϕSH_A must not overlap t_{fall} timer of ϕ_2.
   d. t_{fall} time of ϕSH_B must not overlap t_{fall} timer of ϕ_1.
4. Timing requirements for ϕ_X:
   a. $t\phi_X \geq 0.1\mu s$
   b. t_{rise} and t_{fall} times of ϕ_X must not overlap t_{rise} or t_{fall} times of ϕ_1 or ϕ_2.
5. Effective number of pixels "N" is selected by "$V_{switch\ (\#i)}$" pins as follows:

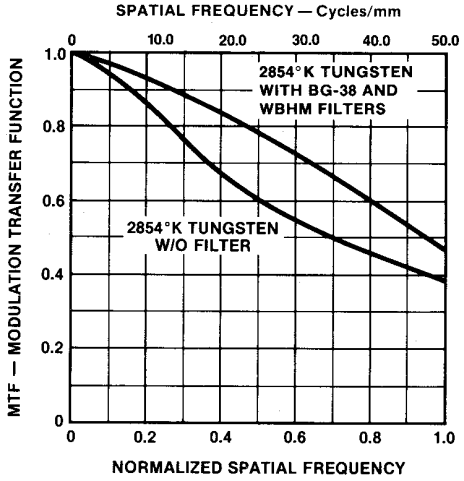
N	INPUTS TO V_{SWITCH} PINS:			
	V_{SWITCH} (1024)	V_{SWITCH} (1728)	V_{SWITCH} (2048)	
1024	V_{SS}	ϕ_2	ϕ_2	
1728	ϕ_2	V_{SS}	ϕ_2	
2048	ϕ_2	ϕ_2	V_{SS}	
2592	ϕ_2	ϕ_2	ϕ_2	

   Resistance between the clocked V_{switch} pins and the $\phi 2_A$ and $\phi 2_B$ pins should be negligiable (<10Ω).

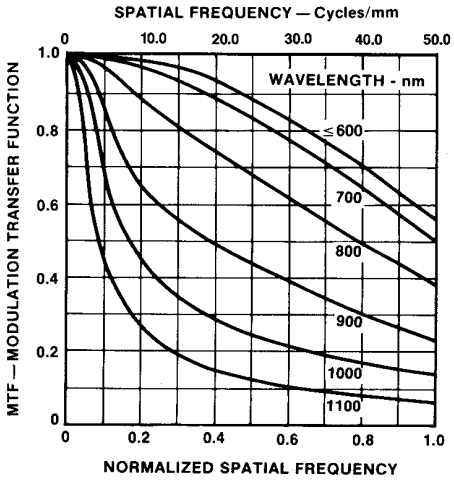
6. Integration Control Clock (ϕIC) has been omitted from these timing diagrams for clarity. See "Integration Control Clock Timing" diagram for details (Fig. 3).

TYPICAL PERFORMANCE CURVES

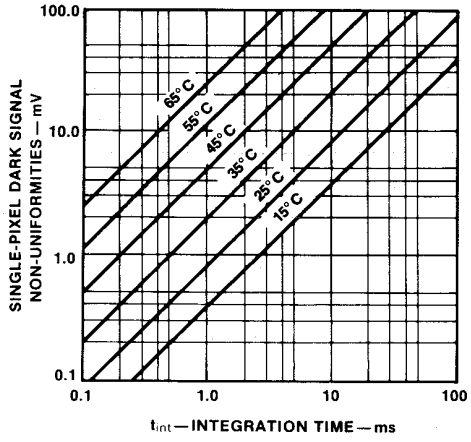
MODULATION TRANSFER FUNCTIONS FOR TWO BROADBAND ILLUMINATION SOURCES



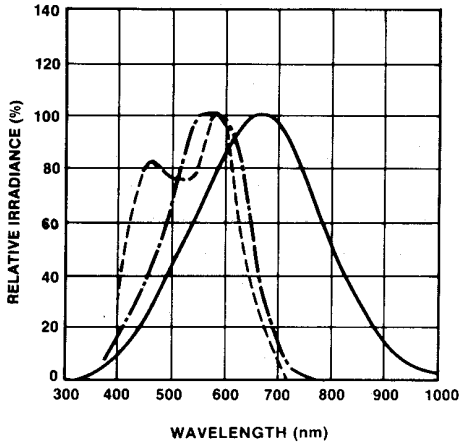
MODULATION TRANSFER FUNCTIONS FOR NARROW BAND ILLUMINATION SOURCES



SINGLE-PIXEL DARK SIGNAL NON-UNIFORMITIES VERSUS INTEGRATION TIME



*RELATIVE RADIANT FLUX VS WAVELENGTH

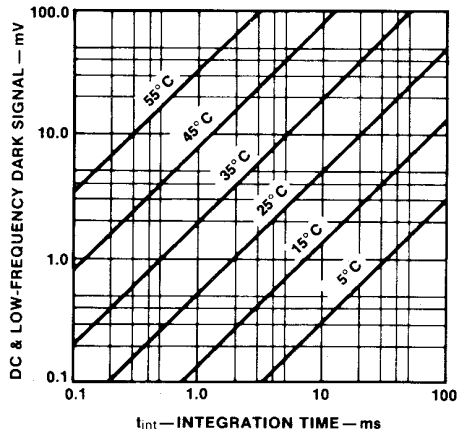


TYPICAL "DAYLIGHT FLUORESCENT" BULB

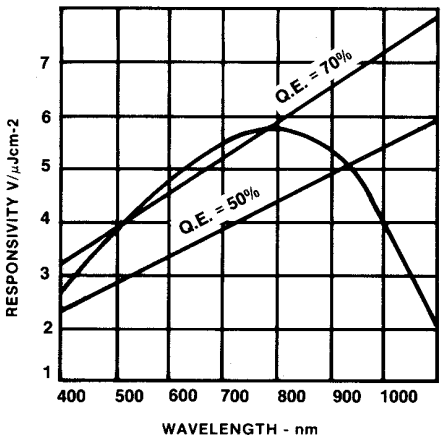
2854°K LIGHT SOURCE +WBHM + 2.0 mm THICK BG-38

2854°K LIGHT SOURCE + 3.0 mm THICK 1-75

DC AND LOW-FREQUENCY DARK SIGNAL VS INTEGRATION TIME

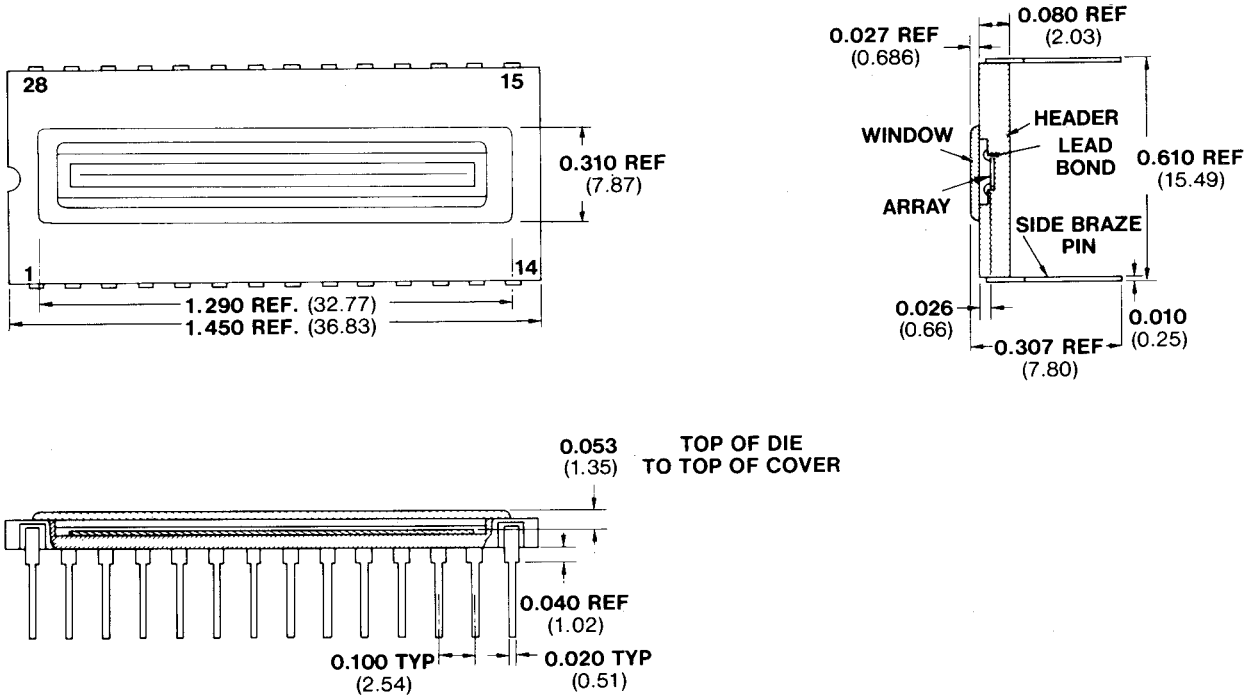


TYPICAL SPECTRAL RESPONSE



Fairchild Imaging, Inc., 1801 McCarthy Blvd., Milpitas, CA 95035 • (800)325-6975 • (408) 433-2500

PACKAGE OUTLINE
28-Pin Dual In-line Ceramic Package



NOTES

All dimensions in inches (bold) and millimeters (parentheses). Header is black ceramic (Al_2O_3). Window is glass. The amplifier of the device is located near the notched end of the package.

DEVICE CARE AND OPERATION

Glass may be cleaned by saturating a cotton swab in alcohol and lightly wiping the surface. Rinse off the alcohol with deionized water. Allow the glass to dry, preferably by blowing with filtered dry N_2 or air.

It is important to note in design and applications considerations that the devices are very sensitive to thermal conditions. The dark signal DC and low frequency components approximately double for every 5º C temperature increase and single-pixel dark signal non-uniformities approximately double for every 12º C temperature increase. The devices may be cooled to achieve very long integration times and very low light level capability.

ORDER INFORMATION

Order CCD181DC where “D” stands for a ceramic package and “C” for commercial temperature range.

Fairchild Imaging, Inc., 1801 McCarthy Blvd., Milpitas, CA 95035 • (800)325-6975 • (408) 433-2500