Dynamic Differential Hall Effect Sensor **TLE4926C-HTN E6747**

Data Sheet Version 3.0 (valid for 8" product)

Features

- **High sensitivity**
- **Single chip solution**
- **Symmetrical thresholds**
- **High resistance to Piezo effects**
- **Advanced performance by dynamic self calibration principle**
- **South and north pole pre-induction possible**
- **1Hz low cut-off frequency**
- **Digital output signal**
- **Two-wire and three-wire configuration possible**
- **Wide operating temperature range**
- **Fast start-up time**
- **Large operating airgaps**
- **Reverse voltage protection at Vs- PIN**
- **Short- circuit and over temperature protection of output**
- **No external filter capacitor required**
- **Digital output signal (voltage interface)**
- **Module style package with two integrated capacitors:**
  - **4.7nF between Q and GND**
  - **47nF[1] between V_S and GND: Needed for micro cuts in power suply**
- **High temperature profile**
- **Package: PG-SSO-3-91 with nickel plating instead of standard 100% Sn plating**

Type	Marking	Ordering Code	Package
TLE4926C-HTN E6747	26C8	SP000269347	PG-SSO-3-91

[1] value of capacitor: 47nF±10%; (excluded drift due to temperature and over lifetime); ceramic: X7R; maximum voltage: 50V.

General Information

TLE4926C is an active Hall sensor suited to detect the motion and position of ferromagnetic and permanent magnet structures. An additional self-calibration module has been implemented to achieve optimum accuracy during normal running operation. It comes in a three-pin package for the supply voltage and an open drain output.

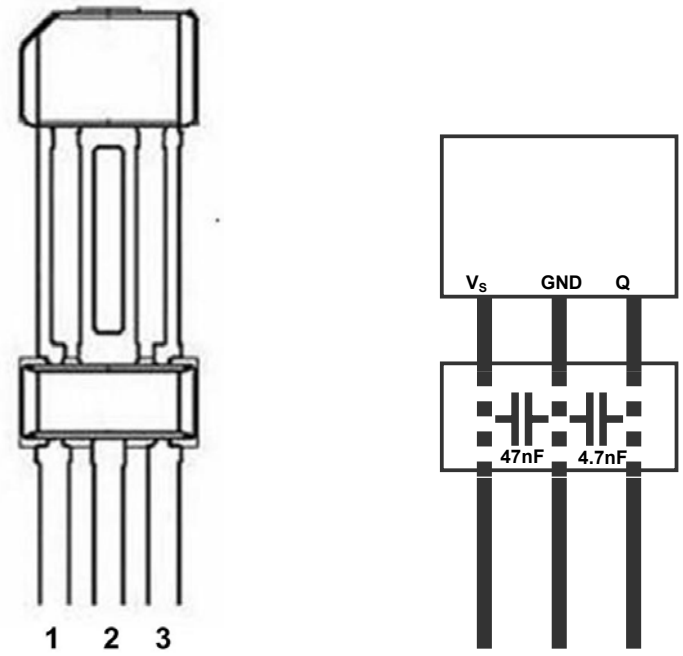


Figure 1: Pin configuration in PG-SSO-3-91

Pin No.	Symbol	Function
1	V_S	Supply Voltage
2	GND	Ground
3	Q	Open Drain Output

Functional Description

The differential Hall sensor IC detects the motion and position of ferromagnetic and permanent magnet structures by measuring the differential flux density of the magnetic field. To detect ferromagnetic objects the magnetic field must be provided by a back biasing permanent magnet (south or north pole of the magnet attached to the rear unmarked side of the IC package).
Offset cancellation is achieved by advanced digital signal processing. Immediately after power-on motion is detected (start-up mode). After a few transitions the sensor has finished self-calibration and switches to a high-accuracy mode (running mode). In running mode switching occurs at signal zero-crossing of the arithmetic mean of max and min value of magnetic differential signal. ΔB is defined as difference between hall plate 1 and hall plate 2.

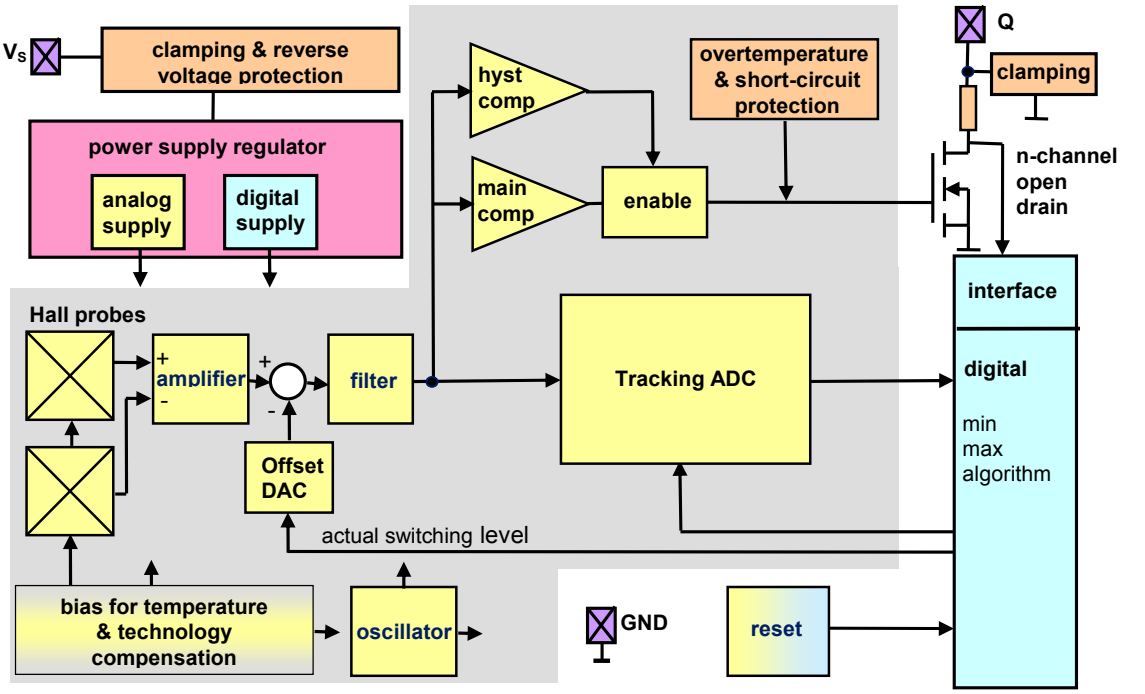


Figure 2: Block Diagram of TLE4926C

Basics of self-calibration

A magnetic signal generated by a typical toothed wheel looks somewhat like a sinusoid. Optimum switching points lie near the zero crossings of the curve. Due to backbiasing conditions and imperfections in the IC the signal is superposed by an offset. Therefore the main task to accomplish is to remove this offset. This is done by measuring the minimum and maximum values of the curve and by calculating the resulting offset. By subtracting this offset from the original signal, the signal is centered on its zero crossings and these can be detected by a normal comparator. The detection of the minimum and maximum values as well as the complete signal correction strategy is implemented in a digital way. Therefore first the signal has to be digitized.

Digitizing the signal

A tracking A/D converter basically does signal conversion from analog into digital domain. The converter has a resolution of 6 bits. This (including some averaging calculation described later on) is sufficient for characterizing the signal if the signal is not too small. Therefore, a programmable gain amplifier (PGA) enhances the A/D converter. Its amplification can be modified by powers of two. 7 different positions are possible; the amplification range lies between ½ and 32 (Full scale A/D converter range referred to full-scale range of the offset- Dac). The gain of the PGA tracks the amplitude of the signal so that sufficient resolution of the converter is ensured. The gain of the PGA is decreased by 1 step (a factor of 2) whenever a signal overrun in the tracking converter is detected. On the other hand, the gain of the PGA is increased by 1 step, when during an offset update low signal amplitude is detected. This means, that the actual minimum value is larger or equal 50H (on an 8 bit base referred to the averaged Gain- Dac) and the actual maximum value is smaller than

B0H. This procedure ensures a sufficient resolution for each signal amplitude. After doing the 6 bit A/D conversion running at system clock speed (1.455MHz), the values are put into a simple decimation filter, which sums up 8 consecutive values and, by truncating the least significant bit, delivers an 8 bit output signal at 1/8 system speed (182kHz). The rest of the digital calibration process now refers to this 8 bit data (Min-Max finding, offset calculation). The tracking converter as well as the PGA is protected against overflow or underflow, so no wrap-around or undefined condition can occurs. Instead the signal is clipped to a maximum or minimum value.

Finding the minimum and maximum values

During operation a dedicated logic block looks for the smallest numerical input value. If the signal is falling, this block permanently stores new input values. If the signal is larger than the stored value, the stored value remains memorized. If, after a minimum value, the signal increases for a certain amount (digital noise constant) this memorized value is called a minimum and propagated to another register (minimum register). The same procedure (with opposite sign) applies to maximum values. The digital noise constant has a value 30H with one exception: If the PGA is in maximum amplification the digital noise constant is 48H. The noise constant is referred to the 8 bit Gain- Dac value. Each newly identified maximum starts another search for a new minimum. Each newly identified minimum starts another search for a new maximum. In this way alternating new minimum and maximum values can be identified. This ensures, that “all time high” or –low values do not remain in memory. Instead, only recent minimum and maximum values are obtainable.

Valid and invalid min/max values

After initialization, new calibration and PGA-changes the circuit starts a new search for minimum and maximum values. Assuming the process starts at a rising signal slope, then the initial point may become to a minimum since it is the lowest observed value so far. This occurrence is memorized, but the minimum is called an invalid minimum. The same can occur if the search starts at a falling edge for a maximum. A minimum is called a valid minimum if it is preceded by any (valid or invalid) maximum. The same is true for maximum values. Any minimum or maximum value is discarded immediately, if there is a new initialization, new calibration or a PGA-change.

Startup of the device

After power on or an internal reset a new calibration procedure is started. First, the external comparator output is locked. Second, the offset-DAC is set in that way, that it compensates the incoming signal. This is done by a successive approximation search. For a steady state input signal the offset DAC therefore gets the value of this input signal and the digital inputs are the digital representation of this value. For a varying signal the approximation search ends up in a value which is somewhere near the input signal during the duration of the successive approximation search. This is the initial calibration value. Of course the remaining offset value may still be quite large. Then the minimum and maximum search is started. After having found the first minimum or maximum the output switches according to the definition (low output

stage for maximum because of falling edge and high output stage for minimum because of rising edge). This behaviour continues until the first valid minimum and maximum values are found. With this pair of values there is sufficient information for getting a quite accurate new calibration result, so that the output can switch with the result given by the internal comparator. The average of the minimum and maximum value gives a representation of the offset. More precisely, the minimum and maximum value (8 bit values respectively) is summed up, the result is subtracted by 256 (=100H), this result is shifted to the correct position taking into account the current setting of the PGA, and finally this value is added to the current offset value. The whole procedure can be repeated for many times and converges to an offset value which compensates for the signal offset. In other words, if the minimum and the maximum have equal magnitude, their sum will be 100H (80H is the mid-value) and after subtraction of 100H a correction value of zero will appear.

The shifter, which multiplies the sum off minimum a maximum in corresponding to the PGA position, calculates the offset- update. In PGA = 3 no shift is applied and the sum is added (or subtracted) directly from the offset. In PGA = 2 the sum is divided by 2, in PGA = 4 the sum is multiplied by 2 and so on. But the so calculated update is not applied every time; in fact there is a nonlinear filter that avoids small offset-correction in order to improve jitter.

Continuous calibration

Once the device has finished its first calibration it enters a continuous calibration mode. Basically this means that after each edge transition going out of the circuit a new offset value can be adjusted. To avoid a offset- jumping due to a unregular wheel or noise there is implemented a fincal state and a update filter. The algorithm enter in the fincal state if the difference between the maximum and minimum is less then 8 Lsb, and the finecal state will be left if the difference is more then 16 Lsb. Below the 8 Lsb value the offset is not changed, between 16 Lsb and 8 Lsb only 1 Lsb steps are done, and over the 16 Lsb threshold value full adjustment is possible. The update- filter lets perform the calculated update- step only if the last and the current update are over the 8 Lsb threshold an if the update- directions are the same. This avoids unwanted offset- updates due to long notches or teeth (long notches generate higher amplitudes). The offset calculation unit is protected against overrun errors so it will clip the values at zero and full scale (3FFH). A set of rules apply to the calibration process which regulate under which condition and to what amount an offset calibration is done.

Mathematical relation between max, min, PGA and offset:
Offset(mT)=Offset(Lsb) * Fullscale/1023(Lsb) – Fullscale/2;
120mT = Full-scale of the Offsetdac with 1023 Bit;
Max(mT)=Offset(mT) + (Max(Lsb) – 128)*2^(PGA –3) * Fullscale/1023(Lsb);
Min(mT)= Offset(mT) - (128 - Min(Lsb))*2^(PGA –3) * Fullscale/1023(Lsb);

Trigger rules for offset update in running mode

As already mentioned, at either a positive or negative comparator edge the offset may be updated. At this time, several circuit conditions are checked. The following rules apply:
After a modification of the PGA setting the update capability is disabled. With the 3rd following comparator edge the update capability is enabled again.
After an offset update the update capability is disabled. With the 2nd following comparator edge the update capability is enabled again.
At any offset update the circuit checks if there has been a larger signal value than that which is stored in the maximum register. In this case, the larger value will be taken. The same (with opposite sign) is true for minimum values.
If a valid minimum or a valid maximum has been found and none of the above rules is against it, a calibration may occur. This must not be the first calibration after the initial calibration.
Any calibration may occur only at the correct comparator edge. This means that a negative signal shift due to offset correction may occur only during the negative going signal slope. The same is true for positive signal shift and the rising signal slope.

Watchdog operation

If for a certain time (2^20 clock pulses – 0.7 s) there is no switching at the output the watchdog will start a new observation period. It is responsible for a new initialization by issuing a system reset. So a new selfcalibration (successive approximation of offset) is started and the PGA and GainDac are reseted (PGA=0, GainDac=100000 binary). During the selfcalibration the output is held to the old value, afterwards it is switched according to the edge-detection.
The second check that is implemented is the PGA decrement: if no max or min is found during 16 output- switching events the PGA is decremented by 1. No other actions are performed if such a situation is detected.

Digital main-comparator

The digital main-comparator receives the output of the three threshold comparators hypcomp_low, main_comp and hypcomp_high. This inputs are used in an asynchronous way, so that no clock-delay is introduced.
The function of the digital main-comparator is to implement a hidden hysteresis; that means, that the ouput switches accordingly to the main_comp threshold and the upper and lower hysteresis limits are used to lock the output. In this way no hysteresis is visible in the switching behavior and we have a high noise rejection.

Summary

The IC monitors the positive and negative peak values of the signal to adjust its offset properly. For large deviations the actual offset correction value is calculated as accurate as possible, for smaller deviations also a slow calibration mode by only incrementing and decrementing or by not changing the offset value can be entered. The device is monitored by a watchdog, which starts a new initialization if there is no input signal.

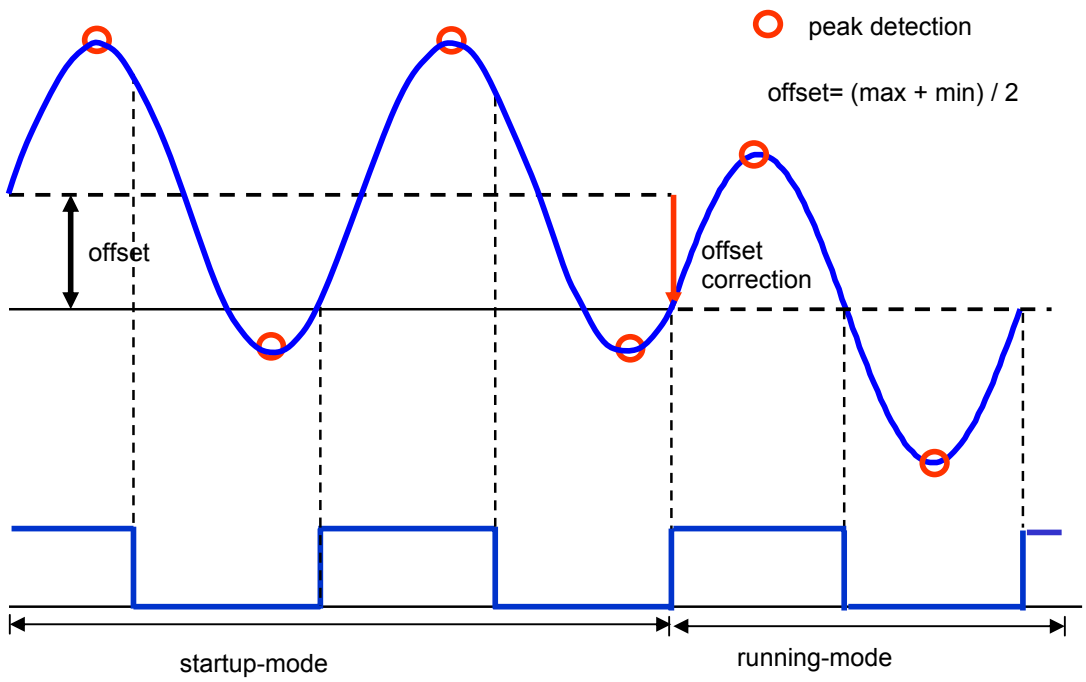


Figure 3: Startup of the device

At transition from startup-mode to running mode switching timing is moving from low-accuracy to high accuracy zero-crossing.

1.1 Absolute Maximum Ratings

No.	Parameter	Symbol	min	typ	max	Unit	Remarks
1.1.1	Supply voltage	V_S	-18		18	V	-
			-24		24	V	1h with $R_{Series} \geq 200\Omega$[2]
			-26		26	V	5min with $R_{Series} \geq 200\Omega$[1]
			-28		28	V	1min with $R_{Series} \geq 200\Omega$[1]
1.1.2	Supply current	I_S	-10		25	mA	-
1.1.3	Output OFF voltage	V_Q	-0.3		18	V	-
			-18		24	V	1h with $R_{Load} \geq 500\Omega$
			-18		26	V	5min with $R_{Load} \geq 500\Omega$
			-1.0		-	V	1h (protected by internal series resistor)
1.1.4	Output ON voltage	V_Q	-		16	V	Current internal limited by Short circuit protection (72h @ $T_A < 40°C$).
			-		18	V	Current internal limited by short circuit protection (1h @ $T_A < 40°C$).
			-		24	V	Current internal limited by short circuit protection (1min @ $T_A < 40°C$).
1.1.5	Continuous output current	I_Q	-50		50	mA	-
1.1.6	Junction temperature	T_j	-40			°C	-
					155	°C	5000 h (not additive)
					165	°C	2500 h (not additive)
					175	°C	500 h (not additive)
					195	°C	10x1 h (additive to the other life times).
1.1.7	Storage temperature	T_S	-40		150	°C	-
1.1.8	Thermal resistance junction-air	$R_{th\ JA}$			190	K/W	Lower values are possible with overmolded device.

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] Accumulated life time

1.2 Electro Magnetic Compatibility - *(values depend on R_{Series}!)*

Ref. ISO 7637-2; see test circuit of figure 4;

ΔB_{PP} = 10mT (ideal sinusoidal signal); V_S=13.5V ± 0.5V, f_B= 1000Hz; T= 25°C; $R_{Series} \geq 200\Omega$;

No.	Parameter	Symbol	Level/typ	Status
1.2.1	Testpulse 1	V_{EMC}	III / -90V	C
	Testpulse 2		III / 40V	A[3]
	Testpulse 3a		IV / -150V	A
	Testpulse 3b		IV / 100V	A
	Testpulse 4		IV / -7V	A
	Testpulse 5		III / 66.5V	C

Note: Test criteria for status A: No missing pulse no additional pulse on the IC output signal plus duty cycle and jitter are in the specification limits.
Test criteria for status B: No missing pulse no additional pulse on the IC output signal. (Output signal "OFF" means switching to the voltage of the pull-up resistor).
Test criteria for status C: One or more parameter can be out of specification during the exposure but returns automatically to normal operation after exposure is removed.
Test criteria for status E: IC destroyed.

Ref. ISO 7637-3; TP 1 and TP 2 ref. DIN 40839-3; see test circuit of figure 4;

ΔB_{PP} = 10mT (ideal sinusoidal signal); V_S=13.5V ± 0.5V, f_B= 1000Hz; T= 25°C; $R_{Series} \geq 200\Omega$;

No.	Parameter	Symbol	Level/typ	Status
1.2.2	Testpulse 1	V_{EMC}	IV / -30V	A
	Testpulse 2		IV / 30V	A
	Testpulse 3a		IV / -60V	A
	Testpulse 3b		IV / 40V	A

Ref. ISO 11452-3; see test circuit of figure 4; measured in TEM-cell

ΔB_{PP} = 4mT (ideal sinusoidal signal); V_S=13.5V ± 0,5V, f_B= 200Hz; T= 25°C; $R_{Series} \geq 200\Omega$;

No.	Parameter	Symbol	Level/max	Remarks
1.2.3	EMC field strength	$E_{TEM\text{-}Cell}$	IV / 200V/m	AM=80%, f=1kHz;

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Test condition for the trigger window: $f_{B\text{-}field}$=200Hz, B_{pp}=4mT, vertical limits are ±200mV and horizontal limits are ±200µs.

[3] Valid for general function, current consumption and jitter may be out of spec during test pulse 2.

1.3 ESD Protection

No.	Parameter	Symbol		max	Unit	Remarks
1.3.1	ESD – protection	V_{ESD}		± 4	kV	According to standard EIA/JESD22-A114-B Human Body Model (HBM).

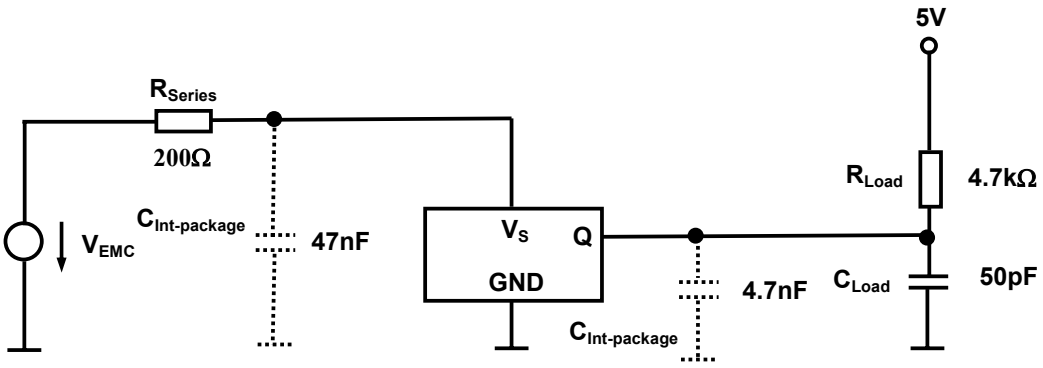


Figure 4: Test circuit for EMC-tests

2.1 Operating Range

No.	Parameter	Symbol	Min	typ	max	Unit	Remarks
2.1.1	Supply voltage	V_S	3.3		18	V	Continuous
					24	V	1h with $R_{Series} \geq 200\Omega$;
					26	V	5min with $R_{Series} \geq 200\Omega$. Extended limits for parameters in characteristics.
			3			V	During test pulse 4 $R_{Series}=200\Omega$; Ta=25°C Limited performance possible (jitter)
2.1.2	Supply voltage ripple	V_{SAC}			6	V_{pp}	V_S=13V; 0 < f < 50kHz
2.1.3	Continuous output OFF voltage	V_Q	0		18	V	Continuous
			0		24	V	1h with $R_{Load} \geq 500\Omega$
2.1.4	Continuous output ON current	I_Q	0		20	mA	V_{Qmax}=0.6V
2.1.5	Power on time	t_{on}			1	ms	Time to achieve specified accuracy After power on the output of the IC is always in high-state. After internal resets output is locked[4].
2.1.6	Operating junction temperature	T_j	-40			°C	-
					155	°C	5000 h (not additive)
					165	°C	2500 h (not additive)
					175	°C	500 h (not additive) reduced signal quality permittable (e.g. jitter).

Note: Unless otherwise noted, all temperatures refer to junction temperature.
For the supply voltage lower than 28V ($R_{Series} \geq 200\Omega$) and junction temperature lower than 195°C the magnetic and AC/DC characteristics can exceed the specification limits.

[4] Output of the IC is locked in present state (high-state or low-state) after an internal reset is launched. This reset happens typically every 780ms when there is no output switching in either case. See also 2.2.14. A voltage reset causes a release of the output and output is in high state after power on again.

2.2 AC/DC Characteristics

Over operating range, unless otherwise specified. Typical values correspond to V_S=12V and T_A=25°C

No.	Parameter	Symbol	min	typ	max	Unit	Remarks
2.2.1	supply current	I_S	3	6.8	9	mA	-
2.2.2	supply current @ 3.3V	I_{SVmin}	3	6.7	8	mA	V_S=3.3V
2.2.3	supply current @ 24V	I_{Smax}	3	7	9.5	mA	V_S=24V $R_{Series} \geq 200\Omega$
2.2.4	Output saturation voltage	V_{Qsat}		0.25	0.6	V	I_Q= 20mA
2.2.5	Output leakage current	I_{Qleak}		0.1	10	µA	V_Q= 18V
2.2.6	Current limit for short-circuit protection	I_{Qshort}	30	60	80	mA	-
2.2.7	Junction temperature limit for output protection	T_{prot}	195	210	230	°C	-
2.2.8	Output rise time	t_r[5]	4	12	20	µs	V_{Load} = 4.5 to 24V R_{Load} = 1.2kΩ; C_{Load} = 4.7nF included in package
2.2.9	Output fall time	t_f[6]	0.5 0.65	0.9 1.15	1.3 1.65	µs µs	V_{Load} = 5V V_{Load} = 12V R_{Load} = 1.2kΩ; C_{Load} = 4.7nF included in package
2.2.10	Delay time Falling edge Rising edge	t_d	7	12.5	18[7] 20 25[8]	µs µs µs	Only valid for Tj=25°C. Tj=-40°C -Tj=175°C Tj=-40°C -Tj=175°C Higher magnetic slopes and over -shoots reduce t_d, because the signal is filtered internal.[9]
2.2.11	Temperature drift of delay time of output to magnetic edge	Δt_d	-6	3[10]	6	µs	Time over specified temperature range; not additional to t_d.

[5] value of capacitor: 4.7nF±10% (excluded drift due to temperature); ceramic: X7R; maximum voltage: 100V. The rise time is defined as the time between the 10 and 90% value.
[6] see footnote 3.
[7] Only valid for the falling edge
[8] Not subject to production test-verified by design/characterisation
[9] measured with a sinusoidal-field with 10mTpp and a frequency of 1kHz.
[10] related to Tj=175°C.

2.2.12	Frequency range	f	0.001		8	kHz	Operation below 1Hz[11]
2.2.13	Oscillator frequency	f_{OSC}	1.08	1.34	1.68	MHz	-
2.2.14	Offset recalibration time after last output change	t_{reset}	625	780	970	ms	Output locked to state before recalibration
2.2.15	Clamping voltage V_S-Pin	V_{Sclamp}	24	27.5		V	I_S = 20mA < 5min.
2.2.16	Clamping voltage Q- Pin	V_{Qclamp}	24	27.5		V	I_Q = 20mA < 5min.
2.2.17	Analog reset voltage	V_{sReset}		2.35	2.9	V	-

Note: The listed AC/DC and magnetic characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not other specified, typical characteristics apply at T_j = 25 °C and V_S = 12 V.

2.3 Magnetic Characteristics in Running Mode

No.	Parameter	Symbol	min	typ	max	Unit	Remarks
2.3.1	Bias preinduction	B_0	-500		500	mT	-
2.3.2	Differential bias induction	ΔB_0	-30		30	mT	-
2.3.3	Minimum signal amplitude	$\lvert\Delta B_{min}\rvert$	0.55		1.5	mT	
2.3.4	Maximum signal amplitude	$\lvert\Delta B_{max}\rvert$			100	mT	Additional to B_0 [12].
2.3.5	Resistivity against mechanical stress (piezo)	$\lvert\Delta B_{min}\rvert$	-0.2		0.2	mT	F= 2N

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_j=25°C and the given supply voltage.

3.1 Self-calibration Characteristics

No.	Parameter	Symbol	min	typ	max	Unit	Remarks
3.1.1	No. of magnetic edges for first output switching	n_{Start}			2	-	latest 2nd magnetic edge will cause output switching
3.1.2	No. of magnetic edges to enter calibrated mode	n_{Calib}			6[13]	-	Low phase accuracy permitted. See 3.1.7 7th edge with high accuracy (calibrated)

[11] Output will switch if magnetic signal is changing more that 2x $\lvert\Delta B_{min}\rvert$ within offset recalibration time even below 1Hz once per magnetic edge, increased phase error is possible.

[12] Exceeding this limit might result in decreased duty cycle performance. With higher values the internal measured signal will be clipped. This will decrease the phase accuracy.

[13] Valid for sinusoidal signal without noise influence

3.1.3	Duty cycle in running mode	Dty	45	50	55	%	ΔB_{PP} = 10mT ideal sinusoidal input signal (T_j=25°C)
			40	50	60	%	ΔB_{PP} = 10mT ideal sinusoidal input signal (-40°C ≤ T_j < 175°C)
3.1.4	Signal jitter in running mode; 1 sigma value[5]	σ1		≤ ±0.11[14]		%	ΔB_{PP} = 10mT ideal sinusoidal input signal; T_j<150°C
		σ2		≤ ±0.16		%	ΔB_{PP} = 10mT ideal sinusoidal input signal; 150°C ≤ T_j < 175°C
3.1.5	Signal Jitter in running mode at Vs=13V and ripple ±3V 1 sigma value*	σ3		≤ ±0.11		%	ΔB_{PP} = 10mT ideal sinusoidal input signal; T_j<150°C
3.1.6	Effective noise value of the magnetic switching points, 1 sigma value	B_{neff}		25		µT	T_j = 25°C; [15]
					70	µT	The max value corresponds to the rms-values in the full temperature range and includes technological spreads.
3.1.7	Uncalibrated phase error Magnetic edge 1-2 After 3rd edge Magnetic edge 1-3				 ≤ ±90 ≤ ±55 ≤ ±90	°	Related to calibrated switching behaviour. ΔB_{PP} = 10mT ideal sinusoidal input signal [16] Magnetic fields close to 2x $\lvert \Delta B_{min} \rvert$
3.1.8	Frequency distribution of signal jitter		Jitter shall be distributed like white noise				-

[14] depends largely on $\lvert \Delta B_{min} \rvert$, magnetic signal steepness and also on frequency.
[15] The magnetic noise is normal distributed, nearly independent to frequency and without sampling noise or digital noise effects. The typical value represents the rms-value here and corresponds therefore to 1σ probability of normal distribution. Consequently a 3σ value corresponds to 0.3% probability of appearance.
[16] smaller phase errors are possible at higher signal amplitudes, because sinus signal changes to a more rectangle signal.

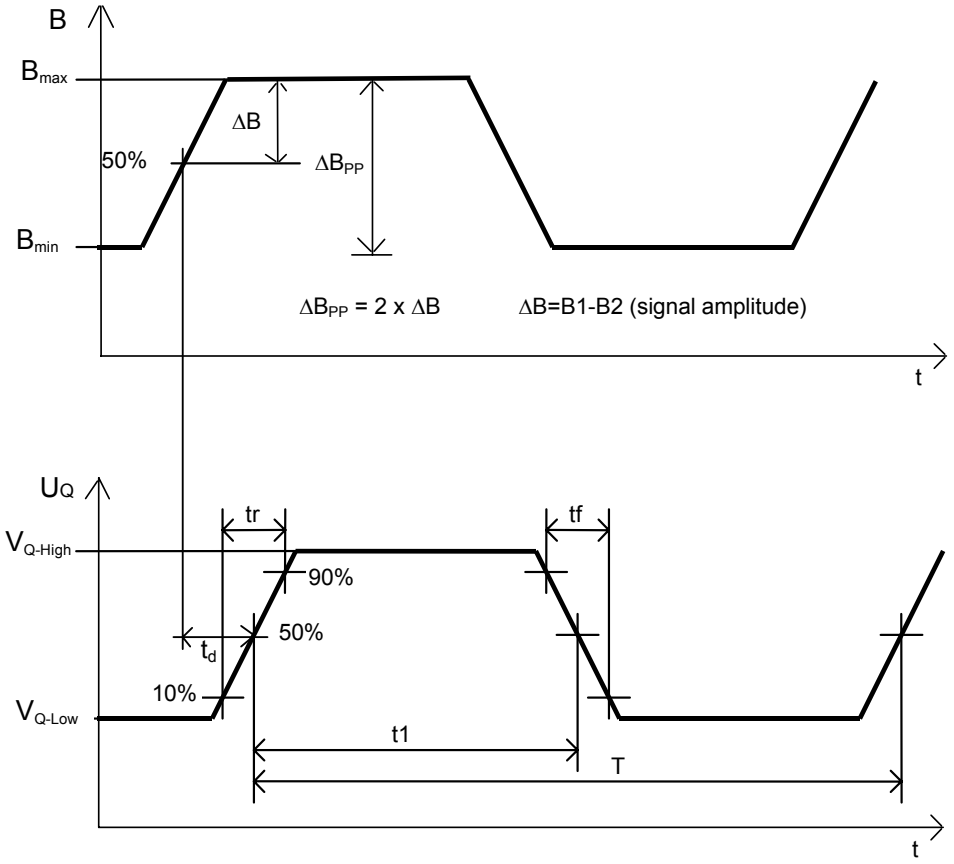
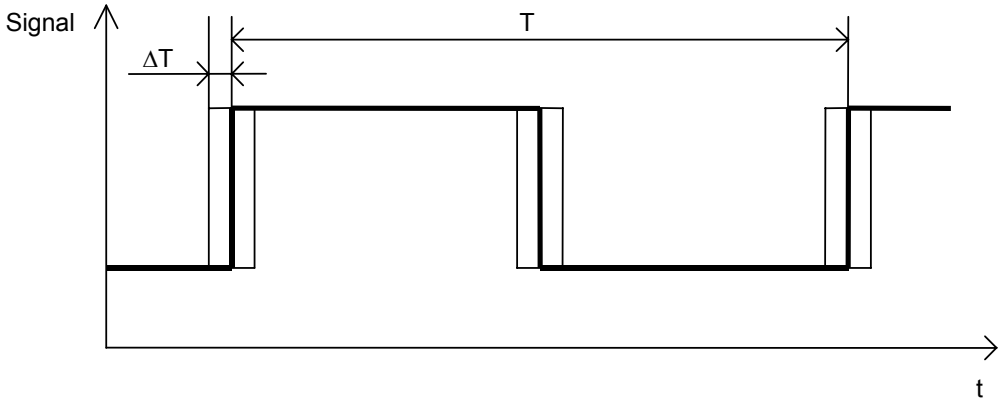


Figure 5 Switching direction



$$\sigma 1 ... \sigma 3 = \frac{1}{T} \cdot \sqrt{\frac{1}{(n-1)} \cdot \sum (\Delta T)^2}$$

measurement condition: n ≥ 1000

Figure 6 Definition of signal jitter

Application Configurations

Two possible applications are shown in **Figure 7** and **Figure 8** (Toothed and Magnet Wheel).

The difference between two-wire and three-wire application is shown in **Figure 11** for the TLE 4926C.

Gear Tooth Sensing

In the case of ferromagnetic toothed wheel application the IC has to be biased by the south or north pole of a permanent magnet (e.g. $SmCO_5$ (Vacuumschmelze VX145)) with the dimensions 8 mm × 5 mm × 3 mm) which should cover both Hall probes.

The maximum air gap depends on

- the magnetic field strength (magnet used; pre-induction) and
- the toothed wheel that is used (dimensions, material, etc.; resulting differential field).

a centered distance of Hall probes
b Hall probes to IC surface
L IC surface to tooth wheel
a = 2.5 mm
b = 0.3 mm

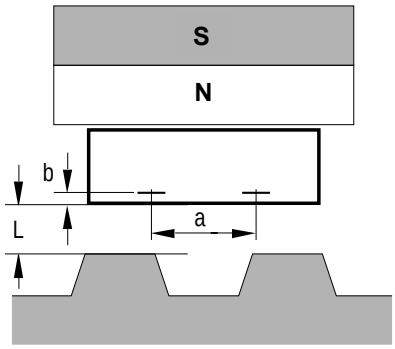
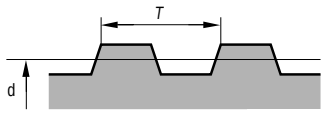


Figure 7 Sensor Spacing



Conversion DIN – ASA
m = 25.4 mm/p
T = 25.4 mm CP

DIN		ASA		
d	diameter (mm)	p	diameter pitch	$p = z/d$ (inch)
z	number of teeth	PD	pitch diameter	$PD = z/p$ (inch)
m	module $m = d/z$ (mm)	CP	circular pitch CP = 1 inch × π/p	
T	pitch $T = \pi \times m$ (mm)			

Figure 8 Toothed Wheel Dimensions

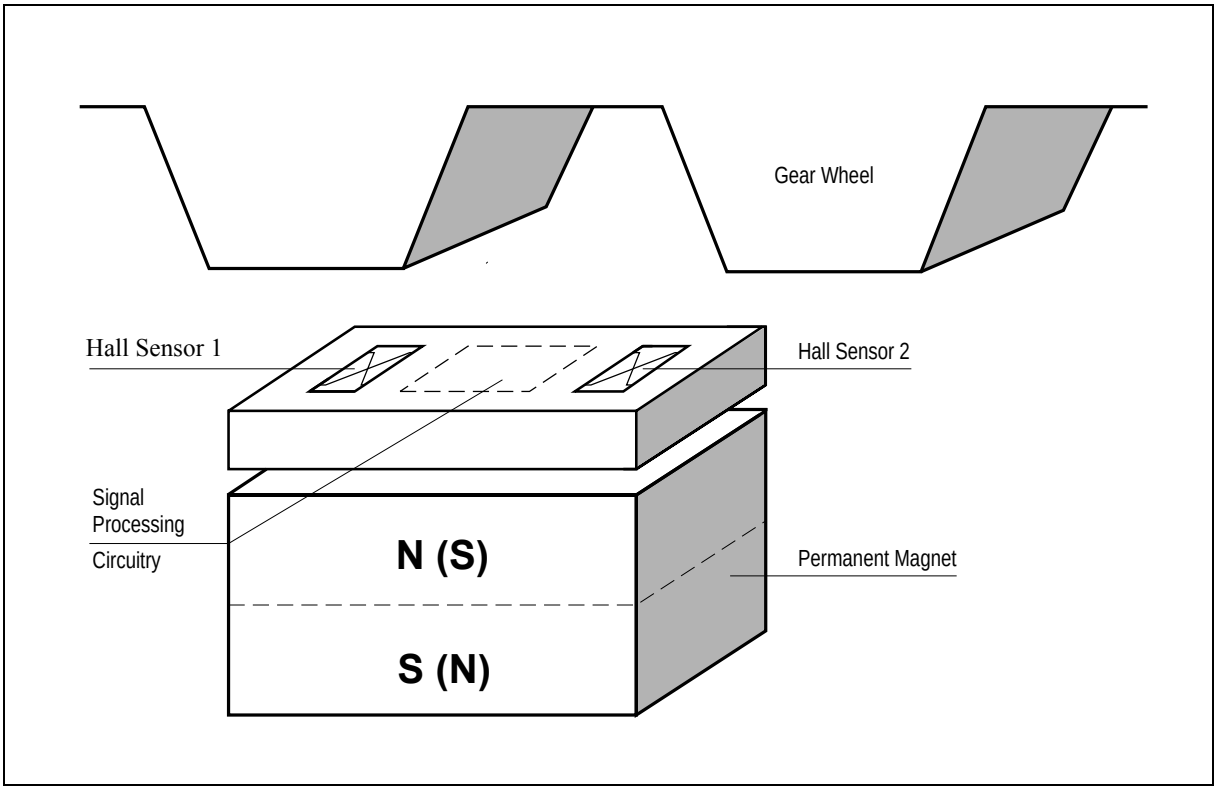


Figure 9 TLE 4926C, with Ferromagnetic Toothed Wheel

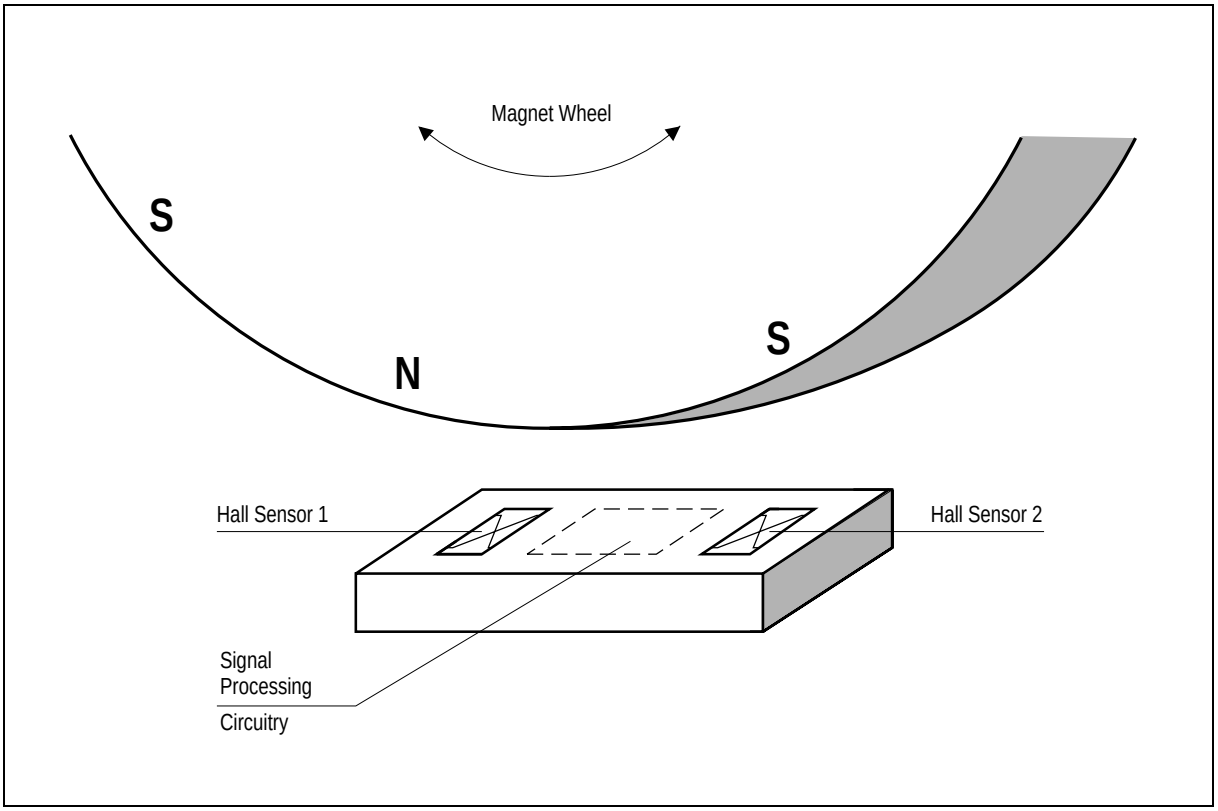


Figure 10 TLE4926C, with Magnet Wheel

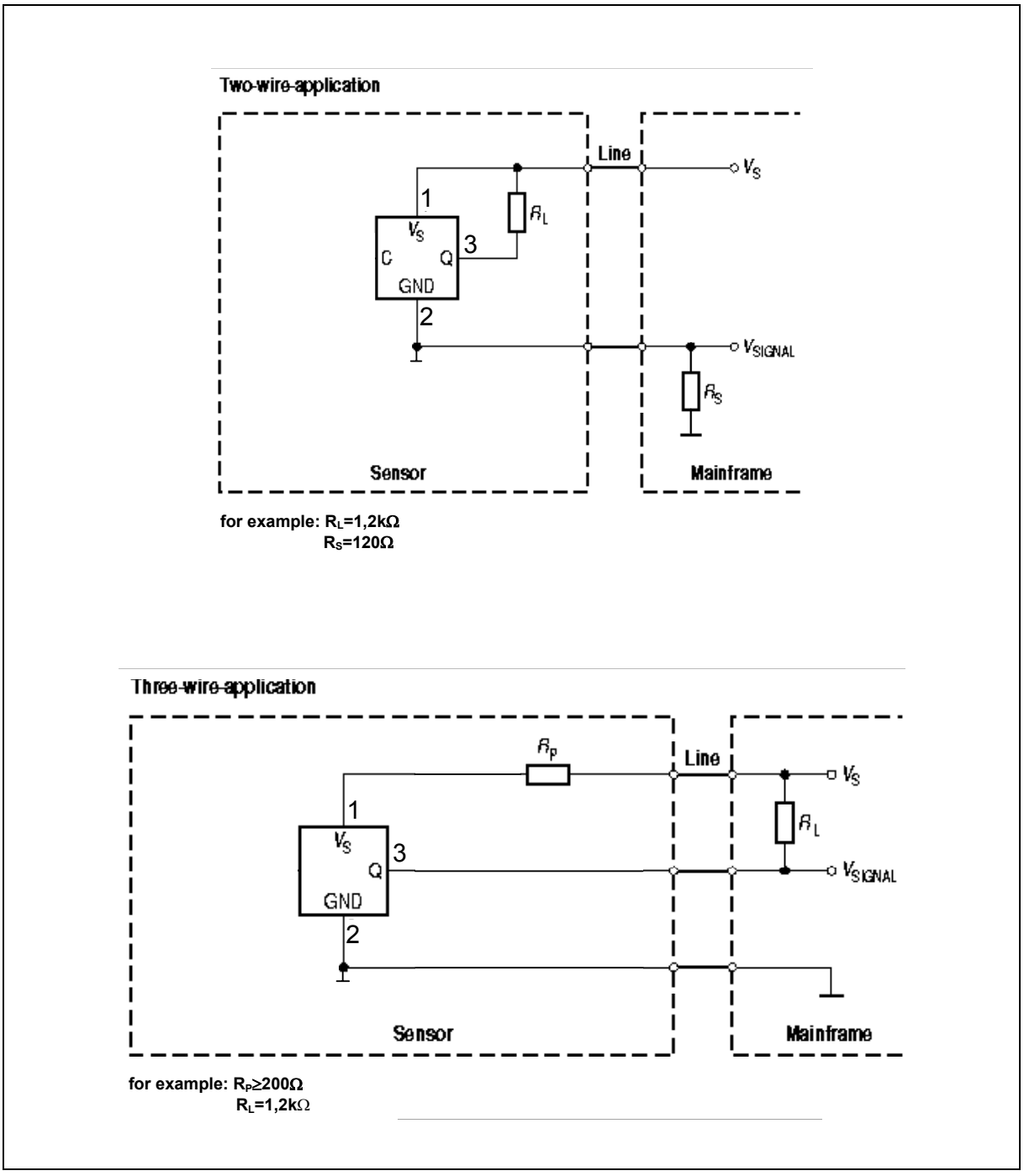


Figure 11 Application Circuits TLE4926C

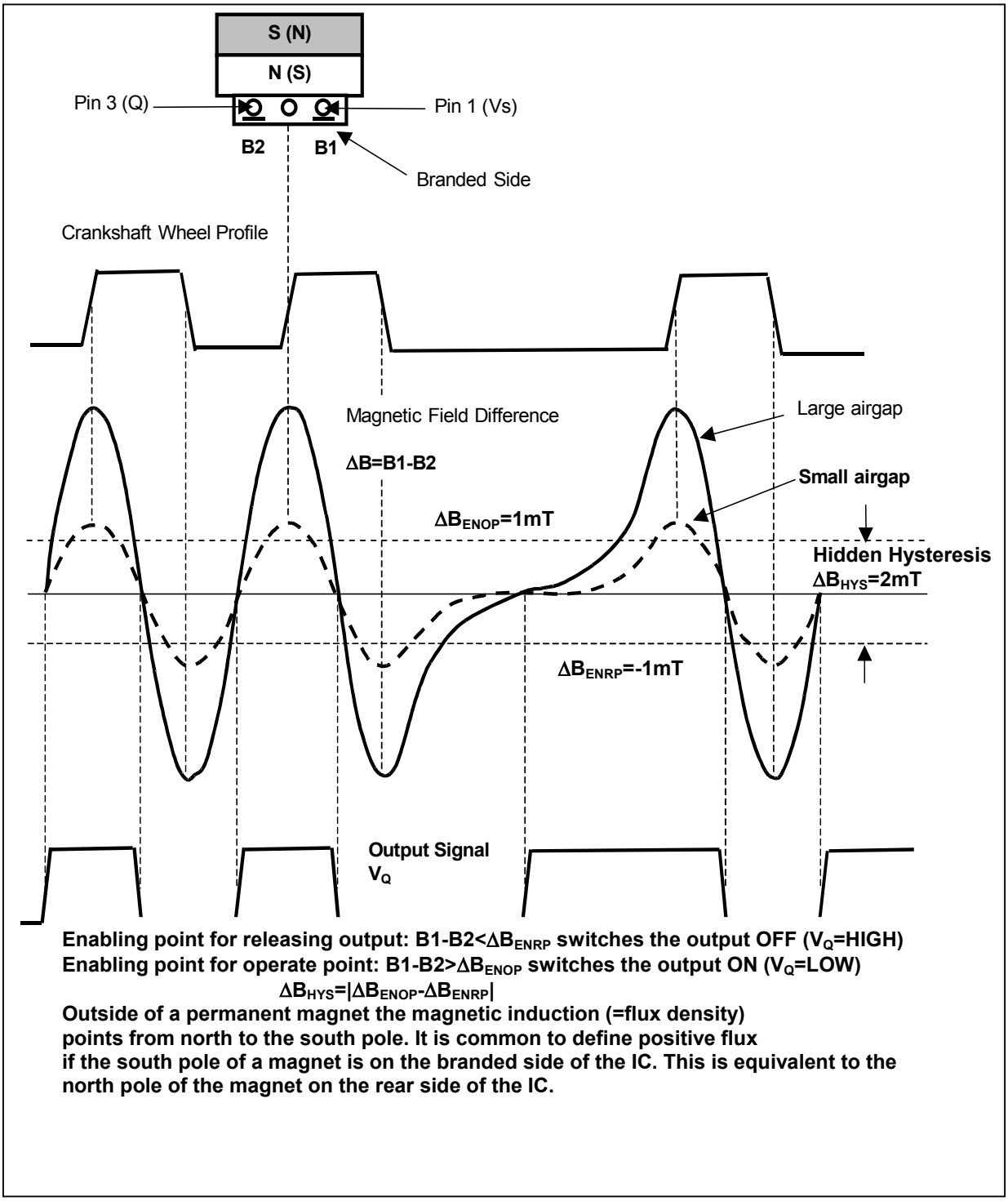


Figure 12 System Operation with hidden hysteresis

PG-SSO-3-91
(**P**lastic **S**ingle **S**mall **O**utline)

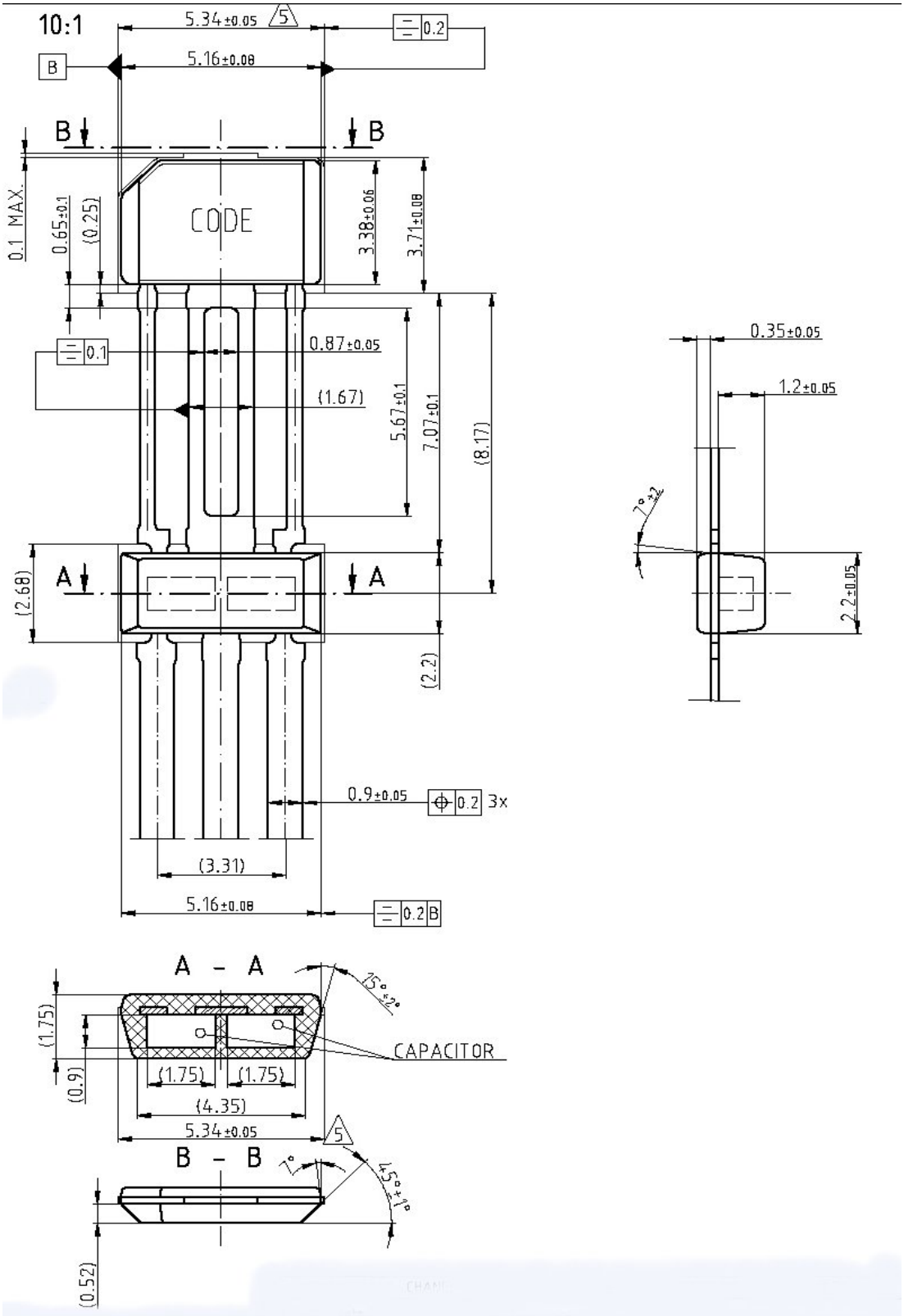


Figure 13 Package Dimensions (PG-SSO-3-91)

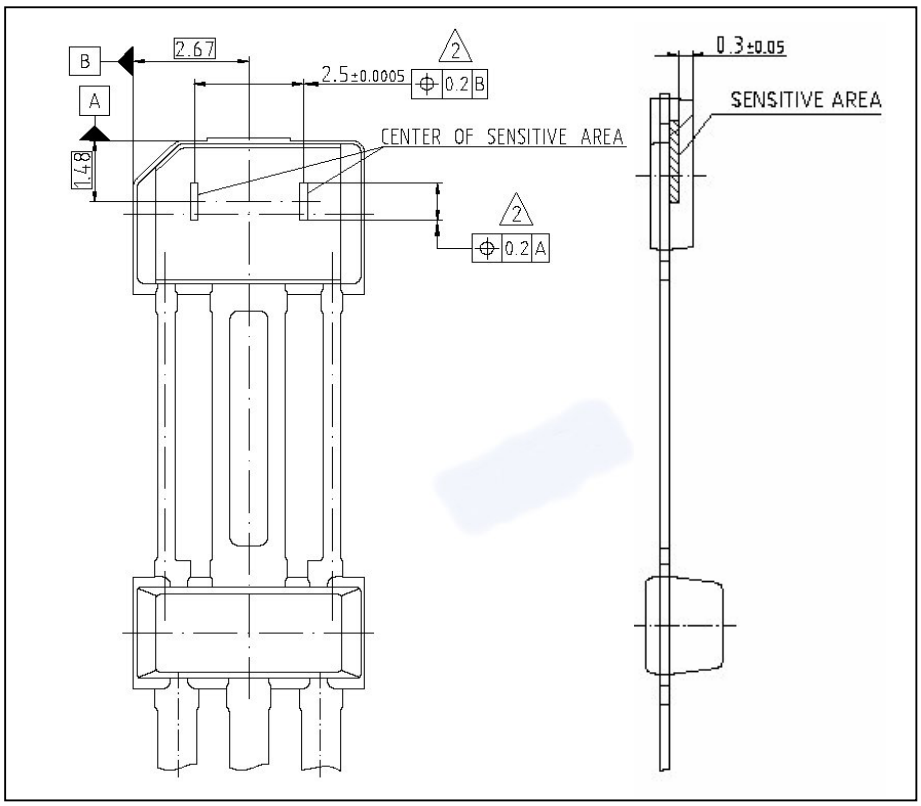


Figure 14 Hall probe spacing in the PG-SSO-3-91 package

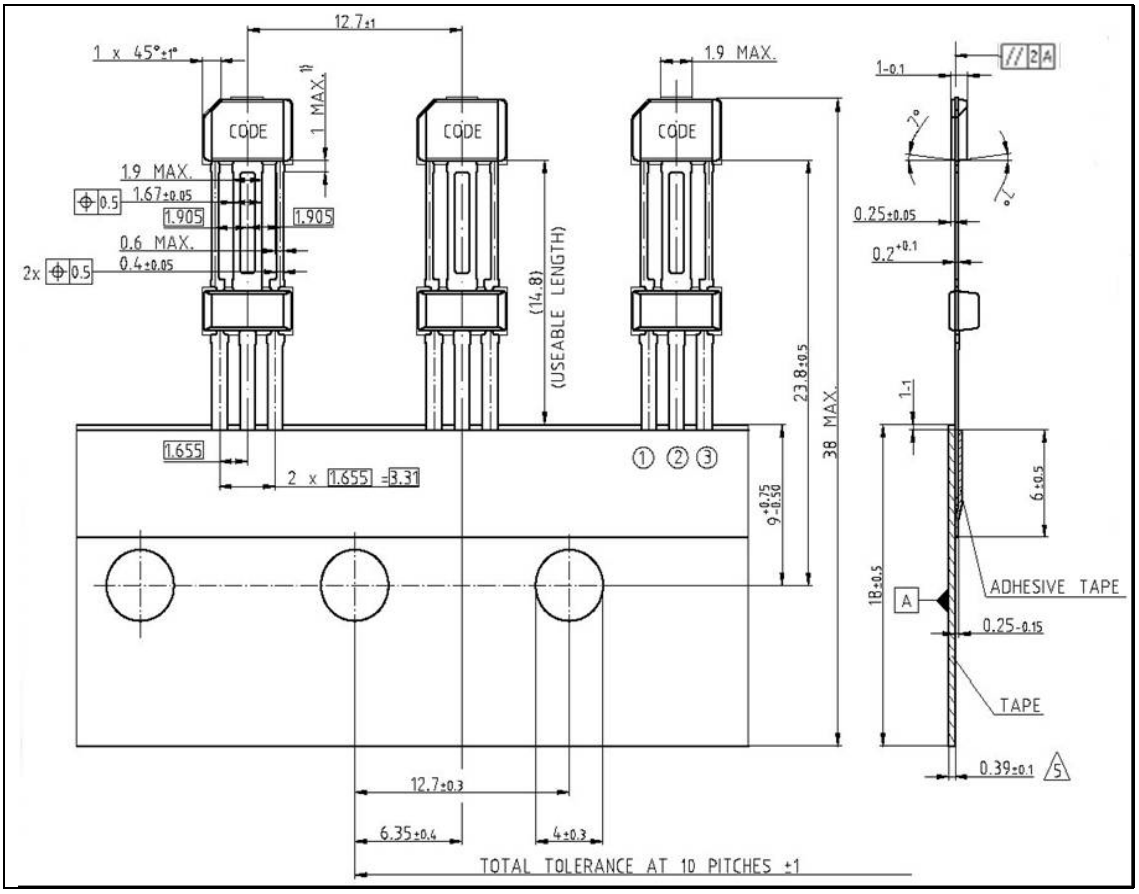


Figure 15 Tape Loading Orientation in the PG-SSO-3-91 package

Appendix:

Calculation of mechanical errors:

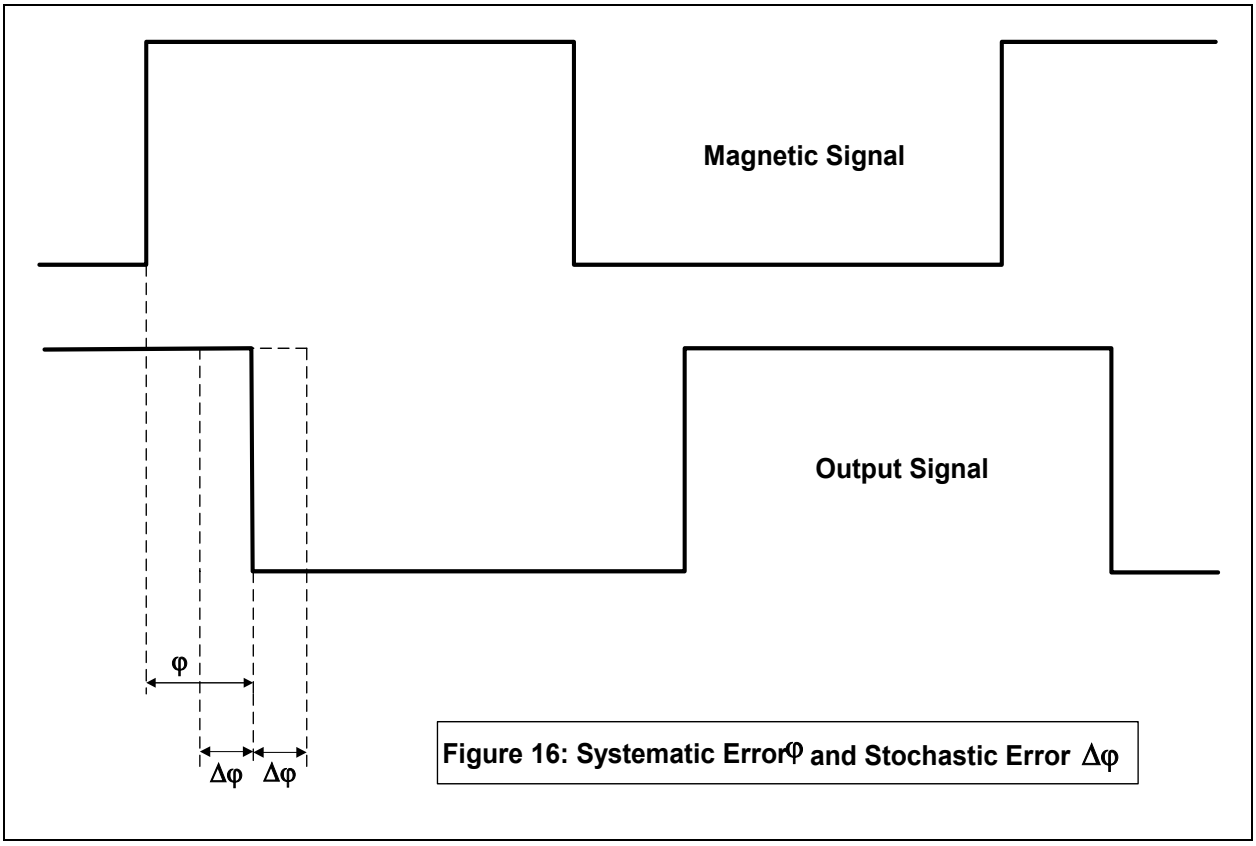


Figure 16: Systematic Error φ and Stochastic Error Δφ

Systematic Phase Error φ

The systematic error comes in because of the delay-time between the threshold point and the time when the output is switching. It can be calculated as follows:

$$\varphi = \frac{360° \bullet n}{60} \bullet t_d$$

φ ... systematic phase error in °
n ... speed of the camshaft-wheel in min^{-1}
t_d ... delay time (see specification) in *sec*

Systematic Phase Error Δφ

The systematic phase error includes the error due to the variation of the delay time with temperature and the error caused by the resolution of the threshold. It can be calculated in the following way:

$$\Delta\varphi_d = \frac{360° \bullet n}{60} \bullet \Delta t_d$$

$\Delta\varphi_d$ ... systematic phase error due to the variation of the delay time over temperature in °
n … speed of the camshaft wheel in *min*$^{-1}$
Δt_d … variation of delay time over temperature in *sec*

Jitter (Repeatability)

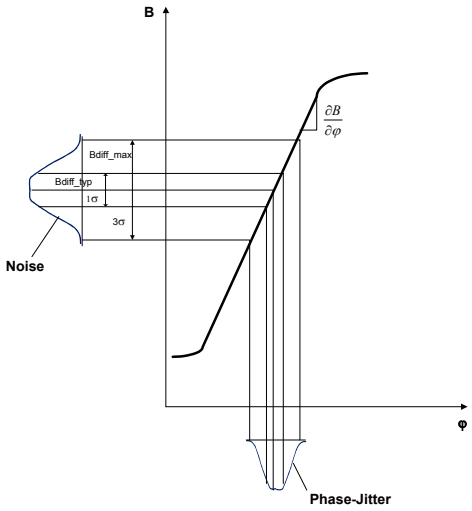


Figure17: Phase-Jitter

The phase jitter is normally caused by the analogue system noise. If there is an update of the offset-DAC due to the algorithm, what could happen after each tooth, then an additional step in the phase occurs (see description of the algorithm). This is not included in the following calculations. The noise is transformed through the slope of the magnetic edge into a phase error. The phase jitter is determined by the two formulas:

$$\varphi_{Jitter\_typ} = \frac{\partial\varphi}{\partial B} \bullet \left(B_{neff\_typ}\right)$$

$$\varphi_{Jitter\_\max} = \frac{\partial\varphi}{\partial B} \bullet \left(B_{neff\_\max}\right)$$

φ_{Jitter_typ} ... typical phase jitter at Tj=25°C in ° (1Sigma)
φ_{Jitter_max} ... maximum phase jitter at Tj=175°C in ° (3Sigma)
$\frac{\partial\varphi}{\partial B}$ ... inverse of the magnetic slope of the edge in °/*T*
B_{neff_typ} ... typical value of B_{diff} in *T* (1σ-value at Tj=25°C)
B_{neff_max} ... maximum value of B_{diff} in *T* (3σ-value at Tj=175°C)

Example:

Assumption:
$n = 4500\ min^{-1}$
$t_d = 14\ \mu s$
$\Delta t_d = \pm 3\ \mu s$
$\frac{\partial B}{\partial \varphi} = 3\ mT/°$
$B_{neff\_typ} = \pm 40\ \mu T$ (1σ-value at Tj=25°C)
$B_{neff\_max} = \pm 210\ \mu T$ (3σ-value at Tj=175°C)

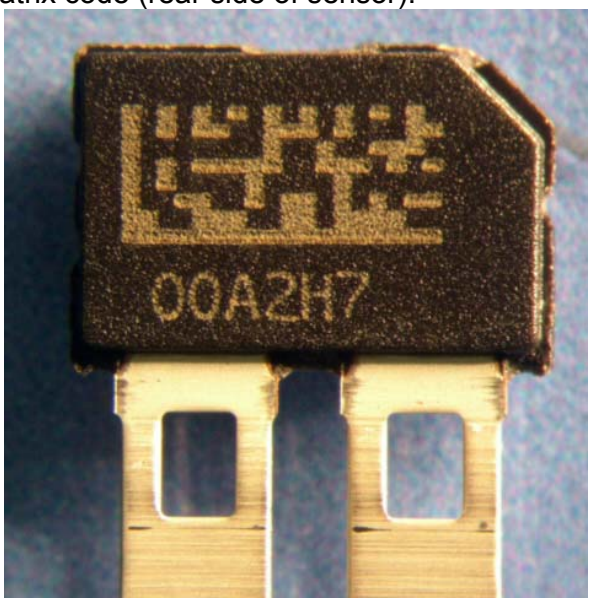
Calculation:

$\varphi = 0.378°$	...	systematic phase error
$\Delta\varphi_d = \pm 0.081°$	...	systematic phase error due to delay time variation
$\varphi_{Jitter\_typ} = \pm 0.013°$	...	typical phase jitter (1σ-value at Tj=25°C)
$\varphi_{Jitter\_max} = \pm 0.07°$	...	maximum phase jitter (3σ-value at Tj=175°C)

Appendix A: Marking & data matrix code information:

Product is RoHS (restriction of hadzardous substances) compliant when marked with letter “G” in front or after the date code marking.

As mentioned in information note N° **136/03** a data matrix code with 8x18 fields according to the ECC200 standard may be used for sensor production. Furthermore the marking technique on the front side of the device may be changed from a mask to a writing laser equipment. The information content (date code and device type) will hereby not be changed.
Please refer to your Key account team or regional sales responsible if you need further information.
Example for data matrix code (rear side of sensor):



Revision History: April 2007 Version 3.0

Previous Version: 2.1	
Page	Subjects (major changes since last revision)
1	Data sheet is valid for 8” products
1	Ordering code updated
6	Watchdog reset condition updated
8, 11	Output OFF voltage typing error corrected
9	EMC performance conducted pulses ISO7637-1 TP1 and TP5 updated
10	ESD performance updated
11	Footnote 2: Watchdog reset condition updated

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