Selectable Adjustable/Fixed Low dropout 300mA Linear Regulator

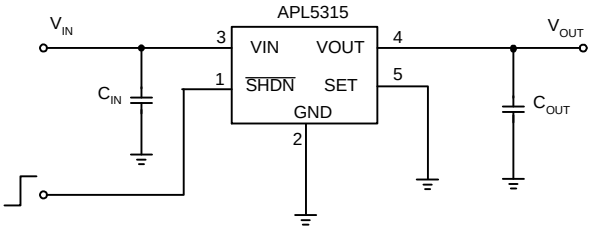
Features

- **Wide Operating Voltage: 2.7~6V**
- **Low Dropout Voltage:**

  230mV(typical) @ 300mA
- **Guaranteed 300mA Output Current**
- **Two Modes for Setting Output Voltage**

  - Fixed Output Voltage: 1~5V
  - Adjustable Output Voltage: 0.8~5.5V
- **Current Limit Protection with Foldback Current**
- **Internal Soft-Start**
- **Over Temperature Protection**
- **Stable with Low ESR Ceriamic Capacitor**
- **SOT-23-5 Package**
- **Lead Free Available (RoHS Compliant)**

Simplified Application Circuit



General Description

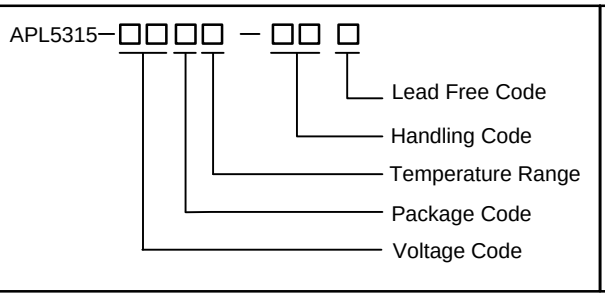
The APL5315 is a P-channel low dropout linear regulator which needs only one input voltage from 2.7~6V, and delivers current up to 300mA to set output voltage. It also can work with low ESR ceramic capacitors and is ideal for using in the battery-powered applications such as note-book computers, cellular phones. Typical dropout voltage is only 230mV at 300mA loading.

The APL5315 provides two kinds of output voltage operation modes for setting the output voltage. Fixed output voltage mode senses the output voltage on VOUT, adjustable output voltage mode needs two resistors as a voltage divider. Current limit with current foldback and thermal shutdown functions protect the device against current over-loads and over temperature. The APL5315 is available in a SOT-23-5 package.

Applications

- **Cellular Phones**
- **Portable and Battery-powered Equipment**
- **Notebook and Personal Computers**

Ordering and Marking Information



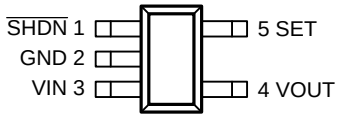
Package Code
B : SOT- 23-5
Operating Junction Temperature Range
I : -40 to 85°C
Handling Code
TR : Tape & Reel
Voltage Code
12 : 1.2V Blank: Adjustable
Lead Free Code
L : Lead Free Device

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldering operations. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

Product Name	Marking	Product Name	Marking	Product Name	Marking
APL5315	35RX	APL5315-12	355X	APL5315-15	359X
APL5315-18	35CX	APL5315-25	35JX	APL5315- 33	35RX (Note2)

Note1 : Other voltage version please contact ANPEC for detail.
Note2 : Because APL5315 and APL5315-33 are identical, the marking of APL5315 is same as APL5315-33.

Pin Configuration



SOT-23-5

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{IN}	VIN Supply Voltage (VIN to GND)	-0.3 ~ 6.5	V
$V_{\overline{SHND}}$	$\overline{SHND}$ Input Voltage ($\overline{SHND}$ to GND)	-0.3 ~ 6.5	V
P_D	Power Dissipation	Internally Limited	W
T_J	Junction Temperature	-40 ~ 150	℃
T_{STG}	Storage Temperature	-65 ~ 150	℃
T_{SDR}	Soldering Temperature, 10 Seconds	260	℃

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Thermal Resistance-Junction to Ambient (Note 3)	240	°C/W

Note3 : θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions

Symbol	Parameter	Range	Unit
V_{IN}	VIN Supply Voltage	2.7 ~ 6	V
V_{OUT}	Output Voltage	0.8 ~ 5.5	V
I_{OUT}	VOUT Output Current	0 ~ 300	mA
C_{OUT}	Output Capacitor	1.5 ~ 33	μF
T_J	Junction Temperature	-40 ~ 125	°C

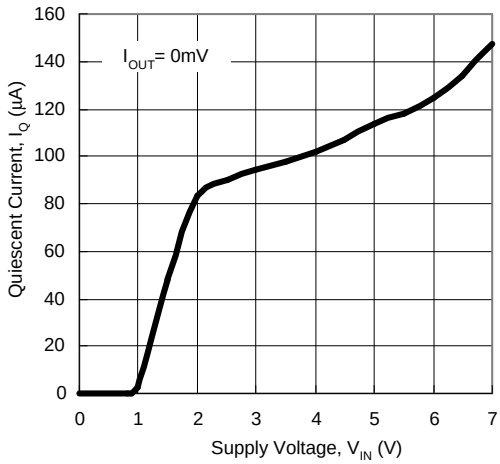
Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN} = V_{OUT}+1V (min V_{IN}=2.7V), I_{OUT}=0~300mA, C_{IN} = 1µF, C_{OUT} = 2.2µF, T_A = -40 to 85°C. Typical values are at T_A = 25°C.

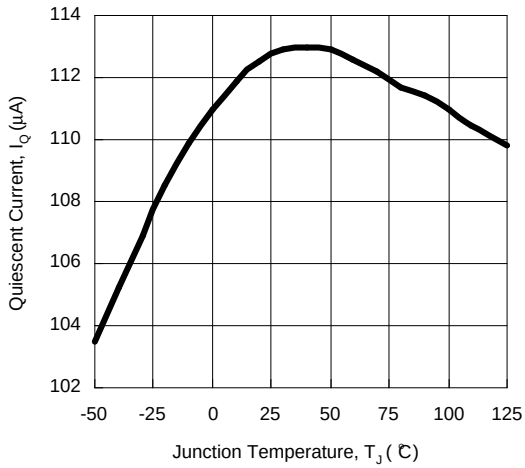
Symbol	Parameter	Test Condition	APL5315			Unit
			Min.	Typ.	Max.	
V_{IN}	Input Voltage		2.7	---	6	V
V_{OUT}	Output Voltage Range		0.8	---	5.5	V
	UVLO Threshold		1.5	2.3	2.6	V
	UVLO Hysteresis		---	0.8	---	V
I_Q	Quiescent Current	I_{OUT} =10mA ~300mA	---	120	160	µA
V_{REF}	Reference Voltage	Measured on SET, V_{IN}=2.7V, I_{OUT}=10mA	0.784	0.8	0.816	V
	Output Voltage Accuracy	Fixed output voltage, I_{OUT}=10mA	-2	---	+2	%
REG_{LINE}	Line Regulation	ΔV_{OUT}%/ΔV_{IN}, I_{OUT}=10mA	-0.06	---	+0.06	%/V
REG_{LOAD}	Load Regulation	ΔV_{OUT}%/ΔI_{OUT}	-0.2	---	+0.2	%/A
V_{DROP}	Dropout Voltage	V_{OUT} = 2.5V, I_{OUT} = 300mA	---	230	360	mV
		V_{OUT} = 3.3V, I_{OUT} = 300mA	---	170	300	
PSRR	Power Supply Ripple Rejection Ratio	f = 10kHz, I_{OUT} = 300mA	---	45	---	dB
	Noise	f = 80Hz to 100KHz, I_{OUT} = 300mA	---	160	---	μV_{RMS}
I_{LIMIT}	Current Limit		400	500	650	mA
I_{SHORT}	Foldback Current	V_{OUT} = 0V	---	80	---	mA
	$\overline{SHDN}$ Input Voltage High		1.6	---	---	V
	$\overline{SHDN}$ Input Voltage Low		---	---	0.4	
	Shutdown VIN Supply Current	$\overline{SHDN}$ = Low, V_{IN} = 6V	---	0.1	1	µA
	$\overline{SHDN}$ Pull Low Resistance		---	3	---	MΩ
	V_{OUT} Discharge MOSFET $R_{DS(ON)}$	$\overline{SHDN}$ = Low	---	60	---	Ω
	Over Temperature Threshold		---	160	---	℃
	Over Temperature Hysteresis		---	40	---	℃
	SET Input Threshold for Fixed/Adjustable Output Voltage Mode		---	100	---	mV
	SET input bias current	V_{SET}=0.8V	-100	---	100	nA
T_{SS}	Soft-Start Interval		60	80	100	µs

Typical Operating Characteristics

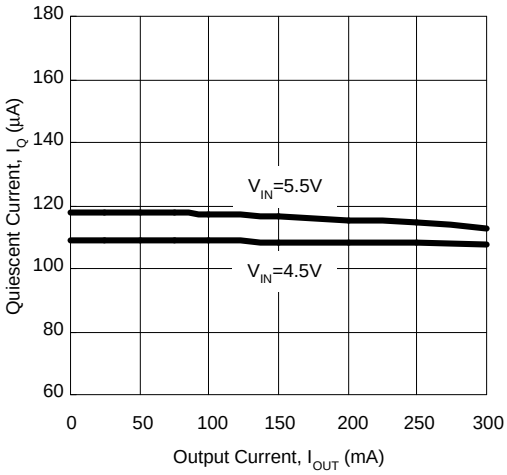
Quiescent Current vs. Supply Voltage



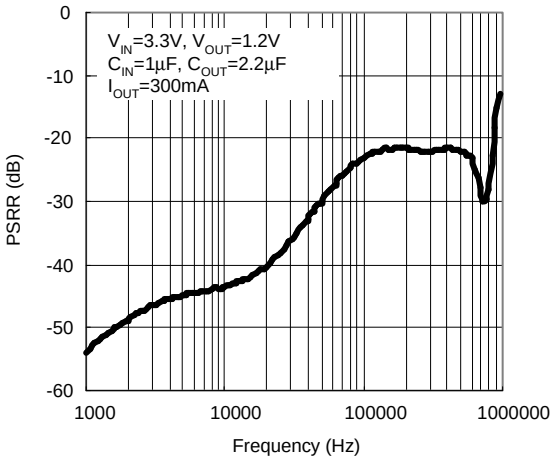
Quiescent Current vs. Junction Temperature



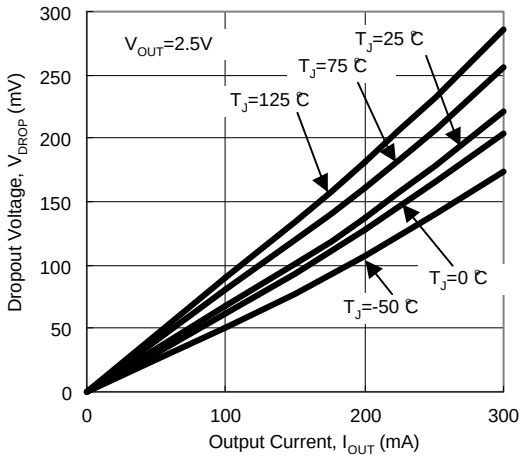
Quiescent Current vs. Output Current



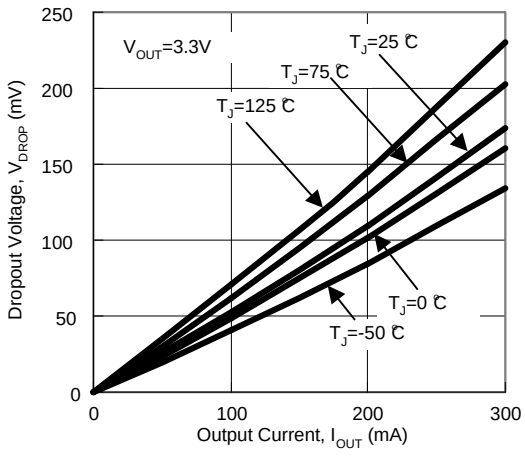
PSRR vs. Frequency



Dropout Voltage vs. Output Current

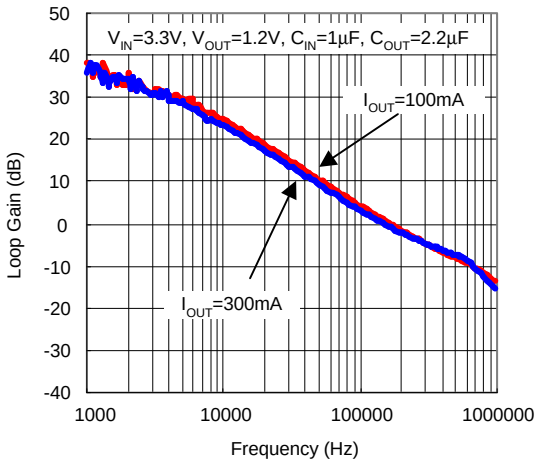


Dropout Voltage vs. Output Current

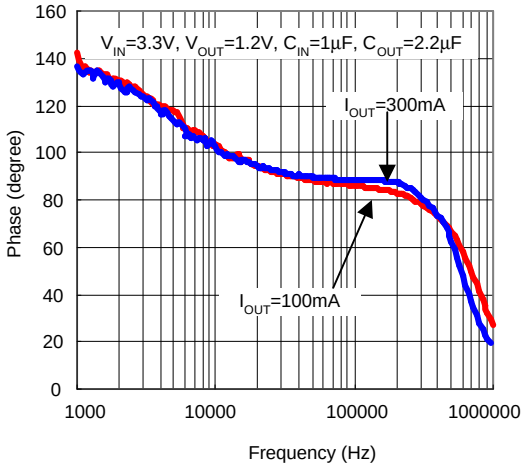


Typical Operating Characteristics (Cont.)

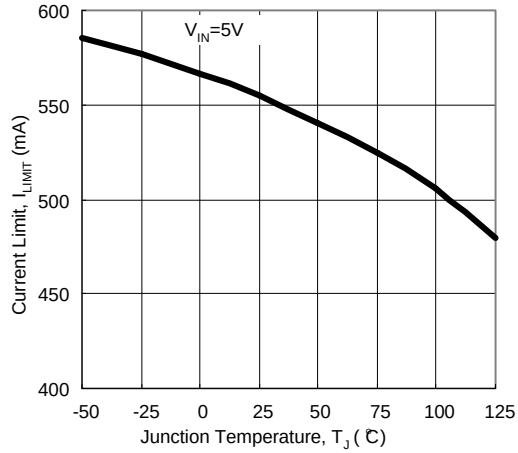
Loop Gain vs. Frequency



Phase vs. Frequency

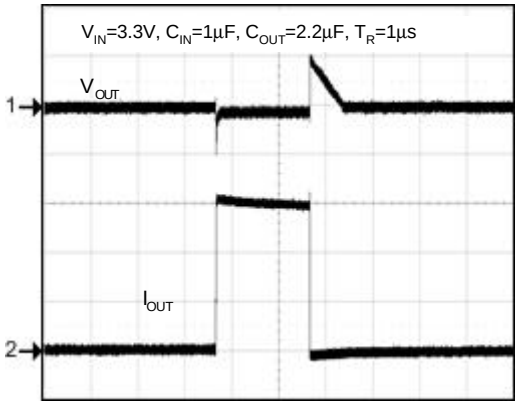


Current Limit vs. Junction Temperature



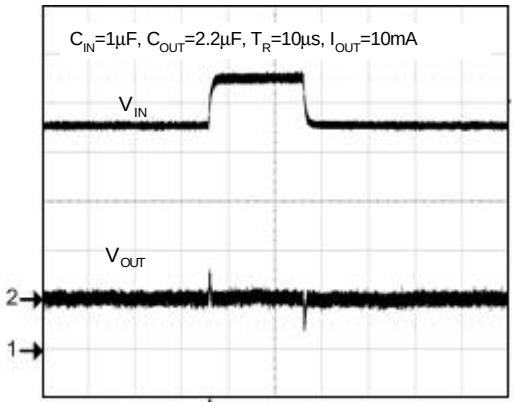
Operating Waveforms

Load Transient



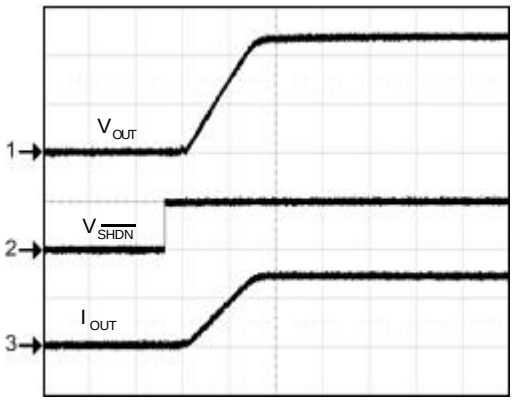
CH1 : V_{OUT}, 50mV/div, AC
CH2 : I_{OUT}, 100mA/div, DC
Time : 100µs/div

Line Transient



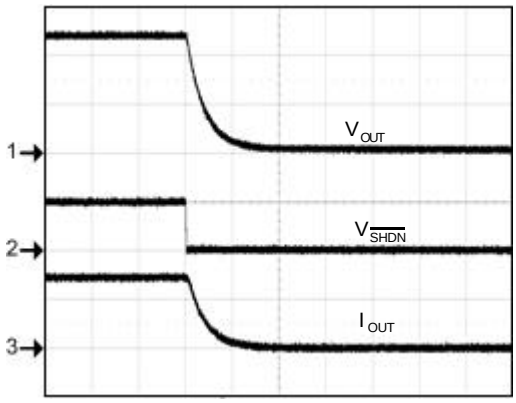
CH1 : V_{IN}, 1V/div, DC
CH2 : V_{OUT}, 20mV/div, AC
Time : 100µs/div

Enable



CH1 : V_{OUT}, 500mV/div
CH2 : $V_{\overline{SHDN}}$, 5V/div
CH3 : I_{OUT}, 200mA/div
Time : 50µs/div

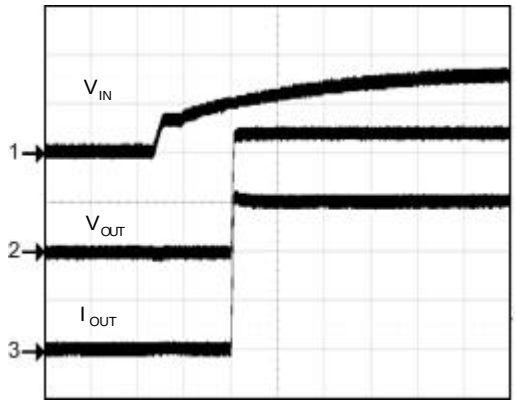
Shutdown



CH1 : V_{OUT}, 500mV/Div
CH2 : $V_{\overline{SHDN}}$, 5V/Div
CH3 : I_{OUT}, 200mA/Div DC
Time : 10µs/Div

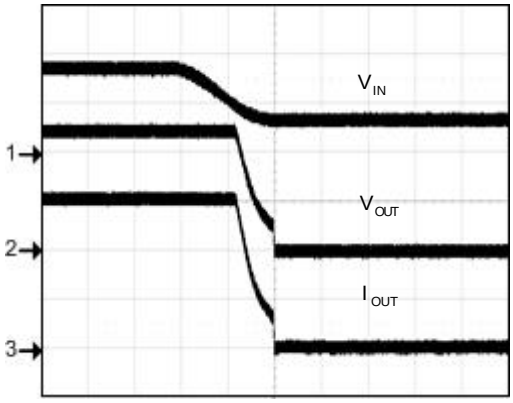
Operating Waveforms (Cont.)

Power on



CH1 : V_{IN}, 2V/div
CH2 : V_{OUT}, 500mV/div
CH3 : I_{OUT}, 100mA/div
Time : 200µs/Div

Power off

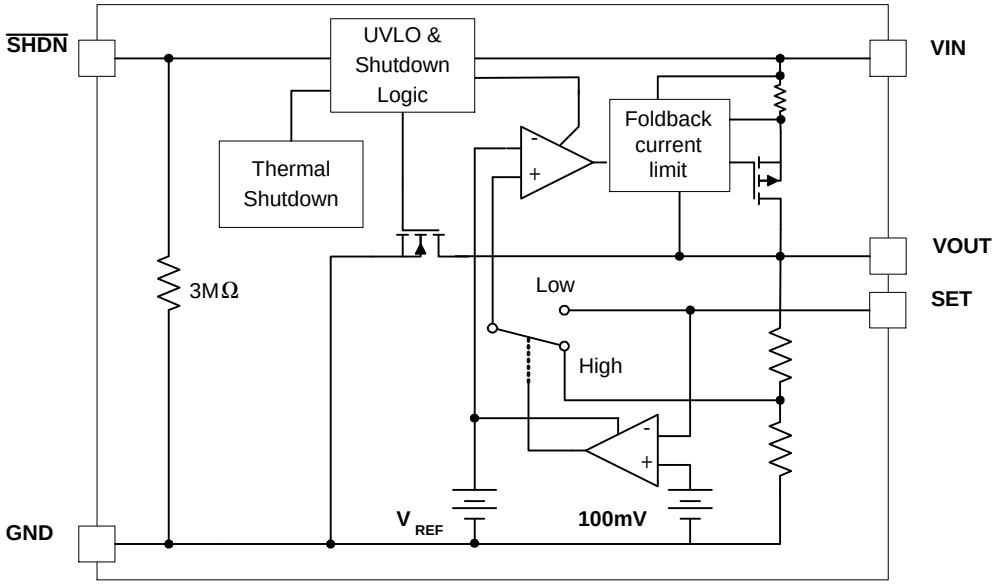


CH1 : V_{IN}, 2V/div
CH2 : V_{OUT},, 500mV/div,
CH3 : I_{OUT}, 100mA/div
Time : 50ms/Div

Pin Descriptions

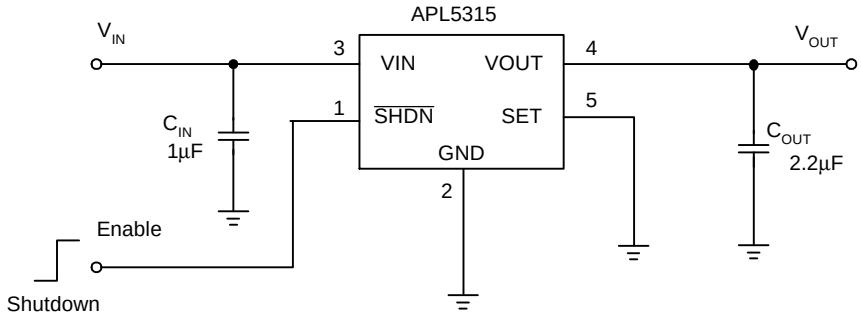
PIN		I/O	FUNCTION
No	NAME		
1	$\overline{SHDN}$	I	Shutdown control pin, logic high: enable; logic low: shutdown
2	GND		Ground pin
3	VIN	I	Voltage supply input pin
4	VOUT	O	Regulator output pin
5	SET	I	Connect this pin to ground for fixed output voltage operation. Connect this pin to an external resistor divider for adjustable output voltage mode operation.

Block Diagram



Typical Application Circuits

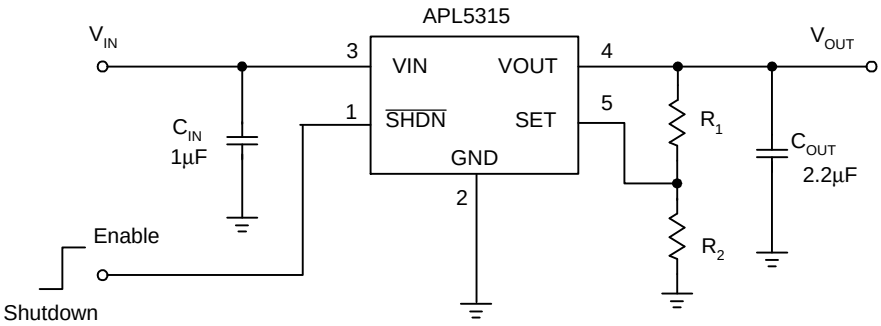
1. Fixed Output Voltage Mode



2.2µF/GRM155R60J225M Murata

Typical Application Circuits (Cont.)

2. Adjustable Output Voltage Mode



$$V_{OUT} = 0.8 \cdot \left(1 + \frac{R1}{R2}\right)$$

Functional Descriptions

Internal Soft-Start

An internal soft-start function controls rising rate of the output voltage to limit the surge current at start-up. The typical soft-start interval is about 80µs.

Output Voltage Regulation

The APL5315 can works in either fixed or adjustable mode by connecting the SET to GND or a resistor-divider which receives the feedback voltage of the regulator. The output voltage set by the resistor-divider is determined by:

$$V_{OUT} = 0.8 \cdot \left(1 + \frac{R1}{R2}\right)$$

Where R1 is connected from VOUT to SET with Kelvin sensing and R2 is connected from SET to GND. The recommended value of R2 is in the range of 100~100KΩ. An error amplifier working with a temperature compensated 0.8V reference and an output PMOS regulates the output to the presetting voltage. The error amplifier designed with high bandwidth and DC gain provides very fast transient response and less load regulation. It compares the reference with the feedback voltage and amplifies the difference to drive the output PMOS which provides load current from VIN to VOUT.

Thermal Shutdown

A thermal shutdown circuit limits the junction temperature of APL5315. When the junction temperature exceeds +160°C, a thermal sensor turns off the output PMOS, allowing the device to cool down. The regulator regulates the output again through initiation of a new soft-start cycle after the junction temperature cools by 40°C. The thermal shutdown designed with a 40°C hysteresis lowers the average junction temperature during continuous thermal overload conditions, extending life time of the device.

For normal operation, device power dissipation should be externally limited so that junction temperature will not exceed 125°C.

Under-Voltage Lock Out (UVLO)

The APL5315 monitors the input voltage to prevent wrong logic control. The UVLO function initiates a soft-start process after input voltage exceeds its rising UVLO threshold during power on. The UVLO function also shuts off the output when the input voltage falls below it's falling threshold. Typical UVLO hysteresis voltage is 0.8V.

Shutdown Control

The APL5315 has an active-low shutdown function. Force $\overline{SHDN}$ high (>1.6V) enables the V_{OUT}; force $\overline{SHDN}$ low (<0.4V) disables the V_{OUT}. $\overline{SHDN}$ is internally pulled low by a resistor (3MΩ typical). If it is not used, connect to VIN for normal operation.

Application Information

Input Capacitor

The APL5315 requires proper input capacitors to supply surge current during stepping load transients to prevent the input rail from dropping . Because the parasitic inductor from the voltage sources or other bulk capacitors to the VIN limit the slew rate of the surge current. Place the Input capacitors near VIN as close as possible. Input capacitors should be larger than 1μF and a minimum ceramic capacitor of 1μF is necessary.

Output Capacitor

The APL5315 needs a proper output capacitor to maintain circuit stability and to improve transient response over temperature and current. In order to insure the circuit stability, the proper output capacitor value should be larger than 2.2μF. With X5R and X7R dielectrics, 2.2μF is sufficient at all operating temperatures. Large output capacitor value can reduce noise and improve load-transient response and PSRR, however it also affects power on issue. Equation (1) shows the relationship between the maximum C_{OUT} value and V_{OUT}.

$$C_{OUT(max)} = 87 \cdot \left(0.55 - \frac{0.1155}{V_{OUT}}\right) \quad \text{.....(1)}$$

Where the unit of C_{OUT} is μF and V_{OUT} is V. Figure 1 shows the curve of maximum output capacitor over the output voltage. The output voltage range is from 0.8 to 5.5V and the output capacitor value should be under the line. Output capacitors must be placed at the load and ground pin as close as possible and the impedance of the layout must be minimized.

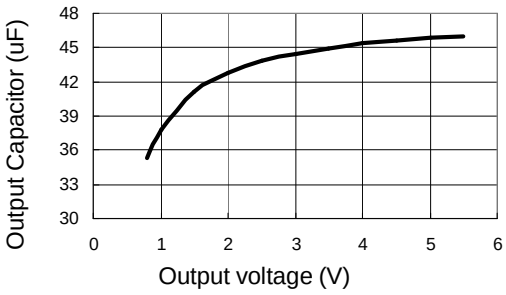


Figure 1

Operation Region and Power dissipation

The APL5315 maximum power dissipation depends on the thermal resistance and temperature difference between the die junction and ambient air. The power dissipation P_D across the device is:

$$P_D = (T_J - T_A) / \theta_{JA}$$

where (T_J-T_A) is the temperature difference between the junction and ambient air. θ_{JA} is the thermal resistance between Junction and ambient air. Assuming the T_A=25°C and maximum T_J=160°C (typical thermal limit threshold), the maximum power dissipation is calculated as:

$$P_{D(max)}=(160-25)/240 = 0.56(W)$$

For normal operation, do not exceed the maximum junction temperature rating of T_J = 125 °C. The calculated power dissipation should less than:

$$P_D=(125-25)/240 = 0.41(W)$$

The GND provides an electrical connection to ground and channels heat away. Connect the GND to ground by using a large pad or ground plane.

Layout Considerations

Figure 2 illustrates the layout. Below is a checklist for yours layout:

1. Please place the input capacitors close to the VIN.
2. Ceramic capacitors for load must be placed near the load as close as possible.
3. To place APL5315 and output capacitors near the load is good for performance.
4. Large current paths, the bold lines in figure 2, must have wide tracks.
5. Divider resistor R1 and R2 must be placed near the SET as close as possible.

Application Information (Cont.)

PCB Layout Consideration(Cont.)

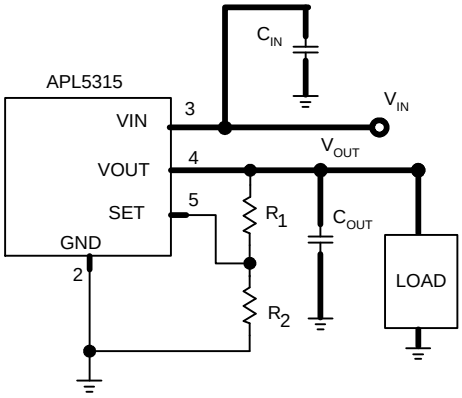
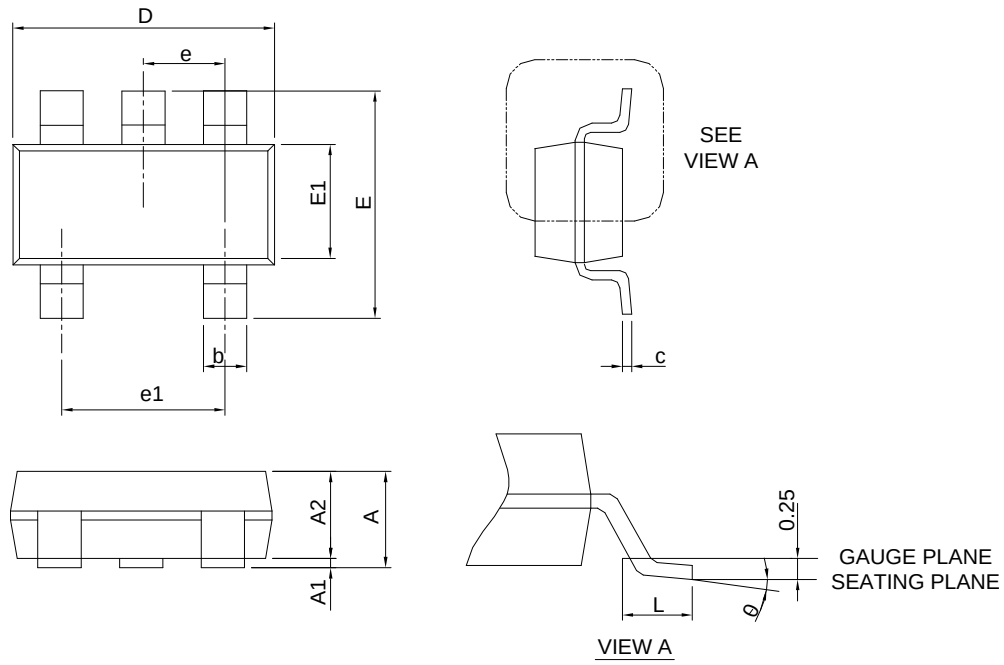


Figure 2

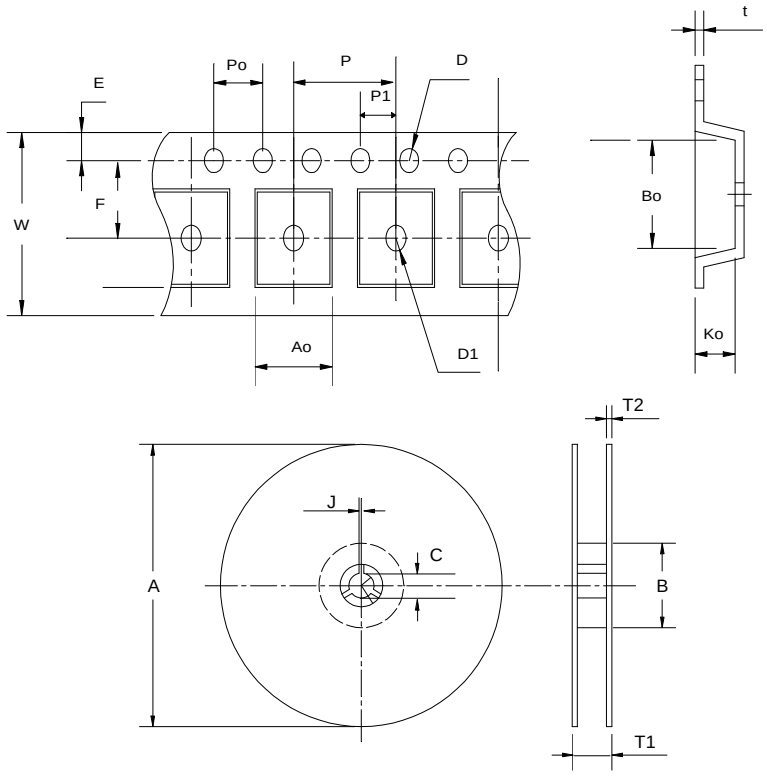
Package Information

SOT23-5



SYMBOL	SOT23-5			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.45		0.057
A1	0.00	0.15	0.000	0.006
A2	0.90	1.30	0.035	0.051
b	0.30	0.50	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.90 BSC		0.114 BSC	
E	2.80 BSC		0.110 BSC	
E1	1.60 BSC		0.063 BSC	
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

Carrier Tape & Reel Dimensions



Application	A	B	C	J	T1	T2	W	P	E
SOT-23-5	178 ±1	72 ± 1.0	13.0 + 0.2	2.5 ± 0.15	8.4 ± 2	1.5 ± 0.3	8.0 ± 0.3	4 ± 0.1	1.75± 0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	3.5 ± 0.05	1.5± 0.1	1.5± 0.1	4.0 ± 0.1	2.0 ± 0.1	3.15 ± 0.1	3.2± 0.1	1.4± 0.1	0.2±0.033

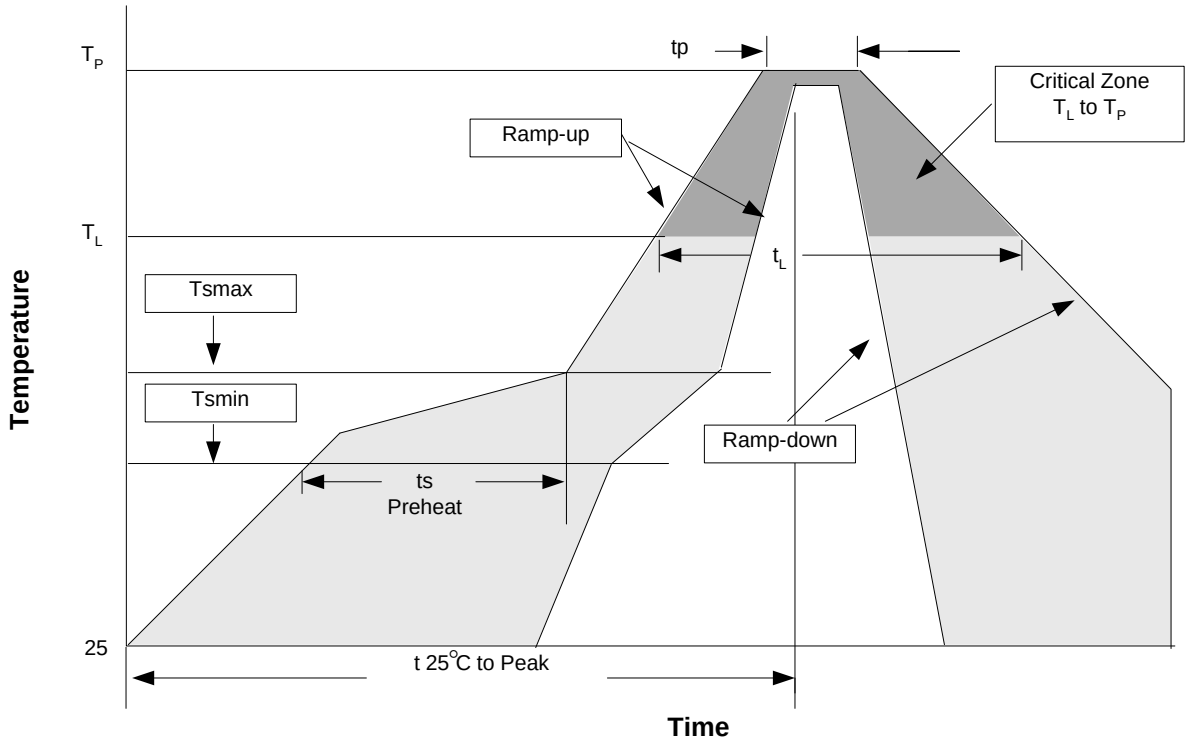
Cover Tape Dimensions

Application	Carrier Width	Cover Tape Width	Devices Per Reel
SOT23-5	8	5.3	3000

Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material: 90/10 or 63/37 SnPb), 100%Sn
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.

Reflow Condition (IR/Convection or VPR Reflow)



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classification Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Notes: All temperatures refer to topside of the package. Measured on the body surface.

Classification Reflow Profiles (Cont.)

Table 1. SnPb Entectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*
* Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.			

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B,A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1_{tr} > 100mA

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