TOSHIBA Digital Integrated Circuit   Silicon Monolithic

TC7WPN3125FK, TC7WPN3125FC

Low Voltage/Low Power 2-Bit Dual Supply Bus Buffer

The TC7WPN3125 is a dual supply, advanced high-speed CMOS 2-bit dual supply voltage interface bus buffer fabricated with silicon gate CMOS technology.

It is also designed with over voltage tolerant inputs and outputs up to 3.6 V.

Designed for use as an interface between a 1.2-V, 1.5-V, 1.8-V, or 2.5-V bus and a 1.8-V, 2.5-V or 3.6-V bus in mixed 1.2-V, 1.5-V, 1.8-V or 2.5-V/1.8-V, 2.5-V or 3.6-V supply systems.

The A-input interfaces with the 1.2-V, 1.5-V, 1.8-V or 2.5-V bus, the B-output with the 1.8-V, 2.5-V, 3.3-V bus.

The enable input ($\overline{\text{OE}}$) can be used to disable the device so that the signal lines are effectively isolated.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.
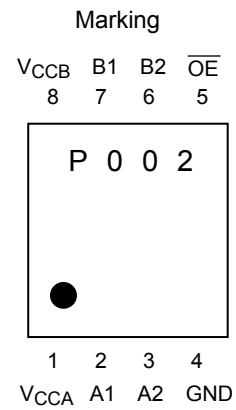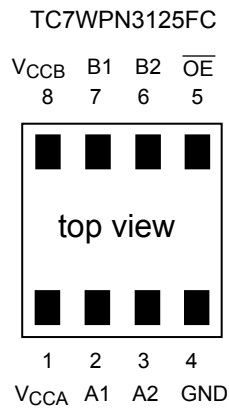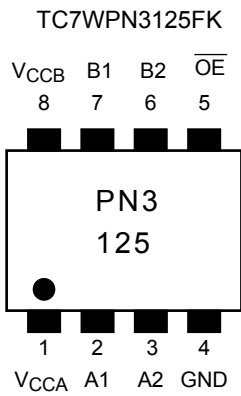
TC7WPN3125FK

SSOP8-P-0.50A

TC7WPN3125FC
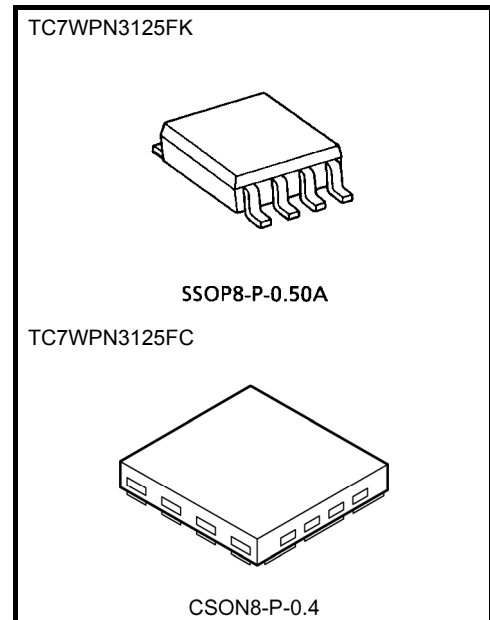
CSON8-P-0.4

Weight:
SSOP8-P-0.50A : 0.01 g (typ.)
CSON8-P-0.4   : 0.002 g (typ.)

Features

- Level converter for interfacing 1.2-V to 1.8-V, 1.2-V to 2.5-V, 1.2-V to 3.3-V, 1.5-V to 2.5-V, 1.5-V to 3.3-V, 1.8-V to 2.5-V, 1.8-V to 3.3-V or 2.5 V to 3.3-V system.

- High-speed operation : t_{pd} = 13.7 ns (max) (V_{CCA} = 2.5 ± 0.2 V, V_{CCB} = 3.3 ± 0.3 V)
  t_{pd} = 14.8 ns (max) (V_{CCA} = 1.8 ± 0.15 V, V_{CCB} = 3.3 ± 0.3 V)
  t_{pd} = 16.0 ns (max) (V_{CCA} = 1.5 ± 0.1 V, V_{CCB} = 3.3 ± 0.3 V)
  t_{pd} = 29 ns (max) (V_{CCA} = 1.2 ± 0.1 V, V_{CCB} = 3.3 ± 0.3 V)
  t_{pd} = 18.5 ns (max) (V_{CCA} = 1.8 ± 0.15 V, V_{CCB} = 2.5 ± 0.2 V)
  t_{pd} = 19.7 ns (max) (V_{CCA} = 1.5 ± 0.15 V, V_{CCB} = 2.5 ± 0.2 V)
  t_{pd} = 33 ns (max) (V_{CCA} = 1.2 ± 0.15 V, V_{CCB} = 2.5 ± 0.2 V)
  t_{pd} = 43 ns (max) (V_{CCA} = 1.2 ± 0.1 V, V_{CCB} = 1.8 ± 0.15 V)

- Output current : I_{OH}/I_{OL} = ±3 mA (min) (V_{CC} = 3.0 V)
  I_{OH}/I_{OL} = ±2mA (min) (V_{CC} = 2.3 V)
  I_{OH}/I_{OL} = ±0.5 mA (min) (V_{CC} = 1.65 V)

- Latch-up performance: −300 mA

- ESD performance: Machine model ≥ ±200 V
  Human body model ≥ ±2000 V

- Ultra-small package: CSON8(CST8), SSOP8(US8)

- Low current consumption : Using the new circuit significantly reduces current consumption when $\overline{\text{OE}}$ = "H".
  Suitable for battery-driven applications such as PDAs and cellular phones.

- 3.6-V tolerant function and power-down protection provided on all inputs and outputs.

Note: Do not apply a signal to any bus pins when it is in the output mode. Damage may result.
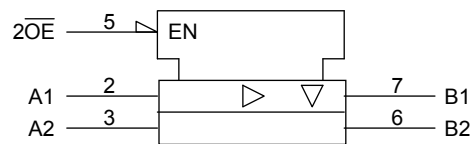
Pin Assignment (top view)

TC7WPN3125FK

V$_{CCB}$	B1	B2	$\overline{OE}$
8	7	6	5

PN3
125

1	2	3	4
V$_{CCA}$	A1	A2	GND

TC7WPN3125FC

V$_{CCB}$	B1	B2	$\overline{OE}$
8	7	6	5

top view

1	2	3	4
V$_{CCA}$	A1	A2	GND

Marking

V$_{CCB}$	B1	B2	$\overline{OE}$
8	7	6	5

P 0 0 2

1	2	3	4
V$_{CCA}$	A1	A2	GND

Truth Table

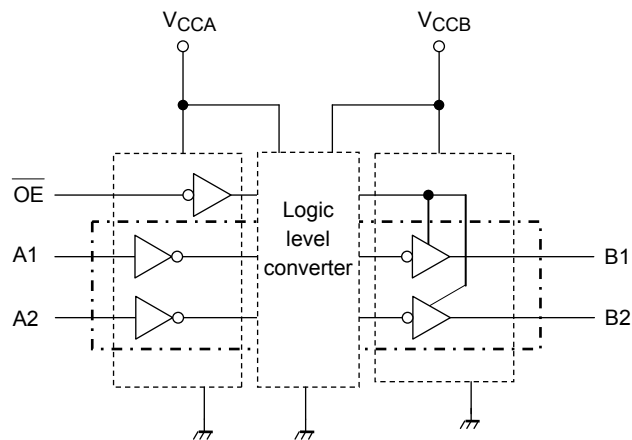| Inputs		Output
$\overline{OE}$	A1, A2	B1, B2
L	L	L
L	H	H
H	X	Z

X: Don't care

Z: High impedance

IEC Logic Symbol

Block Diagram

Absolute Maximum Ratings (Note 1)

Characteristics		Symbol	Rating	Unit
Power supply voltage (Note 2)		V_{CCA}	−0.5 to 4.6	V
		V_{CCB}	−0.5 to 4.6	
DC input voltage (An, $\overline{OE}$)		V_{IN}	−0.5 to 4.6	V
DC output voltage (Bn)		V_{OUT}	−0.5 to 4.6 (Note 3)	V
			−0.5 to V_{CCB} + 0.5 (Note 4)	
Input diode current		I_{IK}	−50	mA
Output diode current		I_{OK}	±50 (Note 5)	mA
DC output current		I_{OUTB}	±6	mA
DC V_{CC}/ground current per supply pin		I_{CCA}	±25	mA
		I_{CCB}	±50	
Power dissipation		P_D	150	mW
Storage temperature		T_{stg}	−65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: Don't supply a voltage to V_{CCB} pin when V_{CCA} is in the OFF state.

Note 3: Output in OFF state

Note 4: High or Low stats. I_{OUT} absolute maximum rating must be observed.

Note 5: $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

Operating Ranges (Note 1)

Characteristics		Symbol	Rating	Unit
Power supply voltage (Note 2)		V_{CCA}	1.1 to 2.7	V
		V_{CCB}	1.65 to 3.6	
Input voltage (An, $\overline{OE}$)		V_{IN}	0 to 3.6	V
Output voltage (Bn)		V_{OUTB}	0 to 3.6 (Note 3)	V
			0 to V_{CCB} (Note 4)	
Output current (Bn)		I_{OUTB}	±3 (Note 5)	mA
			±2 (Note 6)	
			±0.5 (Note 7)	
Operating temperature		T_{opr}	−40 to 85	°C
Input rise and fall time		dt/dv	0 to 10 (Note 8)	ns/V

Note 1: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Note 2: Don't use in $V_{CCA} > V_{CCB}$

Note 3: Output in OFF state

Note 4: High or low state

Note 5: V_{CCB} = 3.0 to 3.6 V

Note 6: V_{CCB} = 2.3 to 2.7 V

Note 7: V_{CCB} = 1.65 to 1.95 V

Note 8: V_{IN} = 0.8 to 2.0 V, V_{CCA} = 2.5 V, V_{CCB} = 3.0 V

Electrical Characteristics

DC Characteristics (1.1 V $\leqq$ V_{CCA} $\leqq$ 2.7 V , 1.65 V $\leqq$ V_{CCB} $\leqq$ 3.6 V)

Characteristics	Symbol	Test Condition		V_{CCA} (V)	V_{CCB} (V)	Ta = −40~85°C		Unit
						Min	Max	
H-level input voltage	V_{IHA}	V_{IN}		1.1$\leqq$$V_{CCA}$ <1.4	1.65 to 3.6	0.65 × V_{CCA}	—	V
				1.4$\leqq$$V_{CCA}$ <1.65	1.65 to 3.6	0.65 × V_{CCA}	—	V
				1.65$\leqq$$V_{CCA}$ <2.3	2.3 to 3.6	0.65 × V_{CCA}	—	V
				2.3$\leqq$$V_{CCA}$ $\leqq$2.7	2.7 to 3.6	1.6	—	V
L-level input voltage	V_{ILA}	V_{IN}		1.1$\leqq$$V_{CCA}$ <1.4	1.65 to 3.6	—	0.30 × V_{CCA}	V
				1.4$\leqq$$V_{CCA}$ <1.65	1.65 to 3.6	—	0.30 × V_{CCA}	V
				1.65$\leqq$$V_{CCA}$ <2.3	2.3 to 3.6	—	0.35 × V_{CCA}	V
				2.3$\leqq$$V_{CCA}$ $\leqq$2.7	2.7 to 3.6	—	0.7	V
H-level output voltage	V_{OHB}	$A_n = V_{IH}$	I_{OHB} = −100 μA	1.1 to 1.65	1.65 to 3.6	V_{CCB} − 0.2	—	V
			I_{OHB} = −0.5mA	1.1 to 1.4	1.65	1.25	—	
			I_{OHB} = −2 mA	1.1 to 2.3	2.3	1.7	—	
			I_{OHB} = −3 mA	1.1 to 3.0	3.0	2.2	—	
L-level output voltage	V_{OLB}	$A_n = V_{IL}$	I_{OLB} = 100 μA	1.1 to 1.65	1.65 to 3.6	—	0.2	V
			I_{OLB} = 0.5 mA	1.1 to 1.4	1.65	—	0.3	
			I_{OLB} = 2 mA	1.1 to 2.3	2.3	—	0.6	
			I_{OLB} = 3 mA	1.1 to 3.0	3.0	—	0.55	
3-state output OFF state current	I_{OZB}	$A_n = V_{IHA}$ or V_{ILA} $B_n = 0~3.6$ V		1.1 to 2.7	1.65 to 3.6	—	±2.0	μA
Input leakage current	I_{IN}	V_{IN} = 0~3.6 V		1.1 to 2.7	1.65 to 3.6	—	±1.0	μA
Power-off leakage current	I_{OFF1}	V_{IN}, B_n = 0~3.6 V		0	0	—	2.0	μA
	I_{OFF2}	$\overline{OE}$ = V_{CCA}		1.1 to 2.7	0	—	2.0	
	I_{OFF3}	A_n, B_n = 0~3.6 V		1.1 to 2.7	OPEN	—	2.0	
Quiescent supply current	I_{CCA}	V_{IN} = V_{CCA} or GND		1.1 to 2.7	1.65 to 3.6	—	2.0	μA
	I_{CCB}	V_{IN} = V_{CCA} or GND		1.1 to 2.7	1.65 to 3.6	—	2.0	
	I_{CCA}	V_{CCA} < V_{IN} $\leqq$ 3.6 V		1.1 to 2.7	1.65 to 3.6	—	±2.0	
	I_{CCB}	V_{IN}=V_{CCA} $V_{CCB}\leqq$ B_n $\leqq$ 3.6 V		1.1 to 2.7	1.65 to 3.6	—	±2.0	

AC Characteristics (Ta = −40 to 85°C, Input: $t_r = t_f = 2.0$ ns)

$V_{CCA} = 2.5 \pm 0.2$ V, $V_{CCB} = 3.3 \pm 0.3$ V

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time (An → Bn)	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.0	13.7	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{pZL} t_{pZH}	Figure 1, Figure 3	1.0	16.6	
3-state output disable time ($\overline{OE}$ → Bn)	t_{pLZ} t_{pHZ}	Figure 1, Figure 3	1.0	7.2	
Output to output skew	t_{osLH} t_{osHL}	(Note)	—	0.5	ns

Note: Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

$V_{CCA} = 1.8 \pm 0.15$ V, $V_{CCB} = 3.3 \pm 0.3$ V

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time (An → Bn)	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.0	14.8	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{pZL} t_{pZH}	Figure 1, Figure 3	1.0	18.9	
3-state output disable time ($\overline{OE}$ → Bn)	t_{pLZ} t_{pHZ}	Figure 1, Figure 3	1.0	8.7	
Output to output skew	t_{osLH} t_{osHL}	(Note)	—	0.5	ns

Note: Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

$V_{CCA} = 1.5 \pm 0.1$ V, $V_{CCB} = 3.3 \pm 0.3$ V

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time (An → Bn)	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.0	16.0	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{pZL} t_{pZH}	Figure 1, Figure 3	1.0	22.8	
3-state output disable time ($\overline{OE}$ → Bn)	t_{pLZ} t_{pHZ}	Figure 1, Figure 3	1.0	10.2	
Output to output skew	t_{osLH} t_{osHL}	(Note)	—	1.5	ns

Note: Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

$V_{CCA} = 1.2 \pm 0.1$ V, $V_{CCB} = 3.3 \pm 0.3$ V

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time (An → Bn)	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.0	29	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{pZL} t_{pZH}	Figure 1, Figure 3	1.0	63	
3-state output disable time ($\overline{OE}$ → Bn)	t_{pLZ} t_{pHZ}	Figure 1, Figure 3	1.0	23	
Output to output skew	t_{osLH} t_{osHL}	(Note)	—	1.5	ns

Note: Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

$V_{CCA} = 1.8 \pm 0.15$ V, $V_{CCB} = 2.5 \pm 0.2$ V

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time (An → Bn)	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.0	18.5	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{pZL} t_{pZH}	Figure 1, Figure 3	1.0	23.6	
3-state output disable time ($\overline{OE}$ → Bn)	t_{pLZ} t_{pHZ}	Figure 1, Figure 3	1.0	6.9	
Output to output skew	t_{osLH} t_{osHL}	(Note)	—	0.5	ns

Note: Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

$V_{CCA} = 1.5 \pm 0.1$ V, $V_{CCB} = 2.5 \pm 0.2$ V

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time (An → Bn)	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.0	19.7	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{pZL} t_{pZH}	Figure 1, Figure 3	1.0	26.6	
3-state output disable time ($\overline{OE}$ → Bn)	t_{pLZ} t_{pHZ}	Figure 1, Figure 3	1.0	8.3	
Output to output skew	t_{osLH} t_{osHL}	(Note)	—	1.5	ns

Note: Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

$V_{CCA} = 1.2 \pm 0.1$ V, $V_{CCB} = 2.5 \pm 0.2$ V

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time (An → Bn)	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.0	33	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{pZL} t_{pZH}	Figure 1, Figure 3	1.0	66	
3-state output disable time ($\overline{OE}$ → Bn)	t_{pLZ} t_{pHZ}	Figure 1, Figure 3	1.0	20	
Output to output skew	t_{osLH} t_{osHL}	(Note)	—	1.5	ns

Note: Parameter guaranteed by design.
$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$

$V_{CCA} = 1.2 \pm 0.1$ V, $V_{CCB} = 1.8 \pm 0.15$ V

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time (An → Bn)	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.0	43	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{pZL} t_{pZH}	Figure 1, Figure 3	1.0	78	
3-state output disable time ($\overline{OE}$ → Bn)	t_{pLZ} t_{pHZ}	Figure 1, Figure 3	1.0	20	
Output to output skew	t_{osLH} t_{osHL}	(Note)	—	1.5	ns

Note: Parameter guaranteed by design.
$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$

Capacitive Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Circuit		V_{CCA} (V)	V_{CCB} (V)	Typ.	Unit
Input capacitance		C_{IN}	An, $\overline{OE}$		2.5	3.3	7	pF
Output capacitance		C_{OUT}	Bn		2.5	3.3	8	pF
Power dissipation capacitance		C_{PDA}	/OE="L"		2.5	3.3	3	pF
			/OE="H"		2.5	3.3	0	
	(Note)	C_{PDB}	/OE="L"		2.5	3.3	13	
			/OE="H"		2.5	3.3	0	

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC\,(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per bit)}$$

AC Test Circuit
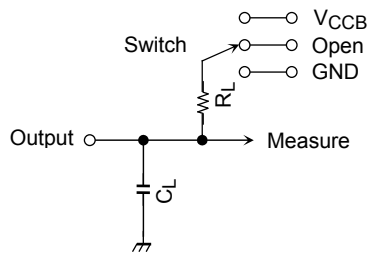
Parameter	Switch
t_{pLH}, t_{pHL}	Open
t_{pLZ}, t_{pZL}	V_{CCB}
t_{pHZ}, t_{pZH}	GND

Symbol	V_{CCB} (output)	
	3.3 ± 0.3 V 2.5 ± 0.2 V	1.8 ± 0.15 V
R_L	1 kΩ	1 kΩ
C_L	30 pF	30 pF

Figure 1

AC Waveform
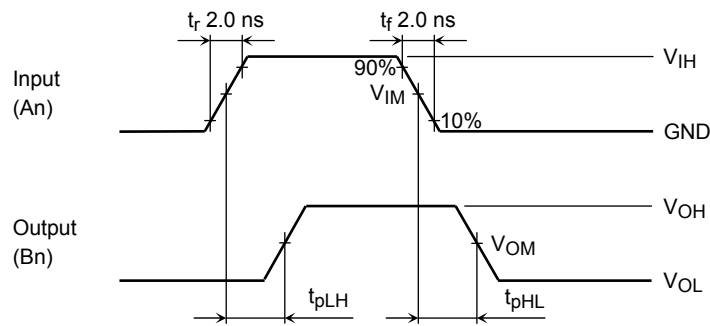
Figure 2 t_{pLH}, t_{pHL}
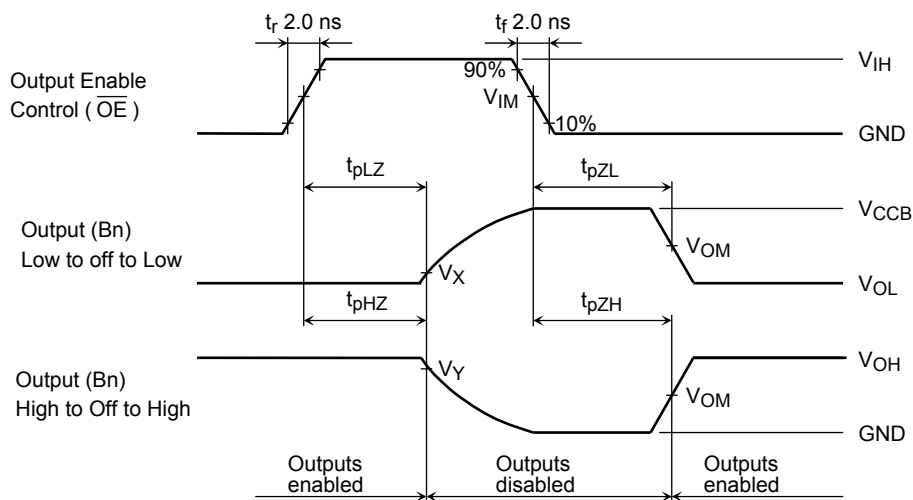
Figure 3 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

		V_{CCA} , V_{CCB}		
	Symbol	3.3 ± 0.3 V	2.5 ± 0.2 V 1.8 ± 0.15 V	1.5 ± 0.1 V 1.2 ± 0.1 V
Input	V_{IH}	-	V_{CCA}	V_{CCA}
	V_{IM}	-	$V_{CCA}/2$	$V_{CCA}/2$
Output	V_{OM}	$V_{OH}/2$	$V_{OH}/2$	-
	V_X	$V_{OL} + 0.3$ V	$V_{OL} + 0.15$ V	-
	V_Y	$V_{OH} - 0.3$ V	$V_{OH} - 0.15$ V	-

2007-10-19

Package Dimensions

SSOP8-P-0.50A

Unit : mm
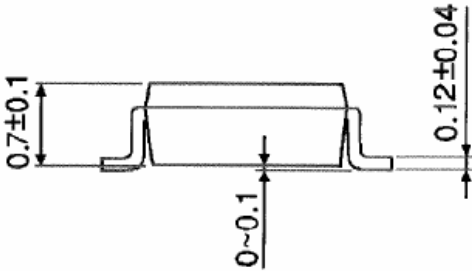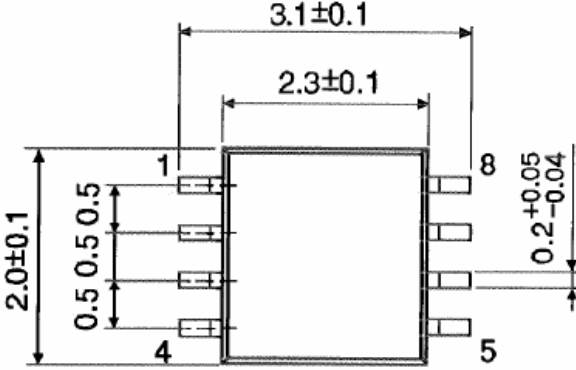
weight: 0.01 g (typ.)

Package Dimensions

CSON8-P-0.4   Unit: mm
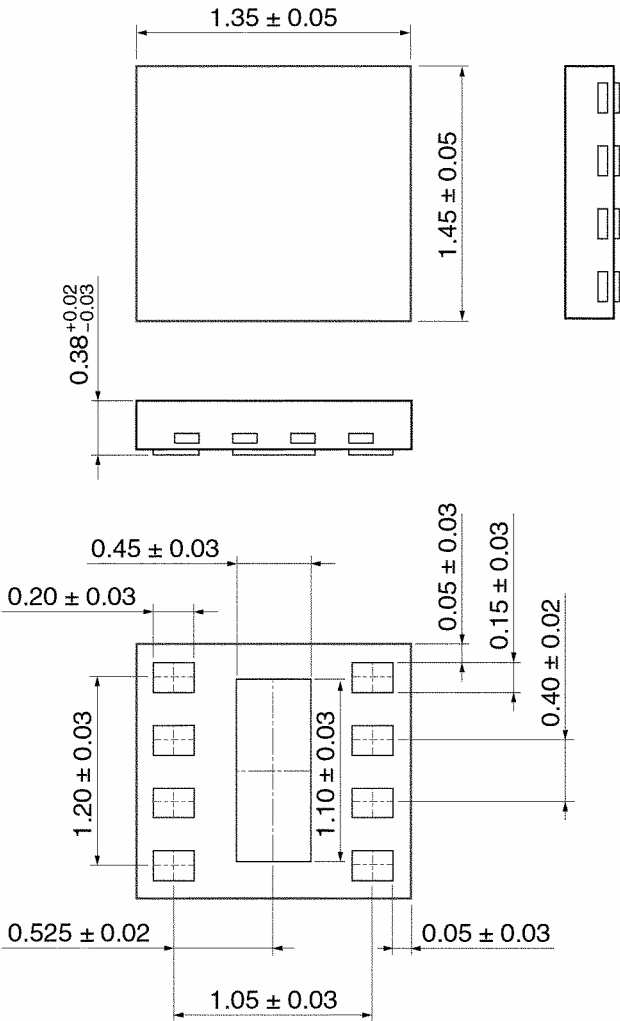
Weight: 0.002 g (typ.)

RESTRICTIONS ON PRODUCT USE