SC1404
Mobile Multi-Output PWM Controller with Virtual Current Sense™

POWER MANAGEMENT

Description

The SC1404 is a multiple-output power supply controller designed for battery operated systems. The SC1404 provides synchronous rectified buck converter control for two power supplies. An efficiency of 95% can be achieved. The SC1404 uses Semtech's proprietary Virtual Current Sense™ technology along with external error amplifier compensation to achieve enhanced stability and DC accuracy over a wide range of output filter components while maintaining fixed frequency operation. The SC1404 also provides two linear regulators for system housekeeping. The 5V linear regulator takes its input from the battery; for efficiency, the output is switched to the 5V output when available. The 12V linear regulator output is generated from a coupled inductor off the 5V switching regulator.

Control functions include: power up sequencing, soft start, power-good signaling, and frequency synchronization. Line and load regulation is to +/-1% of the output voltage. The internal oscillator can be adjusted to 200 kHz or 300 kHz or synchronized to an external clock. The mosfet drivers provide >1A peak drive current for fast mosfet switching.

The SC1404 includes a PSAVE# input to select pulse skipping mode for high efficiency at light load, or fixed frequency mode for low noise operation.

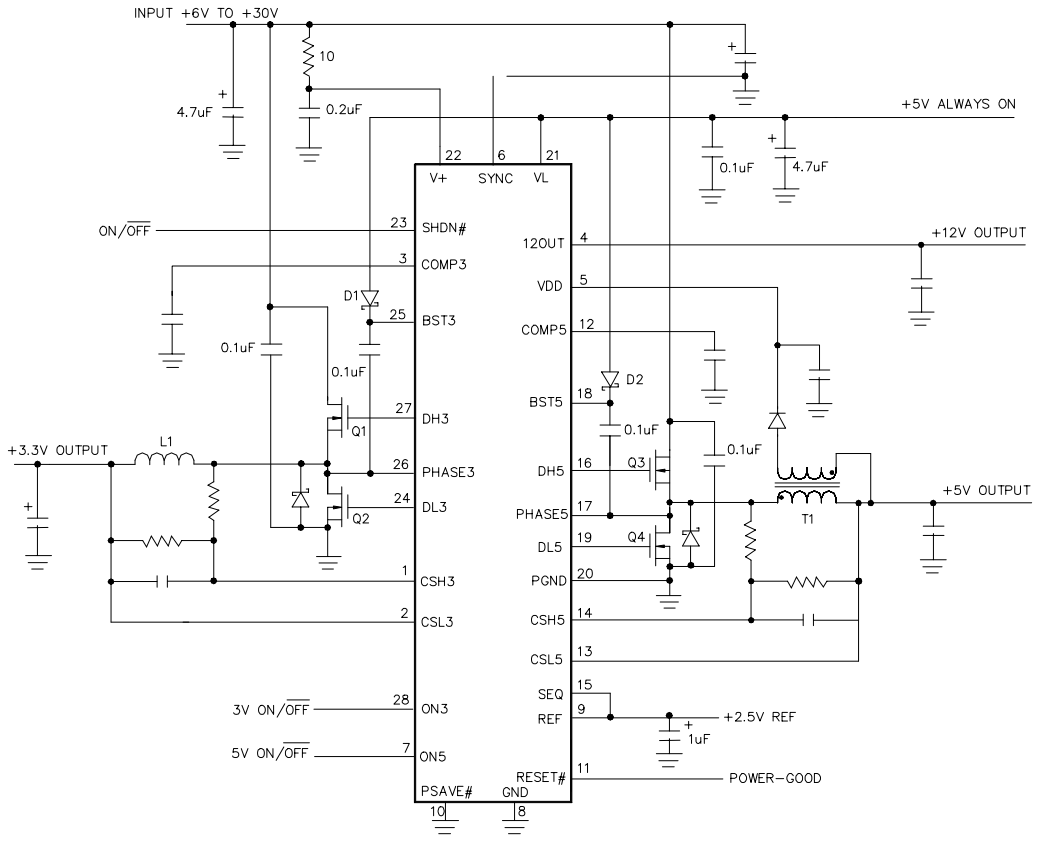
Features

- 6 to 30V input range (operation possible below 6V)
- 3.3V and 5V dual synchronous outputs
- Fixed-frequency or PSAVE for maximum efficiency over wide load current range
- 5V/50mA linear regulator
- 12V/200mA linear regulator
- Virtual Current Sense™ for enhanced stability
- Accurate low-loss current limiting
- Out-of-phase switching reduces input capacitance
- External compensation supports wide range of output filter components for reduced cost
- Programmable power-up sequence
- Power Good output
- Output overvoltage & overcurrent protection with output undervoltage shutdown
- 4µA typical shutdown current
- 6mW typical quiescent power

Applications

- Notebook and Subnotebook Computers
- Automotive Electronics
- Desktop DC-DC Converters

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

PARAMETER	DESCRIPTION	MAXIMUM	UNITS
VDD, V+, PHASE3, PHASE5 to GND	Supply and Phase Voltages	-0.3 to +30	V
PHASE3, PHASE5 to GND	Phase Voltages	-2.0 (transient - 100 nsec)	V
BST3, BST5, DH3, DH5 to GND	Boost voltages	-0.3 to +36	V
PGND to GND	Power Ground to Signal Ground	± 0.3	V
VL to GND	Logic Supply	-0.3 to +6	V
BST3 to PHASE3; BST5 to PHASE5;	High-side Gate Drive Supply	-0.3 to +6	V
DH3 to PHASE3; DH5 to PHASE5	High-side Gate Drive Outputs	-0.3 to (+BSTx + 0.3)	V
DL3, DL5 to GND CSL5, CSH5, CSL3, CSH3 to GND	Low-side Gate Drive Outputs and Current Sense inputs	-0.3 to +(VL + 0.3)	V
REF, SYNC, SEQ, PSAVE#, ON5, RESET#, VL, FB3, FB5, COMP3, COMP5 to GND	Logic inputs/outputs	-0.3 to +(VL + 0.3)	V
ON3, SHDN# to GND		-0.3 to +(V+ + 0.3V)	V
VL, REF Short to GND		Continuous	
REF Current		+5	mA
VL Current		+50	mA
12OUT to GND		-0.3 to (+VDD + 0.3)	V
12OUT Short to GND		Continuous	
12OUT Current	12V output current	+200	mA
T_J	Junction Temperature Range	+150	°C
Package Thermal Resistance	junction to ambient	76	°C/Watt
T_S	Storage Temperature Range	-65 to +200	°C
T_L	Lead Temperature	+300 °C, 10 second max.	°C

Electrical Characteristics

Unless otherwise noted: V+ = 15V, both PWMs on, SYNC = 0V, VL load = 0mA, REF load = 0mA, PSAVE# = 0V, T_A=-40 to 85°C.
Typical values are at T_A = +25°C. Circuit = Typical Application Circuit

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
MAIN SMPS CONTROLLERS					
Input Voltage Range		6		30.0	V
3V Output Voltage	V+ = 6.0 to 30V, 3V load = 0A to current limit	3.23	3.3	3.37	V
5V Output Voltage	V+ = 6.0 to 30V, 5V load = 0A to current limit	4.9	5.0	5.1	V
Load Regulation	Either SMPS, 0A to current limit, PSAVE# = VL		-0.4		%
Line Regulation	Either SMPS, 6.0 < V+ < 30V, PSAVE# = VL		0.05		%/V

Electrical Characteristics Cont.

Unless otherwise noted: V+ = 15V, both PWMs on, SYNC = 0V, VL load = 0mA, REF load = 0mA, PSAVE# = 0V, T_A=-40 to 85°C.
Typical values are at T_A = +25°C. Circuit = Typical Application Circuit

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Current-Limit Thresholds (Note 2)	CSH_X - CSL_X (positive current) CSH_X - CSL_X (negative current)	40	55 -50	70	mV
Zero Crossing Threshold	CSH_X - CSL_X PSAVE# = 0V, not tested		5		mV
Soft-Start Ramp Time	From enable to 95% full current limit, with respect to f_{OSC}		512		clks
Oscillator Frequency	SYNC = VL SYNC = 0V	220 170	300 200	380 230	kHz
Maximum Duty Factor	SYNC = VL SYNC = 0V	92 94	94 96		%
SYNC Input High Pulse	Not tested		300		ns
SYNC Input Low Pulse Width	Not tested		300		
SYNC Rise/Fall Time	Not tested		200		
SYNC Input Frequency Range			240 - 350		kHz
Current-Sense Input Leakage Current	CSH3 = 3.3V, CSH5 = 5.0V		3	10	µA
ERROR AMP					
DC Loop Gain	From internal feedback node to COMP3/COMP5		18		V/V
Gain Bandwidth Product			8		MHz
Output Resistance	COMP3, COMP5		25		Kohms
INTERNAL REGULATOR AND REFERENCE					
VL Output Voltage	SHDN# = V+; 6V < V+ <30V, 0mA <I_{LOAD}< 30mA, ON3 = ON5 = 0V	4.6		5.25	V
VL Undervoltage Lockout Fault Threshold	Falling edge, hysteresis = 0.7V	3.5	3.7	4.1	
VL Switchover Lockout	Switchover at startup - rising edge		4.5		
REF Output Voltage	No external load	2.45	2.5	2.55	
REF Load Regulation	0µA < I_{LOAD} < 50µA			12.5	mV
	0mA < I_{LOAD} < 5mA			50	

Electrical Characteristics Cont.

Unless otherwise noted: V+ = 15V, both PWMs on, SYNC = 0V, VL load = 0mA, REF load = 0mA, PSAVE# = 0V, T_A =-40 to 85°C.
Typical values are at T_A = +25°C. Circuit = Typical Application Circuit

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
REF Sink Current	10mV rise in REF voltage		10		µA
REF Fault Lockout Voltage	Falling edge	1.8		2.2	V
V+ Operating Supply Current	VL switched over to VOUT5, 5V SMPS on, I_{LOAD5} = I_{LOAD3} = 0A, PSAVE# = 0V		10	50	µA
V+ Standby Supply Current	V+ = 6V to 30V, both SMPS off, PSAVE# = 0V; includes current into SHDN#		300		
V+ Shutdown Supply Current	V+ = 6V to 30V, SHDN# = 0V	-1	3	15	
Quiescent Power Consumption	SMPS enabled, No Load on SMPS		6		mW
FAULT DETECTION					
Overvoltage Trip Threshold	With respect to unloaded output voltage	7	10	15	%
Overvoltage Fault Propagation Delay	Output driven 2% above overvoltage trip V_{TH}		1.5		µs
Output Undervoltage Threshold	With respect to unloaded output voltage	65	75	85	%
Output Undervoltage Lockout Time	From each SMPS enabled, with respect to f_{OSC}	5000	6144	7000	clks
Thermal Shutdown Threshold	Typical hysteresis = 10°C		+150		°C
RESET#					
RESET# Trip Threshold	With respect to unloaded output voltage, falling edge; typical hysteresis = 1%	-12	-9	-5	%
RESET# Propagation Delay	Falling edge, output driven 2% below RESET# trip threshold		1.5		µs
RESET# Delay Time	With respect to f_{OSC}	27,000	32,000	37,000	clks
INPUTS AND OUTPUTS					
Logic Input Low Voltage	ON3, PSAVE#, ON5, SHDN#, SYNC (SEQ = REF)			0.6	V
Logic Input High Voltage	ON3, PSAVE#, ON5, SHDN#, SYNC (SEQ = REF)	2.4			V

Electrical Characteristics Cont.

Unless otherwise noted: V+ = 15V, both PWMs on, SYNC = 0V, VL load = 0mA, REF load = 0mA, PSAVE# = 0V, T_A=-40 to 85°C.
Typical values are at T_A = +25°C. Circuit = Typical Application Circuit

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current PSAVE#, ON5, SYNC	SEQ = REF	-1		+1	µA
Input Leakage Current ON3	ON3 = 15V	-2		+2	µA
Input Leakage Current SHDN#	SHDN# = 15V	-1	3	+10	µA
Logic Output Low Voltage	RESET#, ISINK = 4mA			0.4	V
Logic Output High Current	RESET# = 3.5V		1		mA
ON5 Pull-down Resistance	ON5, ON3 = 0V, SEQ = REF		100		ohms
Gate Driver Sink/Source Current	DL3, DH3, DL5, DH5, forced to 2.5V		1		A
Gate Driver On-Resistance	BST3 to DH3, DH3 to PHASE3, BST5 to DH5, DH5 to PHASE5, VL to DL3, DL3 to PGND, VL to DL5, DL5 to PGND		1.5	7	ohms
Non-Overlap Threshold	PHASE3, PHASE5, to GND		1.0		V
Shoot-through (Non-Overlap) Delay	DHx falling edge to DLx rising edge DLx falling edge to DHx rising edge (1V threshold on DHx and DLx, no external capacitance on DLx or DHx)	10 35	17 75	25 115	nsec
12V LINEAR REGULATOR					
VDD Shunt Threshold	Rising edge, hysteresis = 5%	17		21	V
VDD Shunt Current	VDD = 20V	5	10	30	mA
VDD Leakage Current	VDD = 5V, Standby mode			30	µA
12OUT Output Voltage	0mA < Load < 200mA	11.55	12.1	12.75	V
12OUT Current Limit	12OUT forced to 11V, VDD = 13V	200			mA
12OUT Regulation Threshold	Falling edge		11.9		V
Quiescent VDD Current	VDD = 18V, run mode, no 12OUT load		80	100	µA

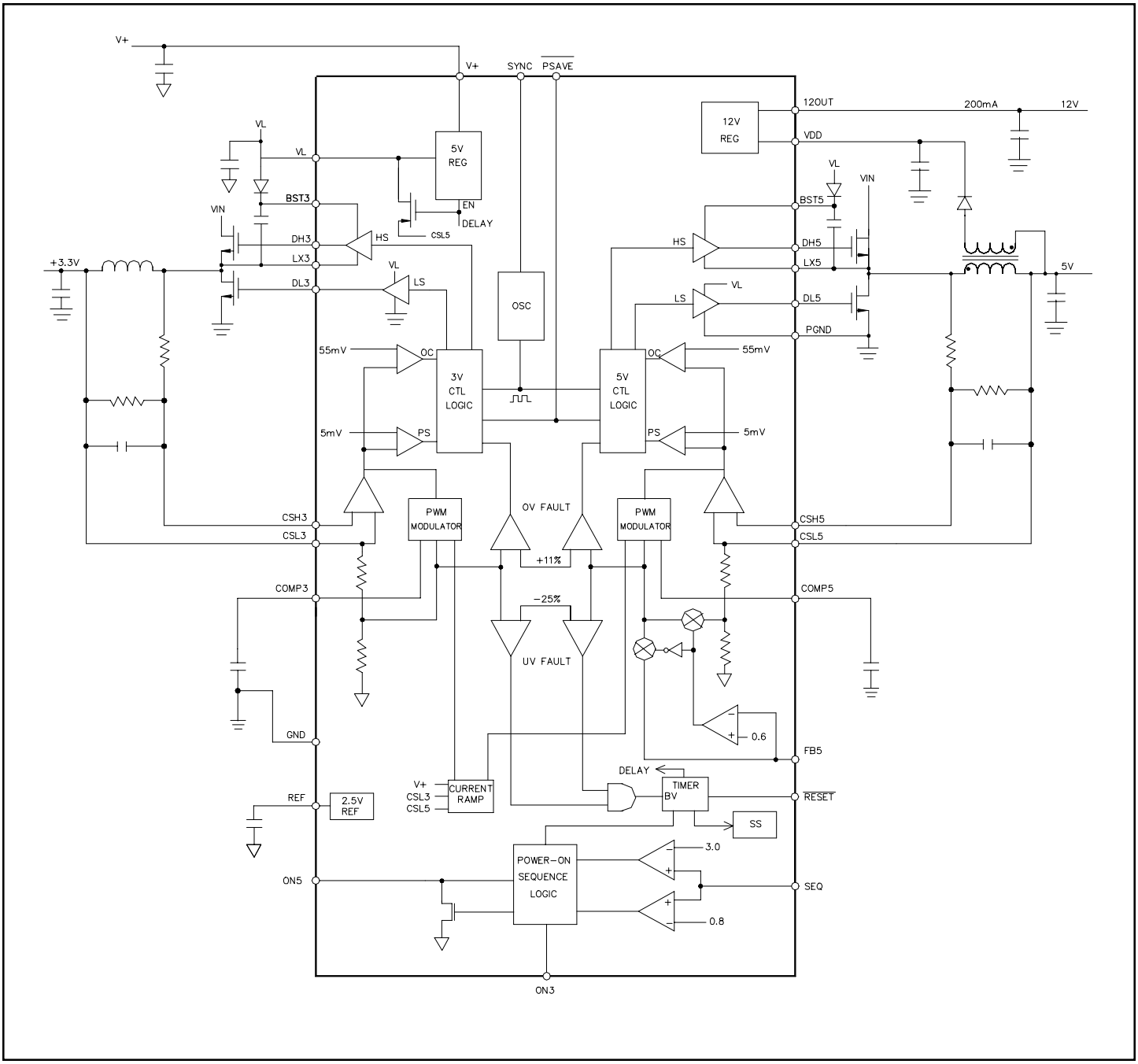
Notes:
(1) This device is ESD sensitive. Use of standard ESD handling procedures required.
(2) Applicable from 0 to +85°C.

Pin Descriptions

Pin #	Pin Name	Pin Function
1	CSH3	Current limit sense input for 3V SMPS. Connect to the inductor side of a current sense resistor.
2	CSL3	Output voltage sense input for 3V SMPS. Connect to the output side of a current sense resistor.
3	COMP3	Compensation pin and output of the 3.3V SMPS error amplifier.
4	12OUT	12V internal linear regulator output.
5	VDD	Supply voltage input for the 12OUT linear regulator. Also connects internally to a 19V overvoltage shunt regulator clamp.
6	SYNC	Oscillator Synchronization and Frequency Select. Tie to VL for 300 kHz operation; tie to GND for 200 kHz. Drive externally to synchronize to an external oscillator between 240 kHz and 350 kHz.
7	ON5	5V ON/OFF Control Input. Connect a 1K-10K ohm resistor in series with ON5 to allow 5V shutdown on OVP/UV.
8	GND	Low noise Analog Ground and Feedback reference point.
9	REF	2.5 V Reference Voltage output. Bypass to GND with 1 µF minimum.
10	PSAVE#	Logic input that disables PSAVE Mode when high. Connect to GND for normal use.
11	RESET#	Active-low timed Reset output. RESET# swings from GND to VL. RESET# goes high after a fixed 32,000 clock cycle delay following a successful power up.
12	COMP5	Compensation pin and output of the 5V SMPS error amplifier.
13	CSL5	Output voltage sense input for 5V SMPS. Connect to the output side of a current sense resistor.
14	CSH5	Current limit sense input for 5V SMPS. Connect to the inductor side of a current sense resistor.
15	SEQ	Input that selects SMPS power-up sequence and selects monitor voltage(s) used by RESET#.
16	DH5	Gate Drive Output for the 5V, high-side N-Channel switch.
17	PHASE5	5V switching node (inductor) connection.
18	BST5	Boost capacitor connection for 5V high-side gate drive.
19	DL5	Gate drive output for the 5V low-side synchronous rectifier MOSFET
20	PGND	Power Ground.
21	VL	5 V internal linear regulator output. For improved efficiency, VL is switched to the 5V SMPS output when 5V SMPS is enabled.
22	V+	Battery Voltage input.
23	SHDN#	Shutdown control input, active low.
24	DL3	Gate drive output for the 3V low-side synchronous rectifier MOSFET.
25	BST3	Boost capacitor connection for 3V high-side gate drive.
26	PHASE3	3V switching node (inductor) connection.
27	DH3	Gate drive output for the 3V high-side N-Channel switch.
28	ON3	3V ON/OFF Control Input.

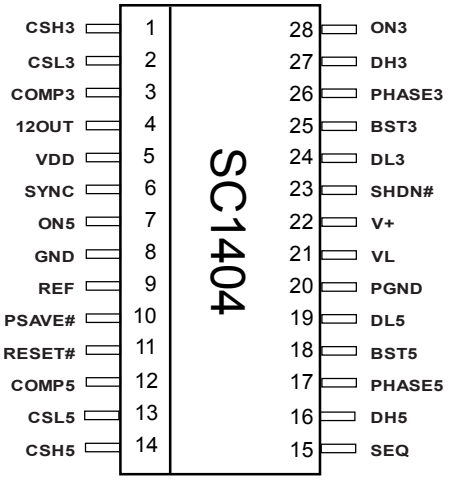
Note: All logic level inputs and outputs are open collector TTL compatible.

Block Diagram



Pin Configuration

Top View



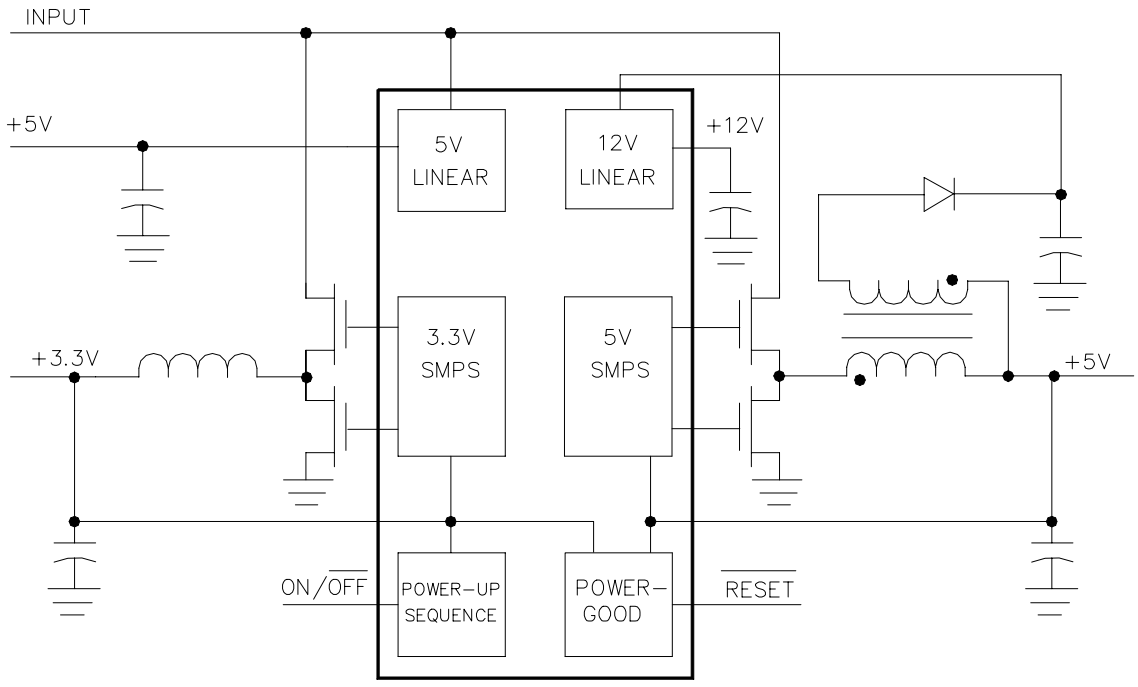
TSSOP-28/SSOP-28

Ordering Information

DEVICE	PACKAGE	TEMP. (T_{AMB})
SC1404ITSTR	TSSOP-28 (1)	-40 - +85°C
SC1404ISSTR	SSOP-28 (1)	

Note:
(1) Only available in tape and reel packaging. A reel contains 2500 devices for TSSOP and 1000 devices for SSOP.

Block Diagram



Detailed Description

The SC1404 is a versatile multiple-output power supply controller for battery operated systems. The SC1404 provides synchronous rectified buck control in fixed frequency forced-continuous (PWM) mode and hysteretic PSAVE mode, for two switching power supplies over a wide load range. Out of phase switching reduces input noise and RMS current, which reduces the input filter inductors and capacitors. The two switchers have on-chip preset output voltages of 5.0V and 3.3V.

The control circuitry for each PWM controller includes digital softstart, voltage error amplifier with built-in slope compensation, pulse width modulator, power save, overcurrent, overvoltage and undervoltage fault protection. Two linear regulators and a precision reference voltage are also provided. The 5V/30mA linear regulator (VL) uses battery power to feed the gate drivers. For improved efficiency, VL automatically switches over the +5V converter output if available. The 12V linear regulator supplies up to 200mA. Semtech's proprietary Virtual Current Sense™ provides greater advantages in the aspect of stability and signal-to-noise ratio than the conventional current sense method.

PWM Control

There are two separate PWM control blocks for each switcher. They are switched out-of-phase with each other. This interleaved topology reduces input filter requirements by reducing current drawn from the filter capacitors. To avoid both switchers switching at the same instance, there is a built-in delay between the turn-on of the 3.3V switcher and 5V switcher, the amount of which depends on the input voltage (see Out-of-Phase Switching).

The PWM provides two modes of control over the entire load range. The SC1404 operates in forced continuous conduction mode as a fixed frequency peak current mode controller with falling edge modulation. Current sense is done differently than in conventional peak current mode control. Semtech's proprietary Virtual Current Sense™ emulates the necessary inductor current information for proper functioning of the IC. In order to accommodate a wide range of output filters, a COMP pin is also available for compensating the error amplifier externally. A nominal error amplifier gain of 18 improves the system loop gain and the output transient behavior.

When operating in continuous conduction mode, the high-side mosfet is turned on at the start of each switching cycle. It is turned off when the desired duty cycle is reached. Active shoot-through protection will delay the lower mosfet turn-on until the phase node drops below 1V. The low-side mosfet remains on until the beginning of the next switching cycle. Again, active shoot-through protection ensures that the low-side mosfet gate voltage drops low before the high-side mosfet turns on.

Under light load conditions when the PSAVE# pin is low, the SC1404 operates hysteretically in the discontinuous conduction mode to reduce its switching frequency and switching bias current. The switching of the output mosfet does not depend on a given oscillator frequency, but on the hysteretic voltage set around the nominal output voltage. When entering PSAVE# mode (from heavy to light load), if the minimum (valley) inductor current measured at CSHx-CSLx is below the Zero Cross threshold (typically 5 mV) for four switching cycles, the virtual current sense circuitry will shut off and the mode changes to hysteretic mode. As the load current increases, if the minimum (valley) inductor current is above the threshold for four switching cycles, the converter stops psave mode and enters PWM operation. The change in frequency between hysteretic psave and PWM mode provides hysteresis to inhibit chattering between the two modes of operation.

Gate Drive / Control

The gate drivers on the SC1404 are designed to switch large mosfets. The high-side gate driver must drive the gate of high-side mosfet above the V+ input. The supply for the gate drivers is generated by charging a boostrap capacitor from the VL supply when the low-side driver is on. In continuous conduction mode, the low-side driver output that controls the synchronous rectifier in the power stage is on when the high-side driver is off. Under light load conditions when PSAVE# pin is low, the inductor ripple current will approach the point where it reverses polarity. This is detected by the low-side driver control and the synchronous rectifier is turned off before the current reverses, preventing energy drain from the output. The low-side driver operation is also affected by various fault conditions as described in the Fault Protection section.

Internal Bias Supply

The VL linear regulator is a 5V output that powers the gate drivers, 2.5V reference and internal controls of the SC1404. The regulator is capable of supplying up to 30mA (including mosfet gate charge current). The VL pin should be bypassed to GND with 4.7uF to supply the large gate drive current pulses.

The regulator receives input power from the V+ battery input. Efficiency is improved by providing a bootstrap for the VL output. When the 5V SMPS output voltage reaches 5V, internal circuitry turns on a PMOS device between CSL5 and VL. The internal VL regulator is then disabled, and VL bias is provided by the high efficiency 5V switcher.

The REF output is accurate to +/- 2% over temperature. It is capable of delivering 5mA max and should be bypassed with 1uF minimum capacitor. Loading the REF pin will reduce the REF voltage slightly as seen in the following table.

Loading Resistance (ohm)	511	2.67K	49.9K	255K	1Meg
Vref Deviation	8.3mV	3.1mV	0.5mV	0.3mV	0mV

Current Sense (CSH, CSL)

Output current of each supply is sensed at the CSH and CSL pins. Overcurrent is reached when the current sense voltage exceeds 55mV typical. On a cycle-by-cycle basis, a positive overcurrent turns off the high-side driver and a negative overcurrent turns off the low-side driver.

Oscillator

When the SYNC pin is high the oscillator runs at 300kHz; when SYNC is low the frequency is 200kHz. The oscillator will synchronize to the falling edge of a clock on the SYNC pin with a frequency between 240kHz and 350kHz. In general, 200kHz operation provides highest efficiency, while 300kHz allows for smaller output ripple and/or smaller filter components.

Fault Protection

In addition to cycle-by-cycle current limit, the SC1404 provides overtemperature, output overvoltage, and undervoltage protection. Overtemperature protection will shut the device down if die temperature exceeds 150°C, with 10°C hysteresis.

If either SMPS output is more than 10% above its nominal value, both SMPS are latched off and the low side mosfets are latched on. To prevent the output from ringing below ground in a fault condition, a 1A Schottky diode should be placed across each output.

Two different levels of undervoltage (UV) are detected. If the output falls 9% below its nominal value, the RESET# output is pulled low. If the output falls 25% below its nominal value, both SMPS are latched off.

Both of the latched faults (OVP and UV) persist until SHDN or ON3 is toggled, or the V+ input is brought below 1V.

Shutdown and Operating Modes

Holding the SHDN pin low disables the SC1404, reducing the V+ input current to less than 10uA. When SHDN is high, the part enters standby mode where the VL regulator and VREF are enabled. Turning on either SMPS will put the SC1404 in run mode.

SHDN	ON3	ON5	MODE	DESCRIPTION
Low	X	X	Shut-down	Minimum bias current
High	Low	Low	Standby	VREF and VL regulator enable
High	High	High	Run Mode	Both SMPS Running

Power up Controls and Soft Start

The user controls the SC1404 RESET# through the SEQ, ON3 and ON5 pins, as shown in the Startup Sequence Chart. At startup, RESET# is held low for 32K switching cycles, and then RESET# is determined by the output voltages and the SEQ pin.

To prevent surge currents at startup, each SMPS has a counter and DAC to incrementally raise the current limit (CSH-CSL voltage). The current limit follows discrete steps of typically 25%, 40%, 60%, 80%, and 100%, each step lasting 128 clock cycles. To charge up the output capacitors, inductor current at startup must exceed load current. When the output voltage reaches it's nominal value the SMPS will reduce duty cycle, but the excess LI^2 energy of the inductor must flow into the load and output capacitors. If the output capacitor is relatively small, the peak output voltage can approach the overvoltage trip point. To prevent nuisance OVP at startup, the inductance and capacitance must meet the following criteria:

$$\frac{L_{MAX}}{C_{MIN}} \le \frac{V_{O\_NOM}^{2}}{IL_{MAX\_OC}^{2}} \cdot 1.59$$

IL_{MAX_OC} is the maximum inductor current set by the current-limit components, and V_{O_NOM} is the nominal output voltage.

12OUT Supply

The 12OUT linear regulator is capable of supplying 200mA. The input voltage to the 12OUT regulator is generated by a secondary winding on the 5V SMPS inductor.

A heavy load on the 12OUT regulator when the 5V SMPS operates in PSAVE mode will cause VDD to sag, causing 12OUT to drop. If 12OUT output drops 0.8% from its nominal value, the 5V SMPS is forced out of PSAVE mode and into PWM mode for several cycles. This recharges the bulk input capacitor on VDD.

The 12OUT linear regulator has internal protection to prevent damage under short circuit conditions. Overvoltage protection is provided on the VDD input. If VDD rises above 19V, a 10mA shunt load is applied to VDD to reduce the voltage. The overvoltage threshold has 0.5V hysteresis.

Startup Sequence Chart

SEQ	ON3	ON5	RESET	DESCRIPTION
REF	LOW	LOW	Follows 3.3V SMPS.	Independant start control mode. Both SMPSs off.
REF	LOW	HIGH	Low.	5V SMPS ON, 3.3V SMPS OFF.
REF	HIGH	LOW	Follows 3.3V SMPS.	3.3V SMPS ON, 5V SMPS OFF.
REF	HIGH	HIGH	Follows 3.3V SMPS.	Both SMPSs on.
GND	LOW	X	Low.	Both SMPSs off.
GND	HIGH	HIGH/LOW	High after both outputs are in regulation.	5V starts when ON3 goes high. If ON5 = HIGH, 3V is on. If ON5 = LOW, 3V is off.
VL	LOW	X	Low.	Both SMPSs off.
VL	HIGH	HIGH/LOW	High after both outputs are in regulation.	3V starts when ON3 goes high. If ON5 = HIGH, 5V is on. If ON5 = LOW, 5V is off.

Applications Information

Reference Circuit Design

The schematic for the reference circuit is shown on page 20. The reference circuit is configured as follows:

Switching Regulator 1	Vout1 = 3.3V @ 6A
Switching Regulator 2	Vout2 = 5.0V @ 6A
VL Regulator	Vout3 = 5.0V @ 30mA
12V regulator	Vout4 = 12.0V @ 200mA
Input voltage	Vin = 7 to 21V

Designing the Output Filter

Before calculating the filter inductance and capacitance, an acceptable inductor ripple current is determined. Ripple current is usually set at 10% to 20% of the maximum load. However, increasing the ripple current allows for a smaller inductor and will also quicken the output transient response. In this example, we set the ripple current to be 25% of maximum load.

$$\Delta Io = 25\% \times 6A = 1.5A$$

The inductance is found from ripple current, frequency, input voltage, and output voltage. Minimum required inductance is found at maximum Vin, where ripple current is the greatest.

$$Lmin = Vo \times \frac{(1 - Vo / Vin)}{F \times \Delta Io} = 6.18uH$$

For the reference design, the Coiltronics DR127-6R8 is used. This is acceptable for the 3V output, which uses a simple inductor. The 5V inductor must have a 12V winding with a turns ratio of 2.2:1. For the 5V inductor, the TTI-8215 from Transpower Technologies is used, which has 5V inductance of 6.4uH.

To specify the output capacitance, the allowable output ripple voltage must be determined. Output ripple is often specified at 1% of the output voltage. For the 3.3V output, we selected a maximum ripple voltage of 33mVp-p. The maximum allowable ESR would then be:

$$ESR_{MAX} = \Delta V_O / \Delta I_O = 33mV / 1.5A = 22m\Omega$$

Panasonic SP Polymer Aluminum capacitors are a good choice. For this design, use one 180uF, 4V device, with ESR of 15mΩ.

The output capacitor must support the inductor RMS ripple current. To check the actual ripple versus the capacitor's RMS rating:

$$I_{RMS\_actual} = \frac{\Delta Io}{\sqrt{12}} = \frac{1.5A}{\sqrt{12}} = 0.43A$$

This is much less than the capacitor's ripple rating of 3.3A.

Choosing the Main Switching mosfet

The IRF7143 is used in the reference design. Before choosing the main (high-side) mosfet, we need to check three parameters: voltage, power, and current rating.

The maximum drain to source voltage of the mosfet is mainly determined by the switcher topology. With a buck topology,

$$V_{DS\_MAX} = V_{IN\_MAX} = 21V$$

The IRF7413 is a 30V device, which allows for 70% derating at 21V operation.

The mosfet power dissipation has three components: conduction losses, switching losses, and gate drive losses. The conduction loss is determined using the RMS mosfet current; the equation is

shown below. The mosfet current is a trapezoid waveform with values equal to:

$$I_{MIN} = I_{LOAD} - \frac{\Delta I_L}{2} \qquad I_{MAX} = I_{LOAD} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = \frac{Vo \cdot (1-D)}{fs \cdot L} \qquad D = \frac{Vo}{Vin}$$

$$I_{RMS} = \sqrt{D \cdot \left(I_{MIN}^{\ 2} + I_{MIN} \cdot I_{MAX} + I_{MAX}^{\ 2}\right)}$$

As input voltage decreases, the duty cycle increases and the ripple current decrease, and overall the RMS mosfet current will increase. The conduction losses are then given by the formula below, where Rds(on) is 18m-ohm for the IRF7413 at room temperature. Note that Rds(on) increases with temperature.

$$P_{CONDUCTION} = R_{ds(on)} \cdot I_{RMS}^{\ 2}$$

The mosfet switching loss is estimated according to:

$$P_{SWITCHING} = \frac{C_{RSS} \cdot V_{IN}^{\ 2} \cdot fs \cdot I_{OUT}}{I_G}$$

Crss is the mosfet's reverse transfer capacitance, 240pF for IRF7413. Ig is the gate driver current, which is 1A for SC1403.

The mosfet gate drive loss is estimated from:

$$P_{GATE} = \frac{1}{2} \cdot C_G \cdot Vgfs^2 \cdot fs$$

Cg is the effective gate capacitance, equal to the Total Gate Charge divided by VGS, from the vendor datasheet, and is 7.9nF for the IRF7413. Vgfs is the final gate-source voltage, 5V in this case.

The total mosfet loss is the sum of the three loss components.

$$P_{TOTAL\_DISS} = P_{CONDUCTION} + P_{SWITCHING} + P_{GATE}$$

The mosfet dissipation under conditions of 15V input, 6A load, and ambient temperature of 25C, can be determined as:

DNOM = 0.22 ΔIL = 1.26A
IMIN = 5.37A IMAX = 6.63A IRMS = 4.88A

Rds(on) (100C) = 18 mohm
PCONDUCTION = 429mW

PSWITCHING = 97mW PGATE = 30mW

PTOTAL_DISS = 429 + 97 + 30 = 556 mW

The junction temperature rise resulting from the power dissipation is calculated as:

$$\Delta T_J = P_T \cdot \theta_{JA}$$

P_T is the total device dissipation, and θ_{JA} is the package thermal resistance, which is 50°C/W for the IRf7413. The junction temperature rise is then:

$$\Delta T_J = 0.556W \cdot 50°C/W = 27.8°$$

This is an acceptable temperature rise, so no special heat sinking is required.

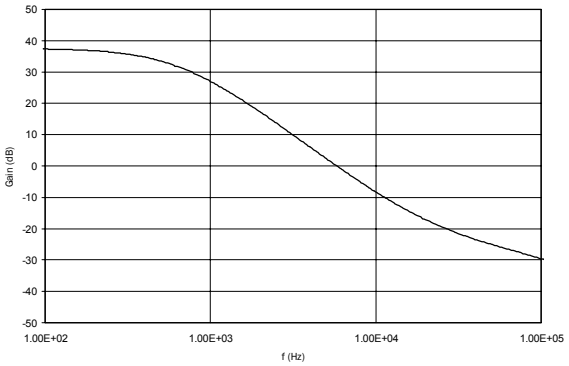
Designing the Loop

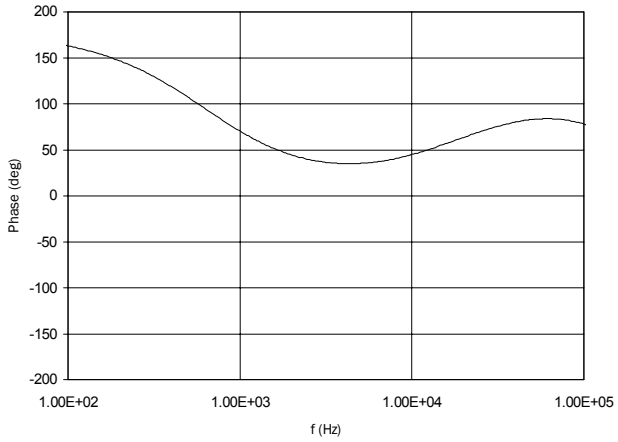
A good loop design is a combination of the power train and compensation design. In the SC1404, the control-to-output/power train response is dominated by the load impedance, the inductor, output capacitance, and the ESR of the output caps. The low frequency gain is dominated by the output load impedance and the effective current sense resistor. Inherent to Virtual Current Sense™, there is one additional low frequency pole sitting between 100Hz and 1kHz and a zero between 15kHz and 25kHz. he output of error amplifier COMP pin is available for external compensation. A traditional pole-zero-pole compensation is not necessary in the design using SC1404, a simple high frequency pole is usually sufficient.

Single-Pole Compensation Method

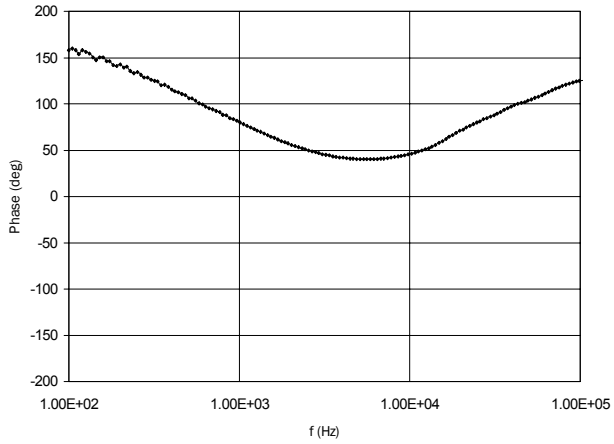
Given parameters:
Vin = 19V, Vout = 3.3V @ 2.2A,
Output impedance, Ro = 3.3V/2.2A = 1.5 Ω ,
Panasonic SP cap, Co = 180uF, Resr = 15 mΩ ,
Output inductor, Lo = 4.7uH
Switching frequency, Fs = 300kHz

Simulated Control-to-Output gain & phase response (up to 100kHz) is plotted below.

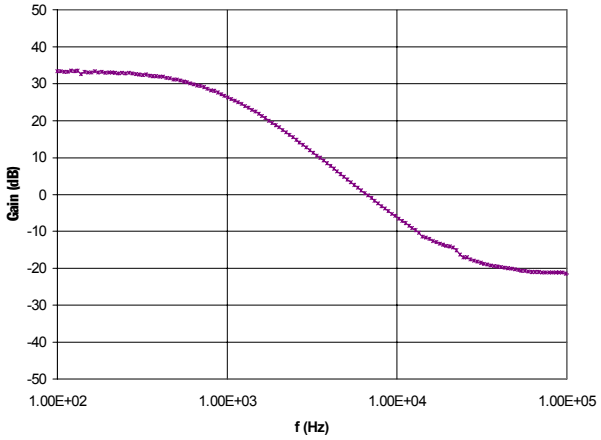


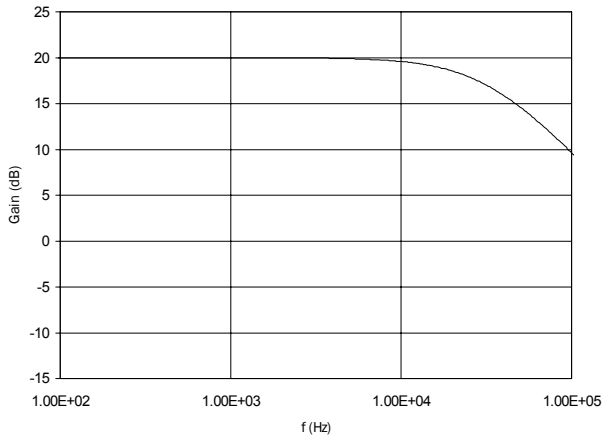


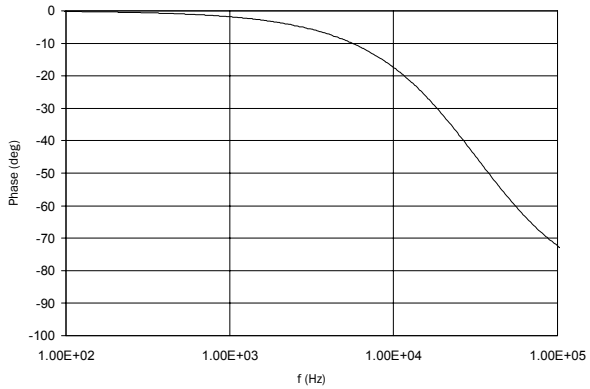
Measured Control-to-Output gain & phase response (up to 100kHz) is plotted below.



Single-pole compensation is achieved using a 100pF capacitor from the COMP pin to ground. The simulated feedback gain & phase response (up to 100kHz) is plotted below.



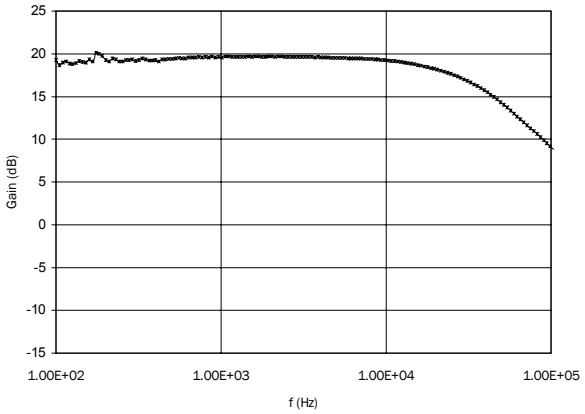


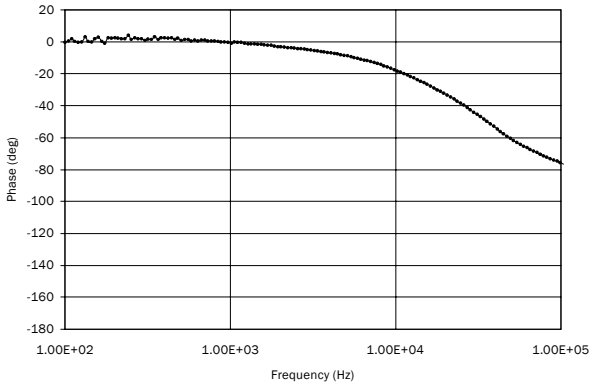


Measured feedback gain & phase responses (up to 100kHz) is plotted below.

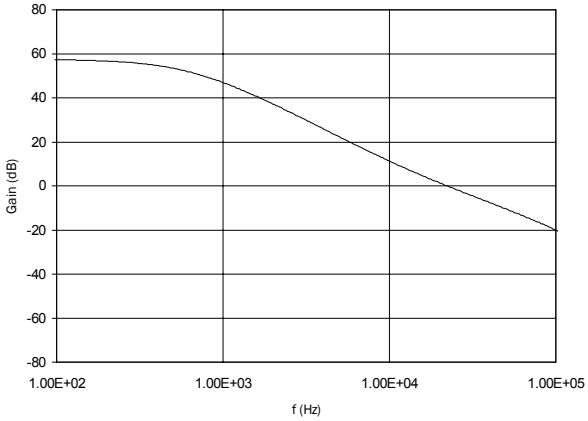
Applications Information

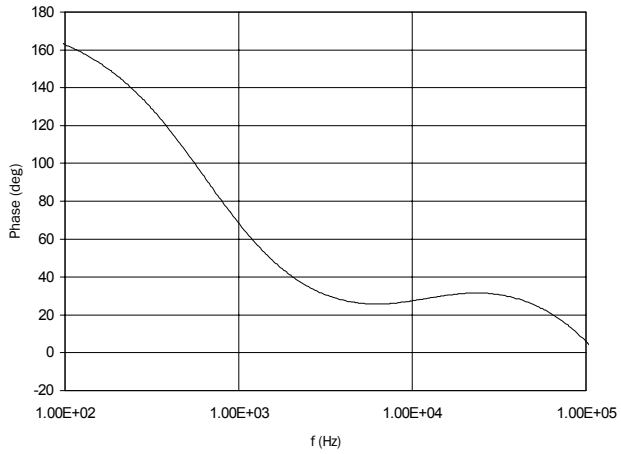
.



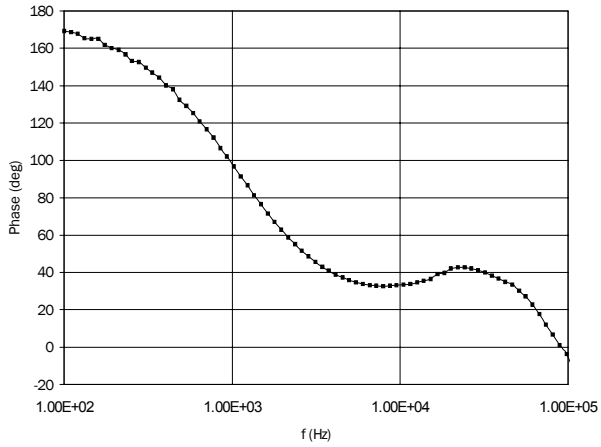


Simulated overall gain & phase responses (up to 100kHz) is plotted below.





Measured overall gain & phase response of the single-pole compensation using SC1404 is plotted below.



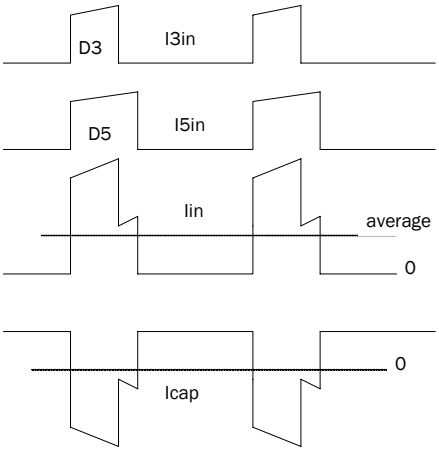
Output Cap	Recommended Compensation Cap Value
< = 180µF	100pF
> 180µF & <1000µF	200pF
>1000µF	330pF

Applications Information

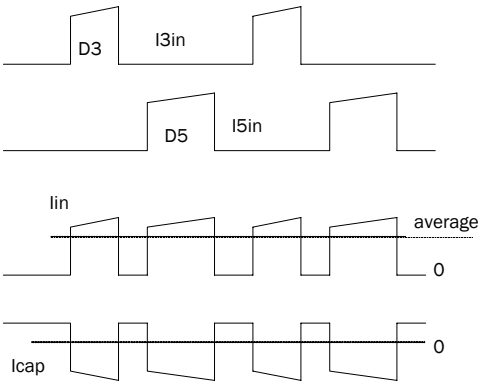
Input Capacitor Selection and Out-of-phase Switching

The SC1404 uses out-of-phase switching between the two converters to reduce input ripple current, allowing smaller cheaper input capacitors compared to in-phase switching.

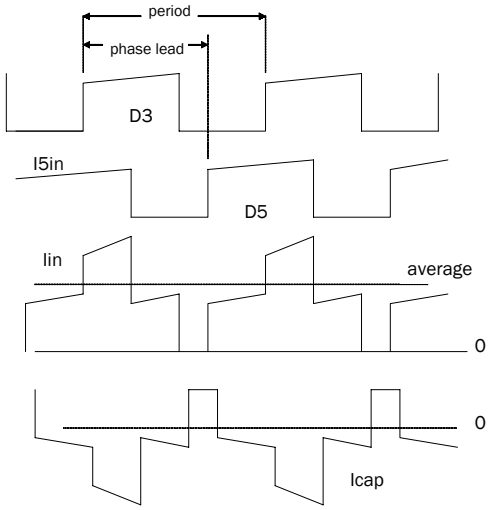
The figure below shows in-phase switching. I3in is the input current for the 3V converter, I5in is the input current for the 5V converter. The two converters start each switching cycle simultaneously, causing a significant amount of overlap and a high peak current. The total input current the third waveform, which shows how the two currents add together. The fourth waveform is current in and out of the input capacitors.



The next figure shows out-of-phase switching. The 3V and 5V pulses are spaced apart, so there is no overlap. This gives two benefits; the peak current is reduced, and the effective switch frequency is raised. Both of these make filtering easier. The third waveform is the total input current, and the fourth waveform shows the current flowing in and out of the input capacitors. The rms value of the capacitor current is significantly lower than the in-phase case, which allows for smaller capacitors.



As the input voltage is reduced, the duty cycle of both converters increases. At input voltages less than 8.3V, it is impossible to prevent overlap regardless of the phase between the converters. Overlap is seen in the following figure.



From an input filter standpoint it is desirable to minimize the overlap; but it is also desirable to keep the turn-on and turn-off transitions of the two converters separated in time, to minimize interaction between the two converters. The SC1404 keeps the turn-on and turn-off transitions separated in time by changing the phase between the converters depending on the input voltage. The following table shows the phase relationship between 3V and 5V turn-on, based on input voltage.

Input voltage	Phase lead from 3V to 5V
Vin > 9.6 V	41% of switching period No overlap between 3.3V and 5V
9.6V > Vin > 6.7V	59% of switching period Small overlap to prevent simultaneous 3V/5V switching
6.7 > Vin	64% of switching period Small overlap to prevent simultaneous 3V/5V switching

Typical Characteristics

Input ripple current can be calculated from the following equations.

$D3 = 3.3V/V_{IN} = 3V$ duty cycle

$D5 = 5V/V_{IN} = 5V$ duty cycle

$I3 = 3V$ DC load current

$I5 = 5V$ DC load current

D_{OVL} = overlapping duty cycle of the 3V and 5V pulses (varies according to input voltage)

$D_{OVL} = 0$ for $9.6V \le V_{IN}$

$D_{OVL} = (D5 - 0.41)$ for $6.7V \le V_{IN} < 9.6V$

$D_{OVL} = (D5 - 0.36)$ for $V_{IN} < 6.7$

I_{IN} = Average DC input current

$I_{IN} = I3 \cdot D3 + I5 \cdot D5$

I_{SW_RMS} = RMS current drawn from V_{IN}

$I_{SW\_RMS}^2 = D3 \cdot I3^2 + D5 \cdot I5^2 + 2 \cdot D_{OVL} \cdot I3 \cdot I5$

$$I_{RMS\_CAP} = \sqrt{I_{SW\_RMS}^{\ 2} + I_{IN\_AVE}^{\ 2}}$$

The worst-case ripple current varies by application. For the case 6A load on both outputs, the worst-case ripple occurs at Vin = 7.5V, and the rms capacitor current is 4.2A. The reference design uses 4 paralleled ceramic capacitors, (Murata GRM32NF51E106Z, 10 uF 25V, size 1210). Each capacitor is rated at 2.2A.

Choosing Synchronous mosfet and Schottky Diode

Since this is a buck topology, the voltage and current ratings of the synchronous mosfet are the same as the main switching mosfet. It makes sense cost- and volume-wise to use the same mosfet for the main switch as for the synchronous mosfet. Therefore, IRF7413 is used again in the design for synchronous mosfet.

To improve overall efficiency, an external Schottky diode is used in parallel with the low side mosfet. The freewheeling current enters the Schottky diode instead of the inefficient body diode of the synchronous mosfet. It is really important when laying out the board to place the synchronous mosfet and Schottky diode close to each other to reduce the current ramp-up and ramp-down time due to parasitic inductance between the channel of the mosfet and the Schottky diode. The current rating of the Schottky diode can be determined by the following equation:

$$IF\_AVG = I_{LOAD} \cdot \frac{100n}{TS} = 0.2A$$

where 100nsec is the estimated time between the mosfet turn-off and the Schottky diode turn-on and Ts = 3.33uS.A Schottky diode with a forward current of 0.5A is sufficient for this design.

Operation below 6V input

The SC1404 will operate below 6V input voltage with careful design, but there are limitations. The first limitation is the maximum available duty cycle from the SC1404, which limits the obtainable output voltage. The design should minimize all circuit losses through the system in order to deliver maximum power to the output.

A second limitation with operation below 6V is transient response. When load current increases rapidly, the output voltage drops slightly; the feedback loop normally increases duty cycle briefly to bring the output voltage back up. If duty cycle is already near the maximum limit, the duty cycle cannot increase enough to meet the demand, and the output voltage sags more than normal. This problem can not be solved by changing the feedback compensation, it is a function of the input voltage, duty cycle, and inductor and capacitor values.

If an application requires 5V output from an input voltage below 6V, the following guidelines should be used:

1 - Set the switching frequency to 200 kHz (Tie SYNC to ground). This increases the maximum duty cycle compared to 300 kHz operation.

2 - Minimize the resistance in the power train. Select mosfets, inductor, and current sense resistor to provide the lowest resistance as is practical.

3 - Minimize the pcb resistance for all traces carrying high current. This includes traces to the input capacitors, mosfetS and diodes, inductor, current sense resistor, and output capacitor.

4 - Minimize the resistance between the SC1404 circuit and the power source (battery, battery charger, AC adaptor).

5 - Use low ESR capacitors on the input to prevent the input voltage dropping during on-time.

6 - If large load transients are expected, high capacitance and low ESR capacitors should be used on both the input and output.

5V Start-up with slow Vin ramp.

Proper startup of the 5V output can be hampered by slow dV/dt on the input. The SC1404 will power up and attempt to generate an output when the input voltage exceeds 4.5 volts. If the input has a slow dV/dt, the input voltage will not rise significantly during the start-up sequence, leading to two conditions. First, the VL supply can be hundreds of mV below 5V, since the input may not yet be above 5V. Second, the duty cycle will be at maximum, leading to very small off-times. These two conditions tend to reduce the boost voltage; if continued indefinitely, the boost capacitor may be unable to recharge fully, and eventually the high-side driver loses its boost bias.

To avoid this the following steps should be taken:

1. If possible the dV/dt of the input supply should exceed .02V/usec. This dV/dt condition only applies when the input passes between 4 and 6 volts, the point at which the SC1404 begins a startup sequence. An alternative is to make sure the input voltage reaches 6 volts within 100 usec of SC1404 startup at approximately 4.2 volts. This is sufficiently fast to allow VL and duty cycle to achieve normal levels and prevents the boost voltage from falling.

2. If the input dV/dt cannot meet condition 1, the startup of the SC1404 should be delayed until the input voltage reaches 6V. This can be done using either the SHDN# or ON5 pin. If the dV/dt is moderate (slews from 4 to 6 volts in several msecs), an RC delay on either the SHDN# or ON5 pin should be enough to delay turn-on until the input reaches 6V.

3. For slow dV/dt on the input (10's of msec), the SC1404 should be held off until the input reaches 6V. This can be done using a comparator or external logic to hold the SHDN# or ON5 pin low until the input reaches 6V.

12V Load Limitations

The 12V regulator derives input power from a secondary winding on the 5V inductor. During the 5V off-time, the inductor transfers energy from the 5V winding to the secondary winding, thereby providing a crudely regulated 15V that feeds the 12V regulator.

Note that duty cycle increases at low input voltages, and therefore the on-time decreases. At low input voltages, the duty cycle increases to maintain the 5V output. The off-time consequently decreases, which has two detrimental effects. It allows less time to recharge the raw 15V capacitor, and it also raises the peak 15V current required to maintain the average 12V load. The 15V winding needs higher peak current, delivered in less time. But the stray (leakage) inductance of the inductor resists rapid changes in winding current, and ultimately limits how much current can be drawn from 15V before the voltage falls.

The following guidelines for 12V loading apply to the typical circuit, page 22.

Vin range	12V load conditions
>10V	12V load < 1/2 * 5V load 12V load = 200mA max
7V - 10V	12V load < 1/2 * 5V load Linearly derate 12V load: 200mA at 10V 100mA at 7V
6V - 7V	12V load < 1/2 * 5V load Linearly derate 12V load: 100mA at 10V 25mA at 7V

Overvoltage Test

Measuring the overvoltage trip point can be problematic. Any buck converter with synchronous mosfets can act as a boost converter, sending energy from output to input. In some cases the energy sent to the input is enough to drive the input voltage beyond normal levels, causing input overvoltage. To prevent this, enable the SC1404 PSAVE# feature, which effectively disables the low side mosfet drive so that little energy, if any, is transferred back to the input.

Semtech recommends the following circuit for measuring the overvoltage trip point. D1 prevents the output voltage from damaging lab supply 1. R1 limits the amount of energy that can be cycled from the output to the input. R2 absorbs the energy that might flow from output to input, and D2 protects lab supply from possible damage. The ON5 signal is monitored to indicate when overvoltage occurs.

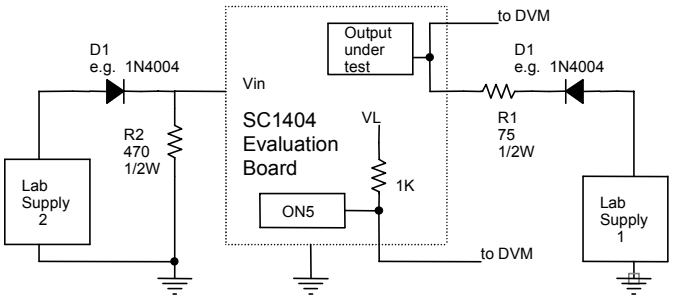
Initial conditions:

Both lab supplies set to zero volts
No load connected to 3V or 5V
PSAVE# enabled (PSAVE# tied to GND)
ON5 enabled
ON3 enabled
DVMs monitoring ON5 and the output under test.
Oscilloscope probe connected to Phase Node of the output under test (not strictly required).

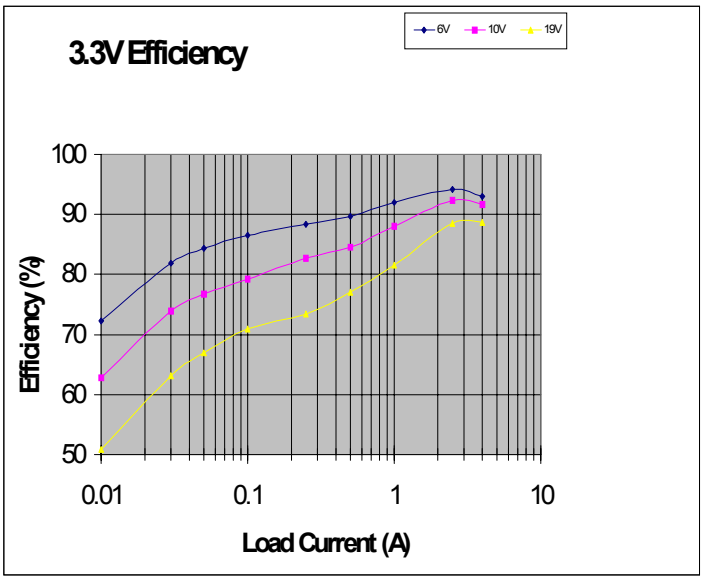
Set Lab Supply 2 to provide 10V at the SC1404 input. The phase node of the output being tested should show some switching activity. The ON5 pin should be above 4V.

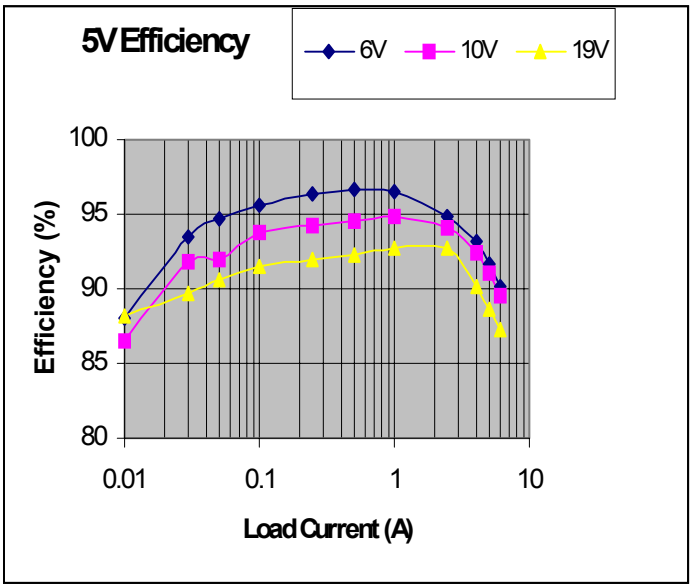
Slowly increase Lab Supply 1 until the output under test rises slightly above it's normal DC level. As Lab Supply 1 increases, switching activity at the phase node will cease. The ON5 pin should remain above 4V.

Increase Lab Supply 1 in very small increments, monitoring both ON5 and the output under test. The overvoltage trip point is the highest voltage seen at the output before ON5 pulls low (approximately 0.3V). Do not record the voltage seen at the output after ON5 has pulled low; when ON5 pulls low, the current flowing in D1 changes, corrupting the voltage seen at the output.



Typical Characteristics





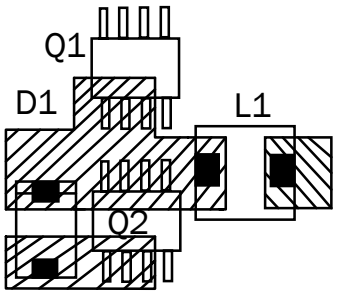
Layout Guidelines

As with any high frequency switching regulator design, a good PCB layout is essential to optimize performance of the converter. Before starting pcb layout, a careful layout strategy is strongly recommended. See the pcb layout in the SC1404 Evaluation Kit manual for example. In most applications, FR4 board material with 4 or more layers and at least 2-ounce copper is recommended(for output current up to 6A). Use at least one inner layer for ground connection. It is good practice to tie signal ground and power ground together at one single point so that the signal ground is not easily contaminated. Also be sure that high current paths have low inductance and resistance by making trace widths as wide as possible and lengths as short as possible. Use low-impedance bypassing for lines that pull large amounts of current in short periods of time. The following step by step layout strategy is recommended.

Step #1. Power train components placement.

a. Power train arrangement.

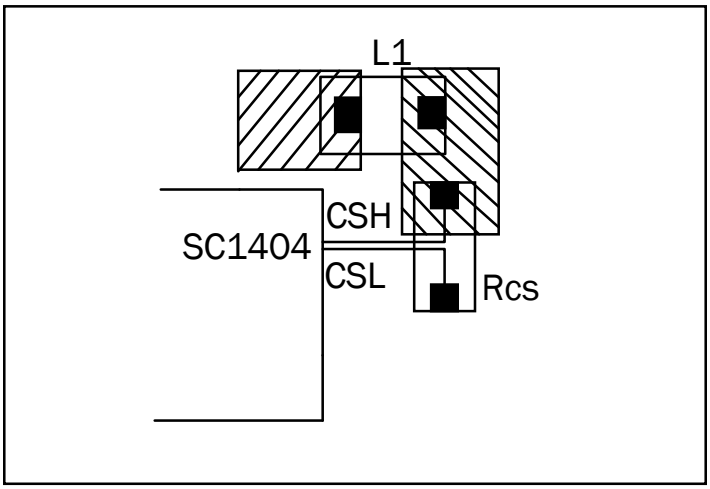
Place power train components first. The figure below shows the recommended power train arrangement. Q1 is the main switching mosfet, Q2 is the low side mosfet, D1 is the Schottky diode and L1 is the output inductor.



The phase node is generally the largest source of noise in the converter circuit since it switches at very high rate of speed. The phase node connections should be kept to a minimum size consistent with its connectivity and current carrying requirements. Place the Schottky diode as close to the phase node as possible to minimize the trace inductance between it and the low side mosfet, to reduce the efficiency loss due to the current ramp-up and down time. This is important when the converter needs to handle high di/dt requirements.

b. Current Sense.

Minimize the length of current sense signal traces. Keep them less than 15mm. Kelvin connections should be used; try to keep the traces parallel to each other and route them close to each other as much as possible. Even though SC1404 implements Virtual Current Sense scheme, the current sense signal is sampled by the SC1404 to determine the PSAVE threshold. See the following figure for a Kelvin connection of the current sense signal.



c. Gate Drive.

SC1404 has built-in gate drivers capable of sinking/sourcing 1A peaks. Upper gate drive signals are noisier than the lower ones. Therefore, place them away from sensitive analog circuitries. Make sure the lower gate traces are as close as possible to the IC pins and both upper and lower gate traces as wide as possible.

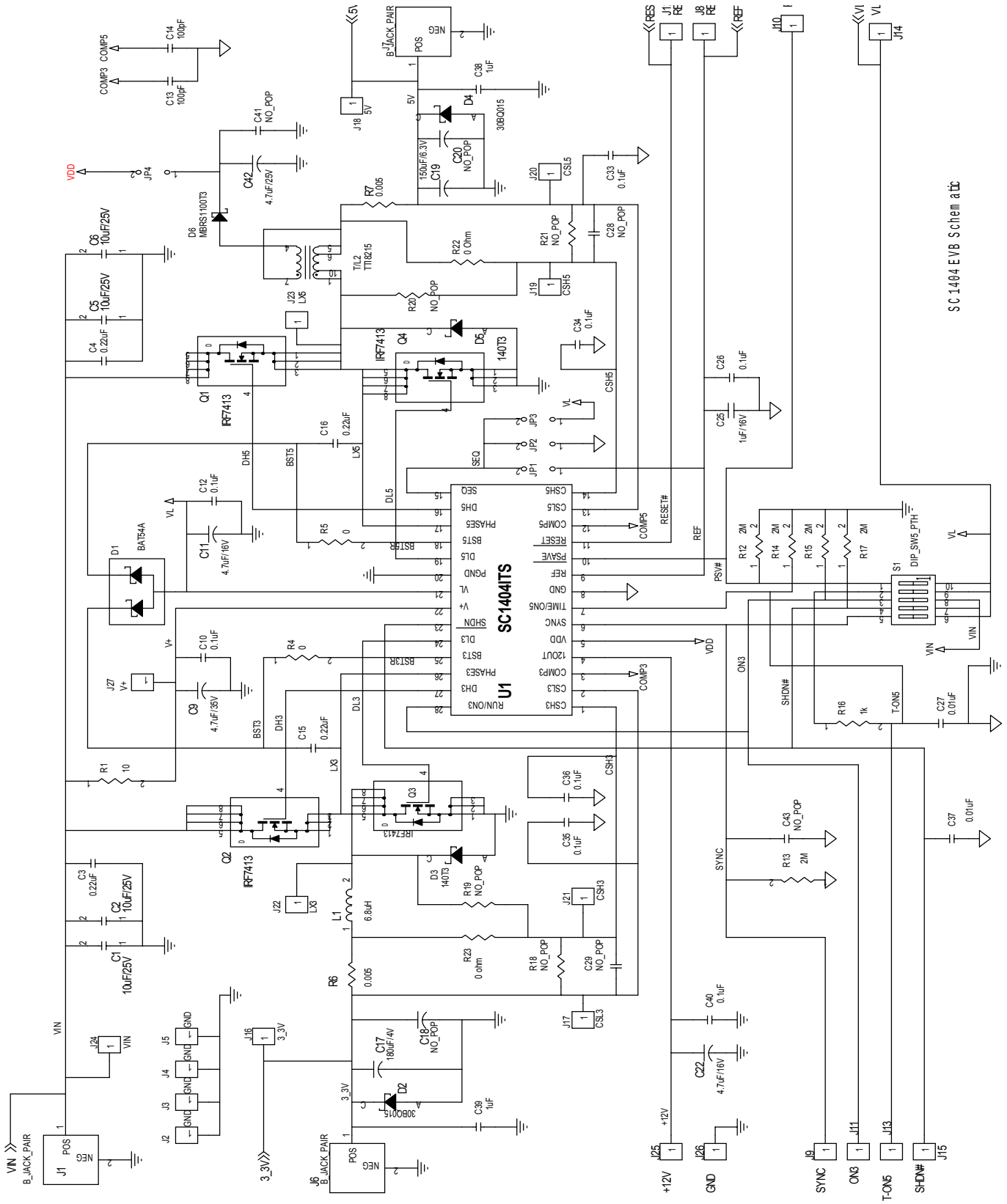
Step #2: PWM controller placement (pins) and signal ground island.

Connect all analog grounds to a separate solid copper island plane, which connects to the SC1404's GND pin. This includes REF, COMP3, COMP5, SYNC, ON3, ON5, PSV# and RESET#.

Step #3: Ground plane arrangement.

There are several ways to tie the different grounds together. Since this is a buck topology converter, the output ground is relatively quieter than the input ground. Therefore connect analog ground to power ground at the output side. Often it is useful to use a separate ground symbol for the two grounds, and tie the two grounds together at a single point through a 0Ω resistor. The power ground for the input side and the power ground for the output side is the same ground and they can be tied together using internal planes.

Evaluation Board Schematic



Evaluation Board Bill of Materials

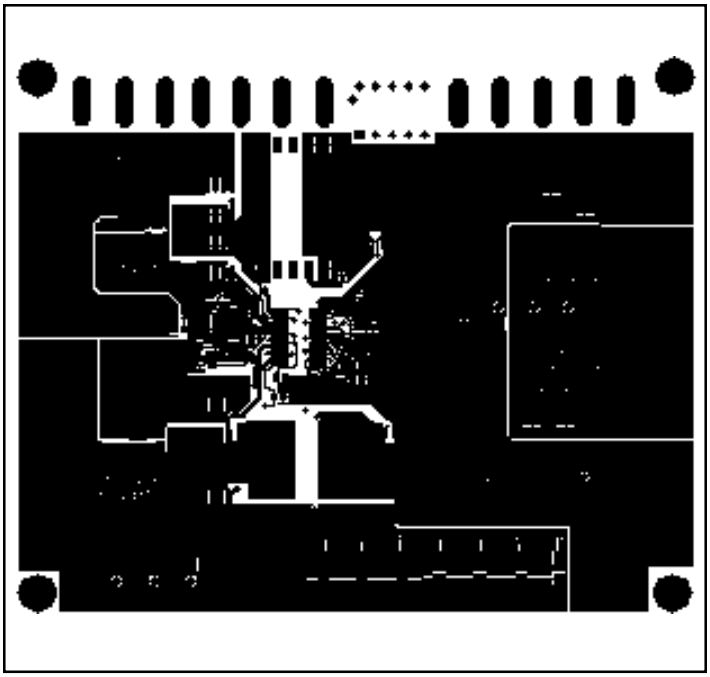
ITEM	QTY	DESIGNATION	PART NUMBER	DESCRIPTION	MANUFACTURER	FORM FACTOR
1	4	C1,C2,C5,C6	GRM230Y5V106Z025	10uF, 25V	Murata	1210
2	1	C3, C4, C15, C16		0.22uF, 50V, Y5V	Panasonic	805
3		C9		4.7uF, 35V		B_case
4		C10,C12,C26,C33,C34,C3-5,C36,C40		0.1uF,50V, X7R	Panasonic	0603
5		C11,C22	Y475M250N	4.7uF, 16V	Novacap	1812
6		C14,C13	ECJ1VC1H101K	100pF, 50V	Panasonic	0603
7		C17	EEF-UE0G181R	180uF, 4V	Panasonic	D_Case_7343
8		C19	EEF-UE0J151R	150uF, 6.3V	Panasonic	D_Case_7343
9		C25	ECJ3FB1C105	1uF, 16V	Panasonic	1206
10		C37,C27	ECJ1VB1C104K	0.01uF, 50V	Panasonic	0603
11		C39,C38		1uF		0603
12		C42		4.7uF, 25V		
13	1	D1	BAT54A	30V, 200ma, dual C_Anode	Zetex	SOT-23
14	2	D2, D4	30BQ015		I. R.	SMC
15	2	D3, D5	MBRS140T3	40V, 1A Schottky	Motorola	SMB
16	1	D6	MBRS1100T3		Motorola	SMB

Evaluation Board Bill of Materials Cont.

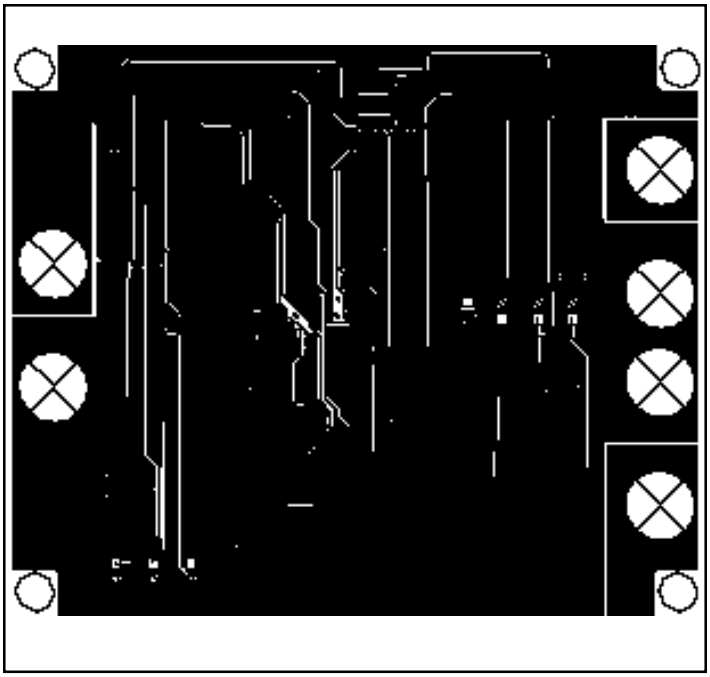
ITEM	QTY	DESIGNATION	PART NUMBER	DESCRIPTION	MANUFACTURER	FORM FACTOR
17	4	JP1, JP2, JP3, JP4		2 Pin Berg Connector	Berg	
18	3	J1, J6, J7		Banana Jack Pair		
19	24	J2-J5, J8-J27		Test Points		
20	1	L1	DR127-6R8	SMT Inductor 6.8uH	Coiltronics	
21	4	Q1, Q2, Q3, Q4	IRF7413	30V N-channel MOSFET	International Rectifier	SO8
22	1	R1	Any	10ohm	Any	0603
23	4	R4, R5, R22, R23	Any	0ohm	Any	0603
24	2	R6, R7	WSL2512R005FB43	5mohm	Vishay Dale	2512
25	5	R12, R13, R14, R15, R17	Any	2Megohm	Any	0603
26	1	R16	Any	1Kohm	Any	0603
27	1	SW1		5-position Dipswitch	Any	
28	1	T/L2	TTI-8215		Transpower Technologies	
29	1	U1	SC1404ITS		Semtech	

Evaluation Board Gerber Plots

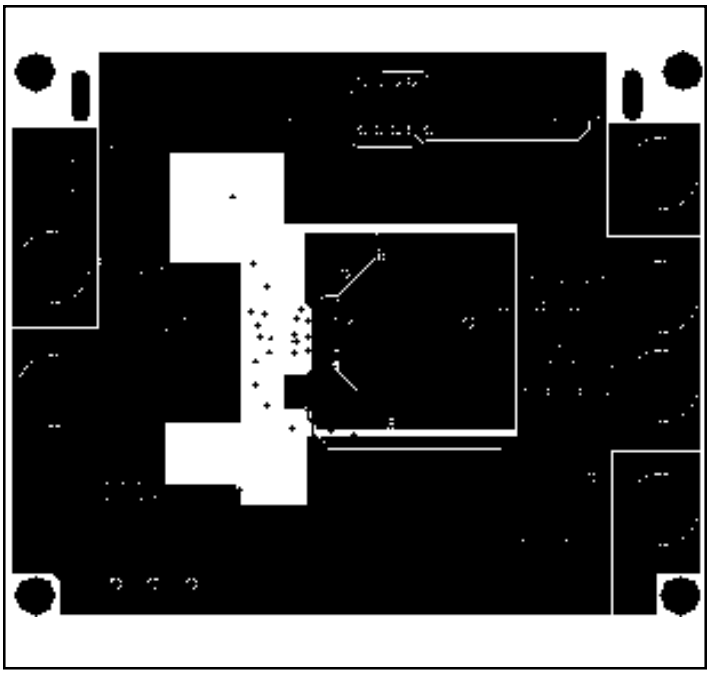
Top



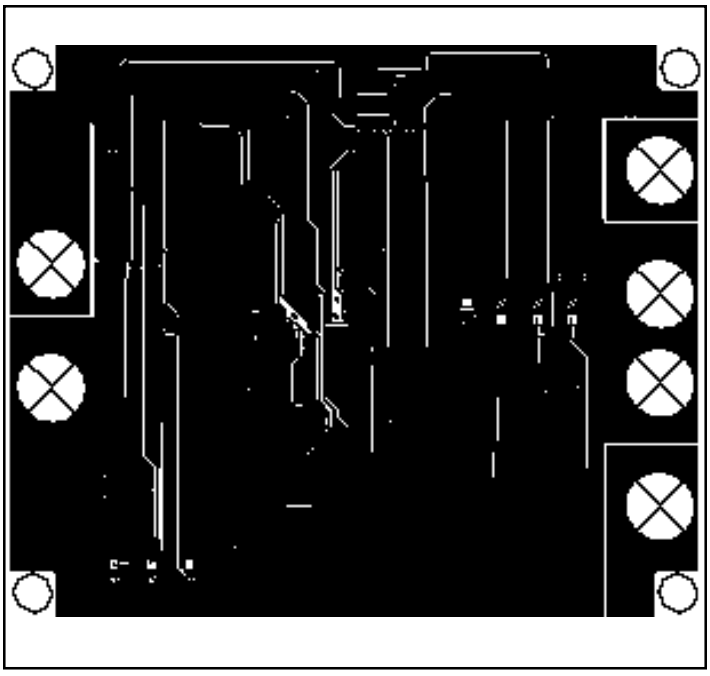
Inner2



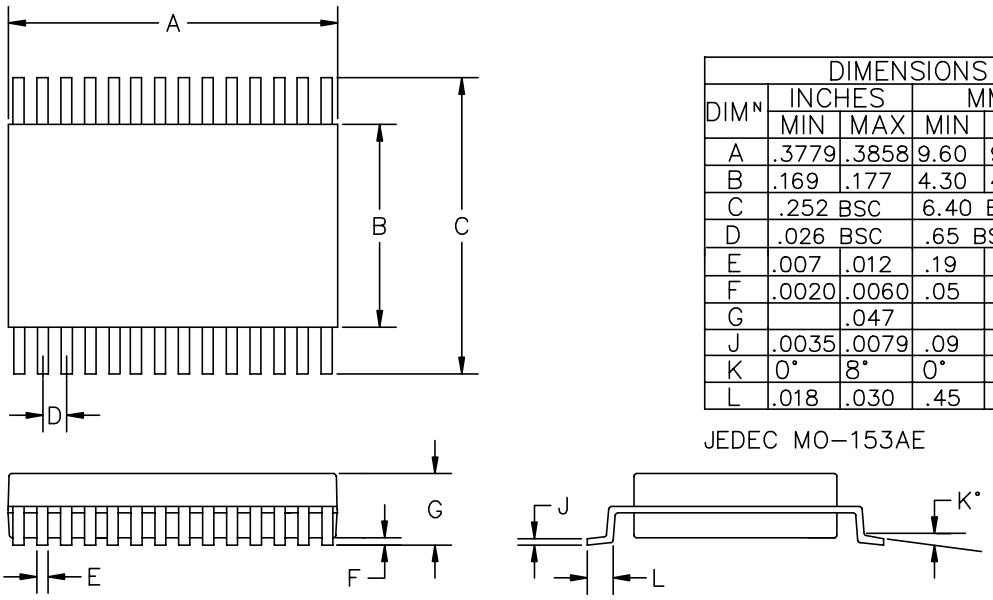
Inner1



Bottom



Outline Drawing - TSSOP-28



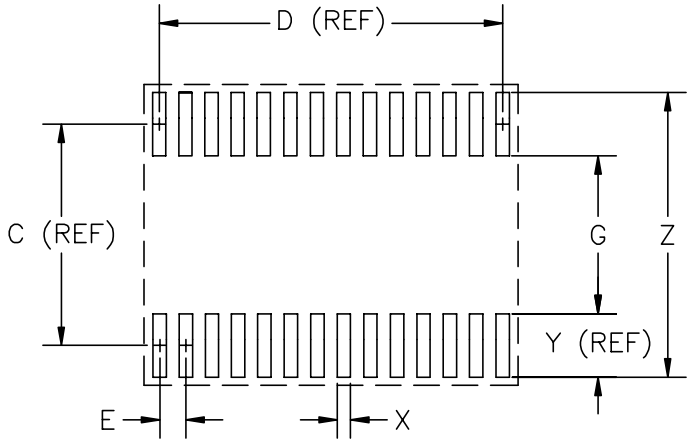
DIMENSIONS [1]					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.3779	.3858	9.60	9.80	[2]
B	.169	.177	4.30	4.50	[2]
C	.252 BSC		6.40 BSC		–
D	.026 BSC		.65 BSC		–
E	.007	.012	.19	.30	–
F	.0020	.0060	.05	.15	–
G		.047		1.20	–
J	.0035	.0079	.09	.20	–
K	0°	8°	0°	8°	–
L	.018	.030	.45	.75	–

JEDEC MO–153AE

[2] DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSIONS.

[1] CONTROLLING DIMENSIONS: MILLIMETERS.

Land Pattern - TSSOP-28

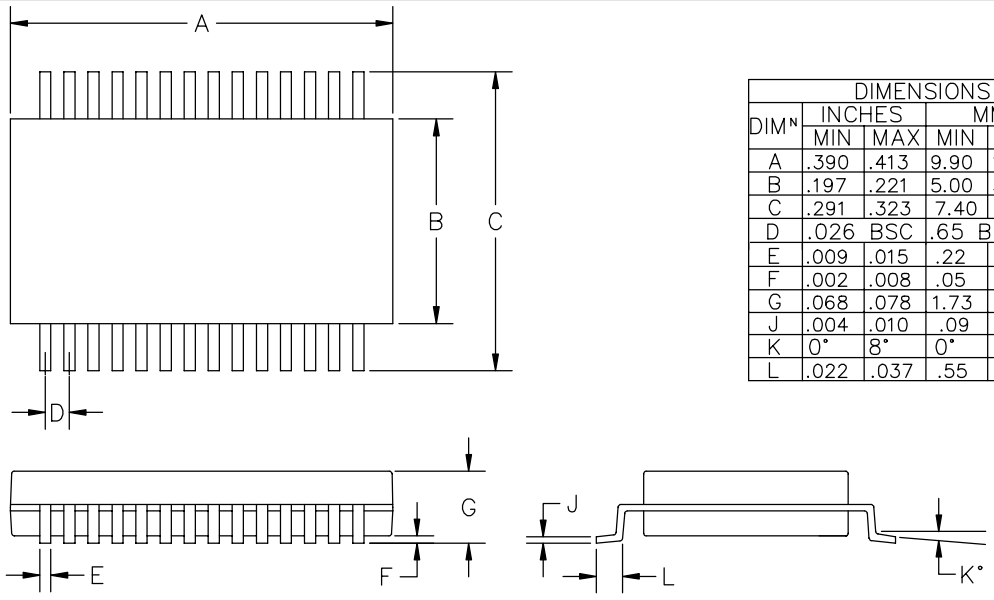


DIMENSIONS [1]					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	–	.218	–	5.53	REF
D	–	.333	–	8.45	REF
E	–	.026	–	0.65	BSC
G	.155	–	3.947	–	–
X	–	.013	–	0.323	–
Y	–	.062	–	1.583	REF
Z	–	.280	–	7.113	–

[2] GRID PLACEMENT COURTYARD IS 18 X 15 ELEMENTS (9mm X 7.5mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN THE IEC PUBLICATION 97.

[1] CONTROLLING DIMENSIONS: MILLIMETERS.

Outline Drawing - SSOP-28

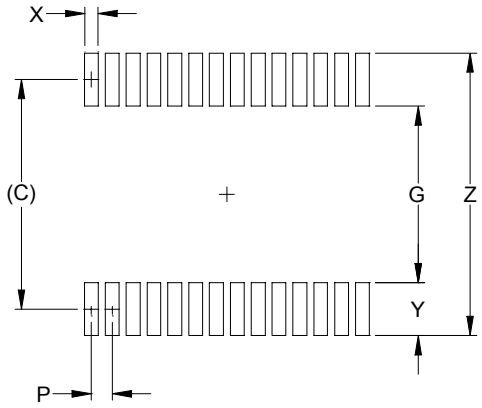


DIM	DIMENSIONS [1]				
	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.390	.413	9.90	10.50	[2]
B	.197	.221	5.00	5.60	[2]
C	.291	.323	7.40	8.20	–
D	.026 BSC		.65 BSC		–
E	.009	.015	.22	.38	–
F	.002	.008	.05	.20	–
G	.068	.078	1.73	2.00	–
J	.004	.010	.09	.25	–
K	0°	8°	0°	8°	–
L	.022	.037	.55	.95	–

[2] DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSIONS.

[1] CONTROLLING DIMENSIONS: MILLIMETERS.

Land Pattern - SSOP-28



DIM	DIMENSIONS	
	INCHES	MILLIMETERS
C	.281	(7.15)
G	.216	5.50
P	.026	0.65
X	.017	0.43
Y	.065	1.65
Z	.346	8.80

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Contact Information

Semtech Corporation
Power Management Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805)498-2111 FAX (805)498-3804