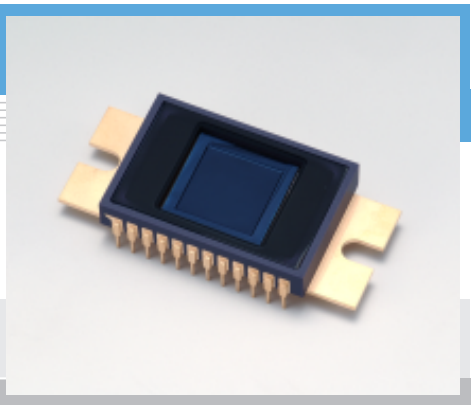
CCD area image sensor
S8844-0909

512 × 512 pixels, Back-thinned FFT-CCD



S8844-0909 is an FFT-CCD area image sensor developed for measurement of low-light-level. S8844-0909 has a back-thinned structure for detecting light from the backside that allows high sensitivity from UV to near infrared region. S8844-0909 also delivers a wide dynamic range and low dark current when operated in MPP (Multi Pinned-Phase) mode. Spectral response characteristics are very stable making high-precision photometry possible.
A one-stage thermoelectric cooler is built into the package along with the CCD chip. The CCD operating temperature can be maintained at -10 ˚C when used at room temperature (25 ˚C). S8844-0909 is identical performance and pin compatible with S7171-0909. S8844-0909 has wider FOV (Field of View) than S7171-0909 because of window structure.

Features

- Number of active pixels: 512 × 512
- Greater than 90 % quantum efficiency at peak sensitivity wavelength
- Wide spectral response range
- Low noise
- Wide dynamic range
- MPP operation
- Built-in one-stage thermoelectric cooler

Applications

- Scientific measurement
- Semiconductor inspection
- UV imaging
- Bio-photon observation
- DNA sequencer

■ Specifications

Type No.	Cooling	Number of total pixels	Number of active pixels	Active area [mm (H) × mm (V)]
S8844-0909	One-stage TE-cooled	532 × 520	512 × 512	12.288 × 12.288

■ General ratings

Parameter	Specifications
Pixel size	24 (H) × 24 (V) µm
Number of active pixels	512 (H) × 512 (V)
Vertical clock phase	2 phase
Horizontal clock phase	2 phase
Output circuit	One-stage MOSFET source follower
Package	24 pin ceramic DIP (refer to dimensional outlines)
Built-in cooler	One-stage
Window	AR coated sapphire glass *1

*1: Windowless type is available on custom order.

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■ Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	Topr	-50	-	+30	°C
Storage temperature	Tstg	-50	-	+70	°C
OD voltage	V_{OD}	-0.5	-	+25	V
RD voltage	V_{RD}	-0.5	-	+18	V
ISV voltage	V_{ISV}	-0.5	-	+18	V
ISH voltage	V_{ISH}	-0.5	-	+18	V
IGV voltage	V_{IG1V}, V_{IG2V}	-10	-	+15	V
IGH voltage	V_{IG1H}, V_{IG2H}	-10	-	+15	V
SG voltage	V_{SG}	-10	-	+15	V
OG voltage	V_{OG}	-10	-	+15	V
RG voltage	V_{RG}	-10	-	+15	V
TG voltage	V_{TG}	-10	-	+15	V
Vertical clock voltage	V_{P1V}, V_{P2V}	-10	-	+15	V
Horizontal clock voltage	V_{P1H}, V_{P2H}	-10	-	+15	V

■ Operating conditions (MPP mode, Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage		V_{OD}	18	20	22	V
Reset drain voltage		V_{RD}	11.5	12	12.5	V
Output gate voltage		V_{OG}	1	3	5	V
Substrate voltage		V_{SS}	-	0	-	V
Test point (vertical input source)		V_{ISV}	-	V_{RD}	-	V
Test point (horizontal input source)		V_{ISH}	-	V_{RD}	-	V
Test point (vertical input gate)		V_{IG1V}, V_{IG2V}	-8	0	-	V
Test point (horizontal input gate)		V_{IG1H}, V_{IG2H}	-8	0	-	V
Vertical shift register clock voltage	High	V_{P1VH}, V_{P2VH}	4	6	8	V
	Low	V_{P1VL}, V_{P2VL}	-9	-8	-7	
Horizontal shift register clock voltage	High	V_{P1HH}, V_{P2HH}	4	6	8	V
	Low	V_{P1HL}, V_{P2HL}	-9	-8	-7	
Summing gate voltage	High	V_{SGH}	4	6	8	V
	Low	V_{SGL}	-9	-8	-7	
Reset gate voltage	High	V_{RGH}	4	6	8	V
	Low	V_{RGL}	-9	-8	-7	
Transfer gate voltage	High	V_{TGH}	4	6	8	V
	Low	V_{TGL}	-9	-8	-7	

■ Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Signal output frequency	fc	-	-	1	MHz
Vertical shift register capacitance	C_{P1V}, C_{P2V}	-	6,400	-	pF
Horizontal shift register capacitance	C_{P1H}, C_{P2H}	-	120	-	pF
Summing gate capacitance	C_{SG}	-	7	-	pF
Reset gate capacitance	C_{RG}	-	7	-	pF
Transfer gate capacitance	C_{TG}	-	150	-	pF
Charge transfer efficiency *2	CTE	0.99995	0.99999	-	-
DC output level *3	Vout	12	15	18	V
Output impedance *3	Zo	-	3	-	kΩ
Power consumption *3 *4	P	-	15	-	mW

*2: Charge transfer efficiency per pixel, measured at half of the full well capacity.
*3: The values depend on the load resistance. (V_{OD}=20 V, Load resistance=22 kΩ)
*4: Power consumption of the on-chip amplifier.

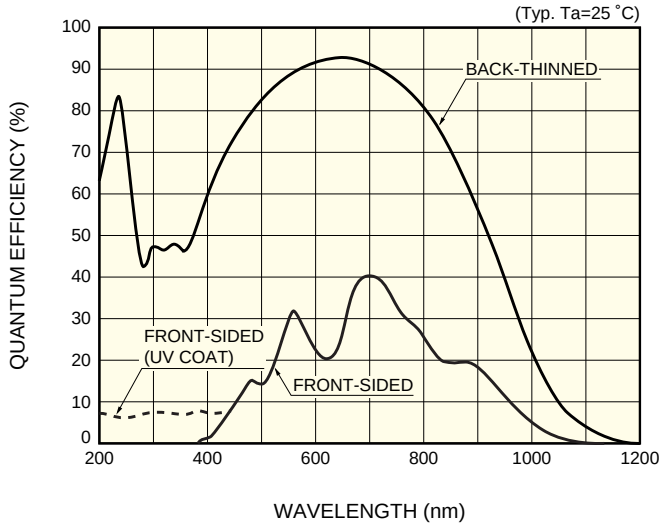
■ Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Saturation output voltage		Vsat	-	Fw × Sv	-	V
Full well capacity	Vertical	Fw	150,000	300,000	-	e^-
	Horizontal		300,000	600,000	-	
CCD node sensitivity		Sv	1.8	2.2	-	μV/e^-
Dark current *5 (MPP mode)	25 °C	DS	-	4,000	12,000	e^-/pixel/s
	0 °C		-	200	600	
Readout noise *6		Nr	-	8	16	e^- rms
Dynamic range *7	Line binning	DR	18,750	75,000	-	-
	Area scanning		9,375	37,500	-	-
Photo response non-uniformity *8		PRNU	-	±3	±10	%
Spectral response range		λ	-	200 to 1100	-	nm

*5: Dark current nearly doubles for every 5 to 7 °C increase in temperature.
*6: Operating frequency is 150 kHz.
*7: Dynamic Range (DR) = Full well/Readout noise
*8: Measured at half of the full well capacity.

$$\text{Photo Response Non-Uniformity (PRNU) [\%]} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100$$

■ Spectral response (without window) *9



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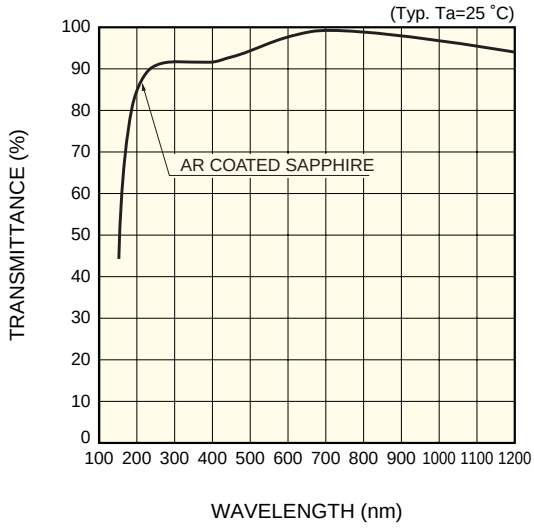
■ Spectral transmittance characteristic of window material



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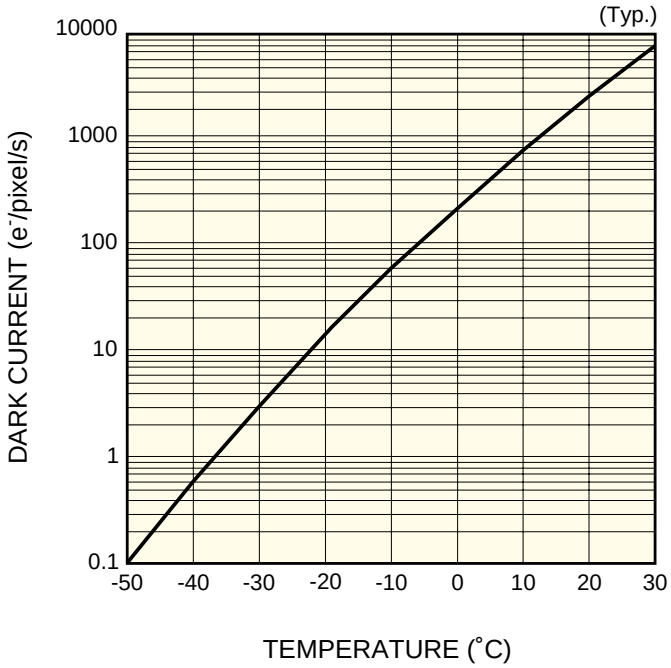
*9: Spectral response with sapphire window is decreased by the transmittance

■ Dark current vs. temperature



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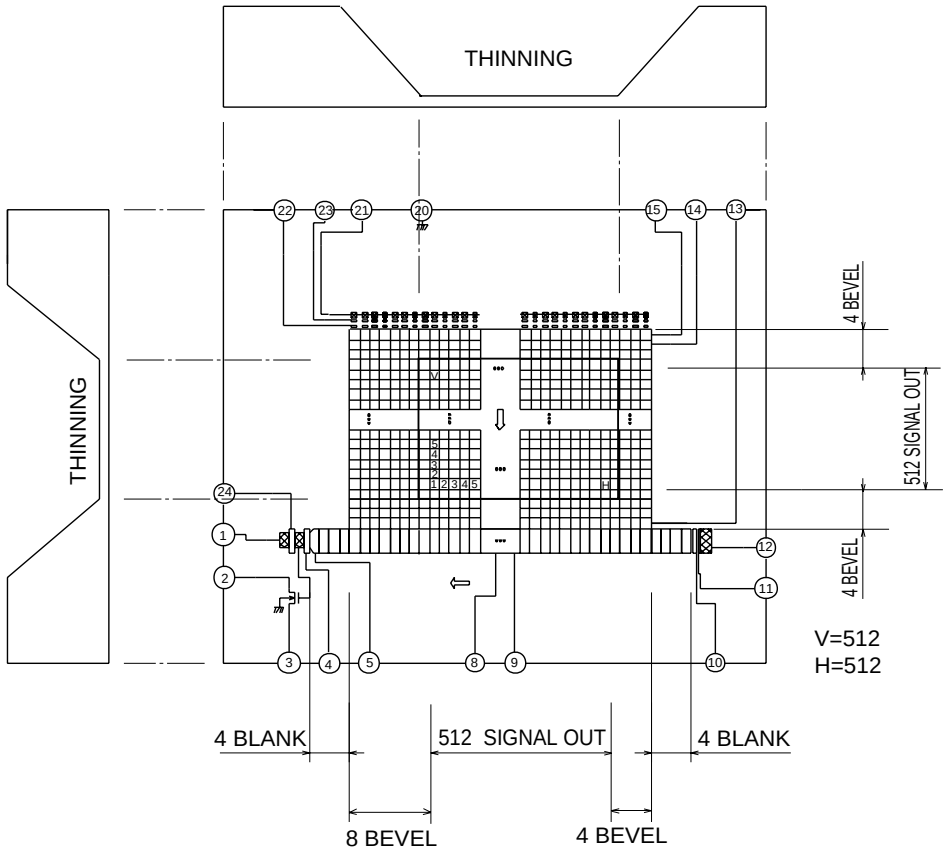
■ Device structure (Conceptual drawing of top view)



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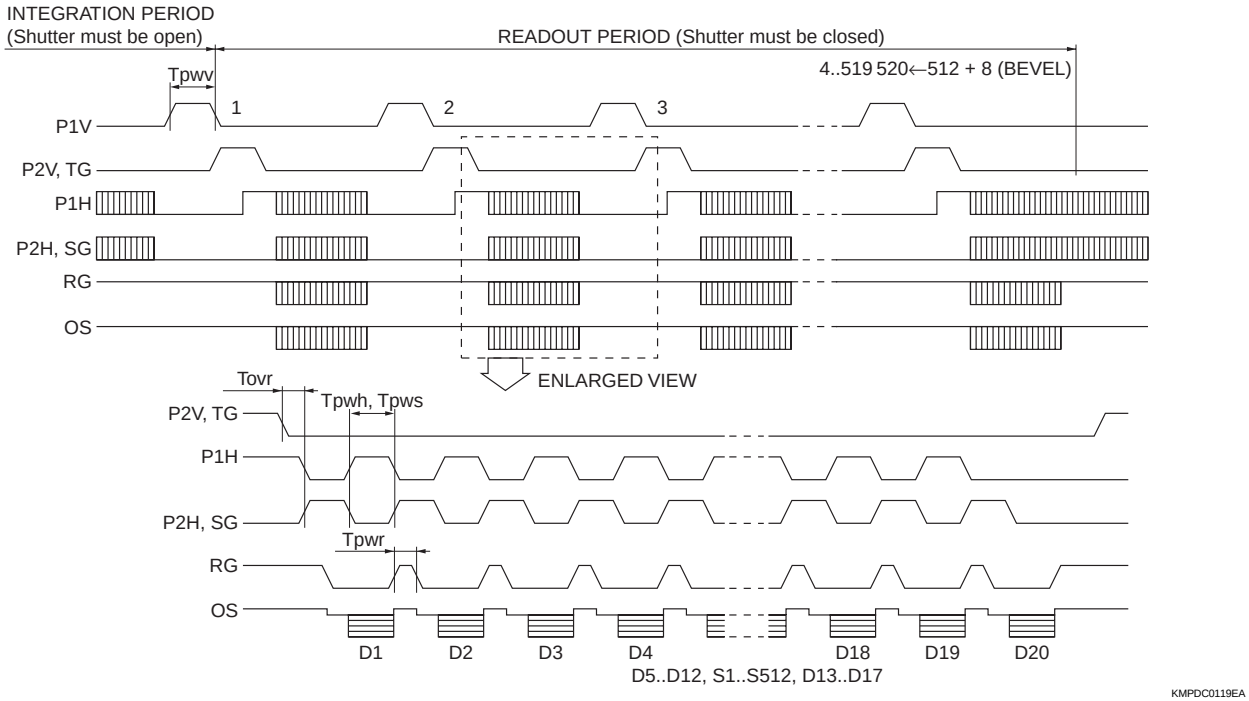
■ Timing chart

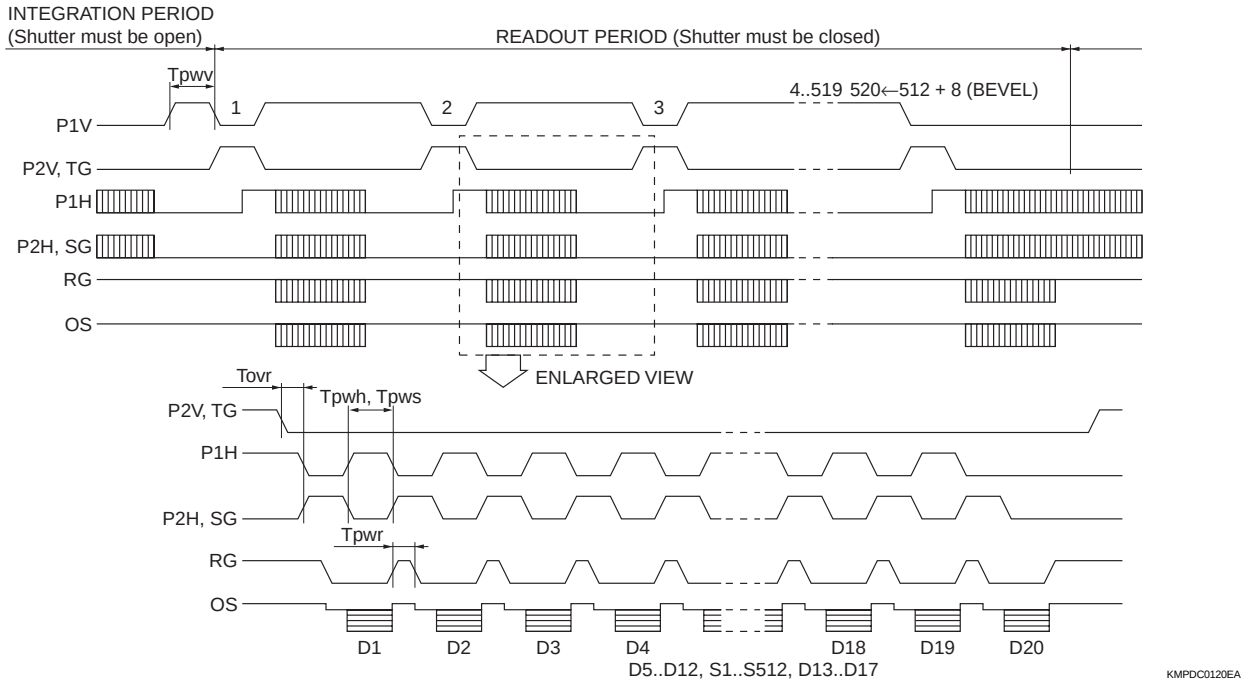
Area scanning 1 (low dark current mode)



Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1V, P2V, TG	Pulse width	Tpwv	*10	6	-	-	µs
	Rise and fall time	Tprv, Tpfv		200	-	-	ns
P1H, P2H	Pulse width	Tpwh	*10	500	-	-	ns
	Rise and fall time	Tprh, pfh		10	-	-	ns
	Duty ratio	-		-	50	-	%
SG	Pulse width	Tpws	-	500	-	-	ns
	Rise and fall time	Tprs, Tpfs		10	-	-	ns
	Duty ratio	-		-	50	-	%
RG	Pulse width	Tpwr	-	100	-	-	ns
	Rise and fall time	Tprr, Tpfr		5	-	-	ns
TG – P1H	Overlap time	Tovr	-	3	-	-	µs

*10: Symmetrical clock pulses should be overlapped at 50 % of maximum amplitude.

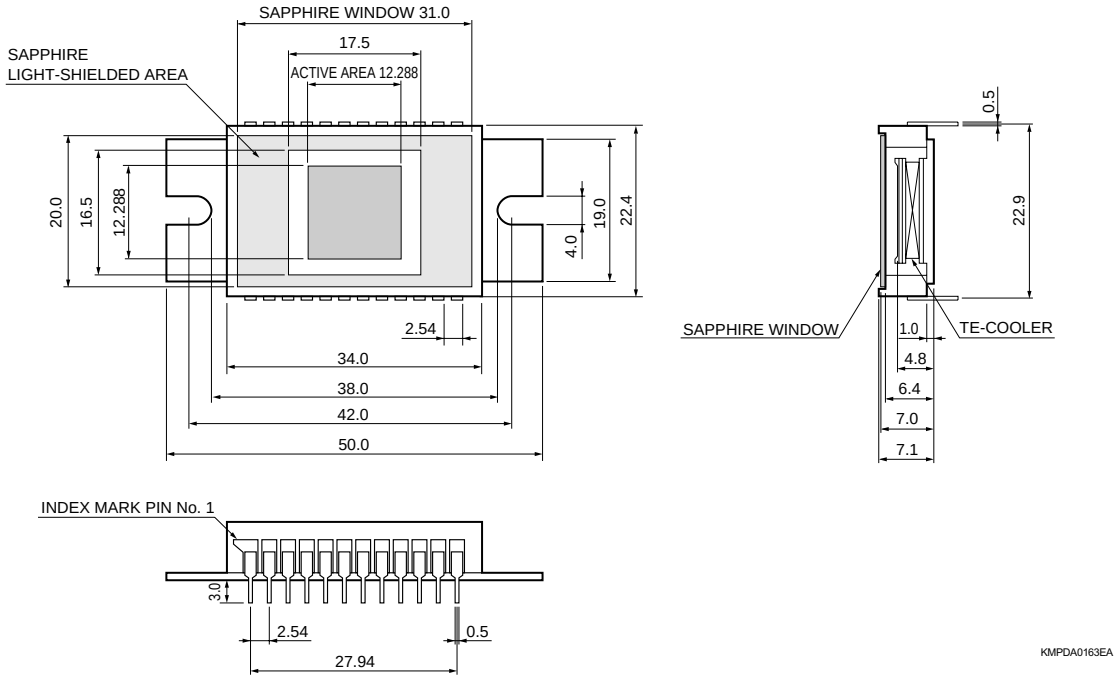
Area scanning 2 (large full well mode)



Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1V, P2V, TG	Pulse width	Tpwv	*11	6	-	-	µs
	Rise and fall time	Tprv, Tpfv		200	-	-	ns
P1H, P2H	Pulse width	Tpwh	*11	500	-	-	ns
	Rise and fall time	Tprh, Tpfh		10	-	-	ns
	Duty ratio	-		-	50	-	%
SG	Pulse width	Tpws	-	500	-	-	ns
	Rise and fall time	Tprs, Tpfs		10	-	-	ns
	Duty ratio	-		-	50	-	%
RG	Pulse width	Tpwr	-	100	-	-	ns
	Rise and fall time	Tprr, Tpfr		5	-	-	ns
TG - P1H	Overlap time	Tovr	-	3	-	-	µs

*11: Symmetrical clock pulses should be overlapped at 50 % of maximum amplitude.

■ Dimensional outline (unit: mm)



■ Pin connections

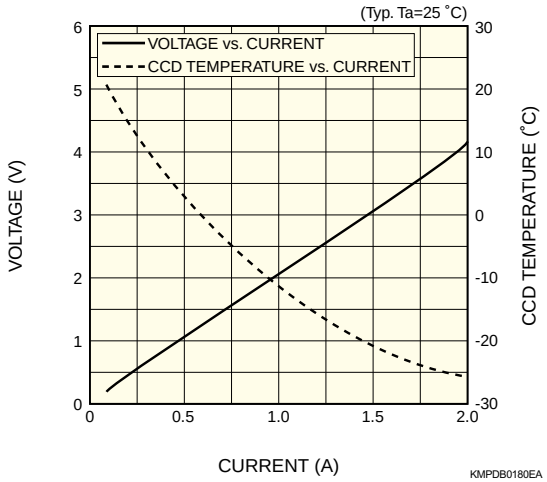
Pin No.	Symbol	Function	Remark (standard operation)
1	RD	Reset drain	+12 V
2	OS	Output transistor source	R_L=10 k to 100 kΩ
3	OD	Output transistor drain	+20 V
4	OG	Output gate	+3 V
5	SG	Summing gate	Same timing as P2H
6	-		
7	-		
8	P2H	CCD horizontal register clock-2	
9	P1H	CCD horizontal register clock-1	
10	IG2H	Test point (horizontal input gate-2)	0 V
11	IG1H	Test point (horizontal input gate-1)	0 V
12	ISH	Test point (horizontal input source)	Connect to RD
13	TG *12	Transfer gate	Same timing as P2V
14	P2V	CCD vertical register clock-2	
15	P1V	CCD vertical register clock-1	
16	Th1	Thermistor	
17	Th2	Thermistor	
18	P-	TE-cooler (-)	
19	P+	TE-cooler (+)	
20	SS	Substrate (GND)	GND
21	ISV	Test point (vertical input source)	Connect to RD
22	IG2V	Test point (vertical input gate-2)	0 V
23	IG1V	Test point (vertical input gate-1)	0 V
24	RG	Reset gate	

*12: Isolation gate between vertical register and horizontal register. In standard operation, TG should be applied the same pulse as P2V.

■ Specifications of built-in TE-cooler

Parameter	Symbol	Condition	Typ.	Unit
Internal resistance	Rint	Ta=25 °C	2.1	Ω
Maximum current *13	Imax	Tc *14=Th *15=25 °C	2.0	A
Maximum voltage	Vmax	Tc *14=Th *15=25 °C	4.2	V
Maximum heat absorption *16	Qmax		4.5	W
Maximum temperature of heat radiating side	-		70	°C

*13: Maximum current Imax:
If the current greater than this value flows into the thermoelectric cooler, the heat absorption begins to decrease due to the Joule heat. It should be noted that this value is not the damage threshold value. To protect the thermoelectric cooler and maintain stable operation, the supply current should be less than 60 % of this maximum current.
*14: Temperature of the cooling side of thermoelectric cooler.
*15: Temperature of the heat radiating side of thermoelectric cooler.
*16: Maximum heat absorption Qmax.
This is a theoretical heat absorption level that offsets the temperature difference in the thermoelectric cooler when the maximum current is supplied to the unit.



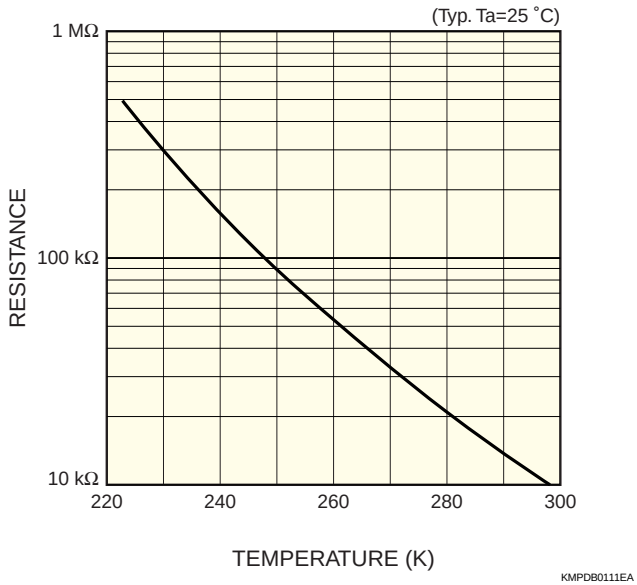
■ Specifications of built-in temperature sensor

A chip thermistor is built in the same package with a CCD chip, and the CCD chip temperature can be monitored with it. A relation between the thermistor resistance and absolute temperature is expressed by the following equation.

$$R1 = R2 \times \exp B\left(\frac{1}{T1} - \frac{1}{T2}\right)$$

R1: Resistance at absolute temperature T1 (K)
R2: Resistance at absolute temperature T2 (K)
B: B constant (K)

The characteristics of the thermistor used are as follows.
R (298K) = 10 kΩ
B (298K / 323K) = 3450 K



■ Precaution for use (Electrostatic countermeasures)

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

■ Element cooling/heating temperature incline rate

Element cooling/heating temperature incline rate should be set at less than 5 K/min.

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