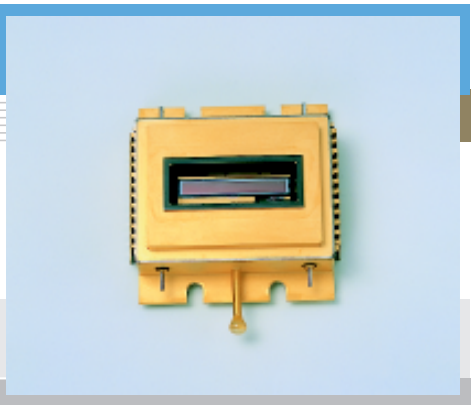

CCD area image sensor
S7017 series

Four-stage TE-cooled, front-illuminated FFT-CCDs

S7017 series is a family of FFT-CCD area image sensors specifically designed for low-light-level detection in scientific applications. By using the binning operation, S7017 series can be used as a linear image sensor having a long aperture in the direction of the device length. This makes S7017 series ideally suited for use in spectrophotometry. The binning operation offers significant improvement in S/N and signal processing speed compared with conventional methods by which signals are digitally added by an external circuit. S7017 series also features low noise and low dark signal (MPP mode operation). These enable low-light-level detection and long integration time, thus achieving a wide dynamic range.
S7017 series has a pixel size of 24 × 24 µm and is available in active area of 24.576 (H) × 2.976 (V) and 24.576 (H) × 6.048 (V) mm.
A four-stage Peltier element is built into the same package for thermoelectric cooling. At room temperature operation, the device can be cooled down to -70 ˚C with using forced air cooling. In addition, since both the CCD chip and Peltier element are hermetically sealed, no dry air is required, thus allowing easy handling.

Features

- 1024 (H) × 124 (V) and 1024 (H) × 252 (V) pixel format
- Pixel size: 24 × 24 µm
- 100 % fill factor
- Wide dynamic range
- Low dark current
- Low readout noise
- MPP operation
- Four-stage TE-cooled

Applications

- Astronomy
- Scientific measuring instrument
- Fluorescence spectrometer
- Raman spectrophotometer
- Optical and spectrophotometric analyzer
- For low-light-level detection requiring

■ Selection and order guide

Type No.	Cooling	Number of total pixels	Number of active pixels	Active area [mm (H) × mm (V)]
S7017-1007	Four-stage TE-cooled	1044 × 128	1024 ×124	24.576 × 2.976
S7017-1008		1044 × 256	1024 × 252	24.576 × 6.048

S7017 series has a hermetically-sealed package with AR-coated sapphire window.

■ General ratings

Parameter	Specification
CCD structure	Full frame transfer
Fill factor	100 %
Number of active pixels	S7017-1007: 1024 (H) × 124 (V) S7017-1008: 1024 (H) × 252 (V)
Pixel size	24 (H) × 24 (V) µm
Active area	S7017-1007: 24.576 (H) × 2.976 (V) mm S7017-1008: 24.576 (H) × 6.048 (V) mm
Vertical clock phase	2 phase
Horizontal clock phase	2 phase
Output circuit	One-stage MOSFET source follower
Package	28 pin metal package
Window	AR coated Sapphire

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■ Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	Topr	-50	-	+30	°C
Storage temperature	Tstg	-100	-	+70	°C
OD voltage	V_{OD}	-0.5	-	+25	V
RD voltage	V_{RD}	-0.5	-	+18	V
ISV voltage	V_{ISV}	-0.5	-	+18	V
ISH voltage	V_{ISH}	-0.5	-	+18	V
IGV voltage	V_{IG1V}, V_{IG2V}	-10	-	+15	V
IGH voltage	V_{IG1H}, V_{IG2H}	-10	-	+15	V
SG voltage	V_{SG}	-10	-	+15	V
OG voltage	V_{OG}	-10	-	+15	V
RG voltage	V_{RG}	-10	-	+15	V
TG voltage	V_{TG}	-10	-	+15	V
Vertical clock voltage	V_{P1V}, V_{P2V}	-10	-	+15	V
Horizontal clock voltage	V_{P1H}, V_{P2H}	-10	-	+15	V

■ Operating conditions (MPP mode, Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage		V_{OD}	18	20	22	V
Reset drain voltage		V_{RD}	11.5	12	12.5	V
Output gate voltage		V_{OG}	1	3	5	V
Substrate voltage		V_{SS}	-	0	-	V
Test point (vertical input source)		V_{ISV}	-	V_{RD}	-	V
Test point (horizontal input source)		V_{ISH}	-	V_{RD}	-	V
Test point (vertical input gate)		V_{IG1V}, V_{IG2V}	-8	0	-	V
Test point (horizontal input gate)		V_{IG1H}, V_{IG2H}	-8	0	-	V
Vertical shift register clock voltage	High	V_{P1VH}, V_{P2VH}	4	6	8	V
	Low	V_{P1VL}, V_{P2VL}	-9	-8	-7	
Horizontal shift register clock voltage	High	V_{P1HH}, V_{P2HH}	4	6	8	V
	Low	V_{P1HL}, V_{P2HL}	-9	-8	-7	
Summing gate voltage	High	V_{SGH}	4	6	8	V
	Low	V_{SGL}	-9	-8	-7	
Reset gate voltage	High	V_{RGH}	4	6	8	V
	Low	V_{RGL}	-9	-8	-7	
Transfer gate voltage	High	V_{TGH}	4	6	8	V
	Low	V_{TGL}	-9	-8	-7	

■ Electrical characteristics (Ta=25 °C)

Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
Signal output frequency		fc	-	-	80	2,000	kHz
Reset clock frequency		frg	-	-	80	2,000	kHz
Vertical shift register capacitance	S7017-1007	C_{P1V}, C_{P2V}	-	-	3,200	-	pF
	S7017-1008		-	-	6,400	-	
Horizontal shift register capacitance		C_{P1H}, C_{P2H}	-	-	300	-	pF
Summing gate capacitance		C_{SG}	-	-	7	-	pF
Reset gate capacitance		C_{RG}	-	-	7	-	pF
Transfer gate capacitance		C_{TG}	-	-	150	-	pF
Transfer efficiency		CTE	*1	0.99995	0.99999	-	-
DC output level		Vout	*2	12	15	18	V
Output impedance		Zo	*2	-	3	-	kΩ
Power dissipation		P	*2, *3	-	15	-	mW

*1: Charge transfer efficiency per pixel, measured at half of the full well capacity.
*2: V_{OD}=20 V , Load resistance=22 kΩ
*3: Power dissipation of the on-chip amplifier.

■Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
Saturation output voltage		Vsat	-	-	Fw × Sv	-	V
Full well capacity	Vertical	Fw	*4	150	300	-	ke⁻
	Horizontal			300	600	-	
CCD conversion efficiency		Sv	*5	1.8	2.2	-	μV/e⁻
Dark current (MPP mode)	+25 °C	DS	*6	-	400	3,000	e⁻/pixel/s
	0 °C			-	20	150	
	-70 °C			-	0.0015	0.01	
Readout noise		Nr	*7	-	6	12	e⁻rms
Dynamic range	Line binning	DR	*8	25,000	75,000	-	-
	Area scanning			12,500	37,500	-	
Spectral response range		λ	-	-	400 to 1,100	-	nm
Photo response non-uniformity		PRNU	*9	-	-	±10	%
Blemish	Point defects	-	*10	-	-	0	-
	Cluster defects		*11	-	-	0	
	Column defects		*12	-	-	0	

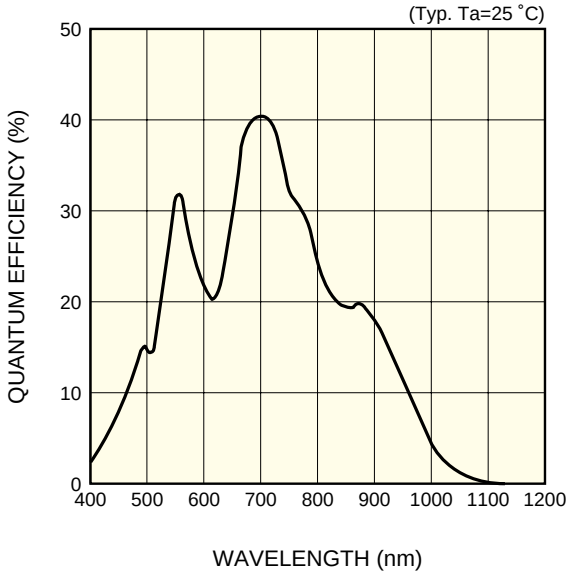
*4: Large horizontal full well for line binning operation.
*5: V_{OD}=20 V , Load resistance=22 kΩ
*6: Dark current nearly doubles for every 5 to7 °C increase in temperature.
*7: -40 °C, operating frequency is 80 kHz.
*8: DR = Fw / Nr
*9: Measured at half of the full well capacity. PRNU (%) = noise / signal × 100, noise: fixed pattern noise (peak to peak)
*10: White spots > 3 % of full well at 0 °C after Ts=1 s, Black spots > 50 % reduction in response relative to adjacent pixels
*11: continuous 2 to 9 point defects
*12: continuous >10 point defects

■ PIN connections

Pin No.	Symbol	Description	Remark
1	P-	TE-cooler-	
2	NC		
3	SS	Substrate (GND)	
4	NC		
5	ISV	Test point (vertical input source)	Shorted to RD
6	IG2V	Test point (vertical input gate-2)	Shorted to 0 V
7	IG1V	Test point (vertical input gate-1)	Shorted to 0 V
8	RG	Reset gate	
9	RD	Reset drain	
10	OS	Output transistor source	
11	OD	Output transistor drain	
12	OG	Output gate	
13	SG	Summing gate	Same timing as P2H
14	P+	TE-cooler+	
15	TSH1	Temperature sensor (hot side)	
16	TSC1	Temperature sensor (cool side)	
17	TSC2	Temperature sensor (cool side)	
18	P2H	CCD horizontal register clock-2	
19	P1H	CCD horizontal register clock-1	
20	IG2H	Test point (horizontal input gate-2)	Shorted to 0 V
21	IG1H	Test point (horizontal input gate-1)	Shorted to 0 V
22	ISH	Test point (horizontal input source)	Shorted to RD
23	P2V	CCD vertical register clock-2	
24	P1V	CCD vertical register clock-1	
25	TG	Transfer gate	Same timing as P2V *13
26	NC		
27	NC		
28	TSH2	Temperature sensor (hot side)	

*13: TG is an isolation gate between vertical register and horizontal resister.
In standard operation, the same pulse of P2V should be applied to the TG.

■ Spectral response without window



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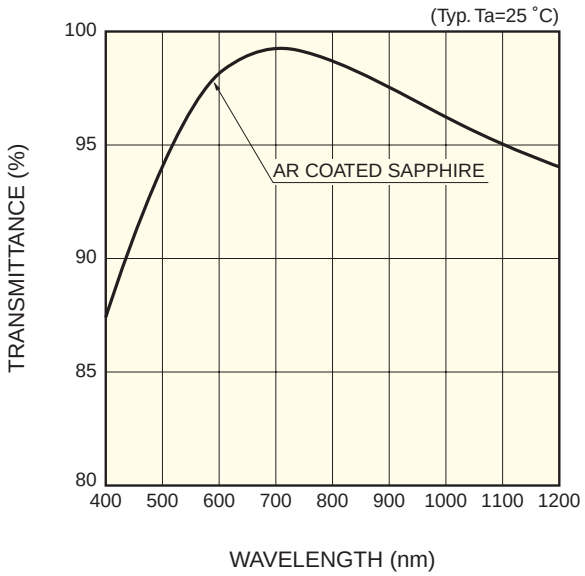
■ Spectral transmittance characteristic of window material



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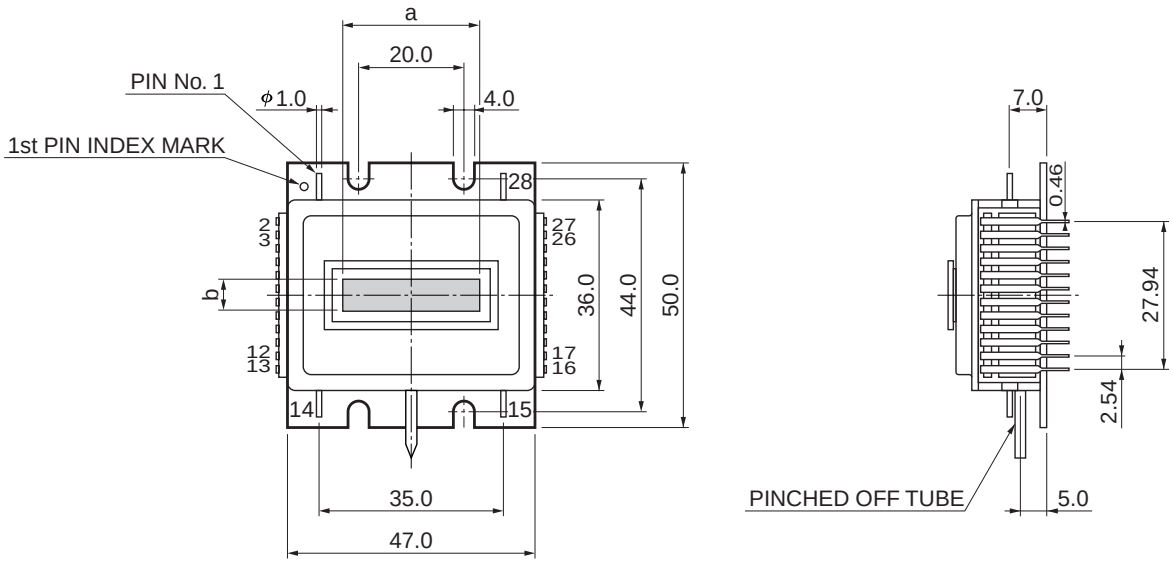
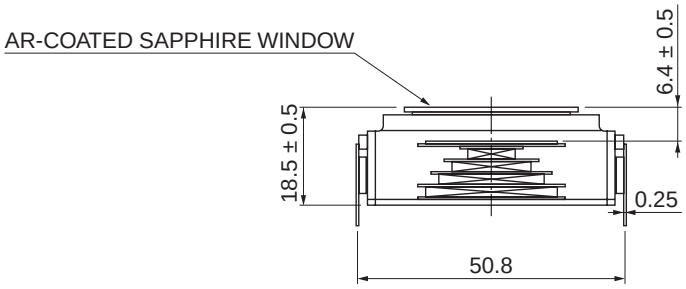
■ Dimensional outline (unit: mm)

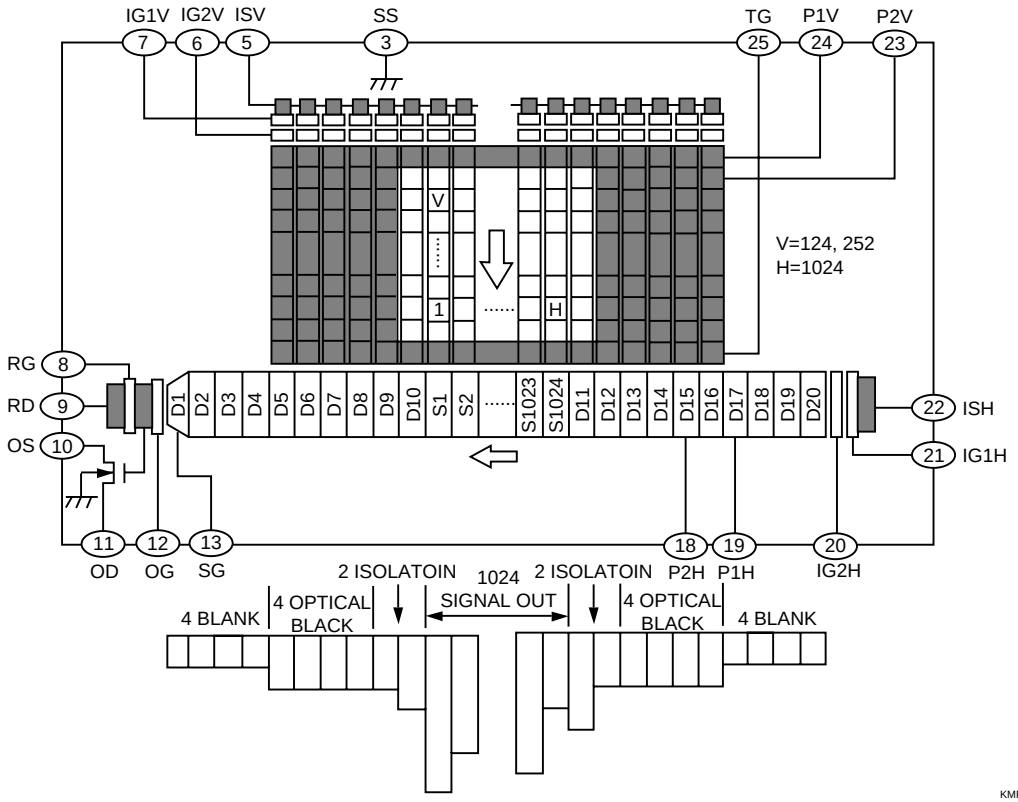




TYPE No.	ACTIVE AREA	
	a	b
S7017-1007	24.576 (H)	2.976 (V)
S7017-1008	24.576 (H)	6.048 (V)

KMPDA0098EA

■ Device structure, line output format



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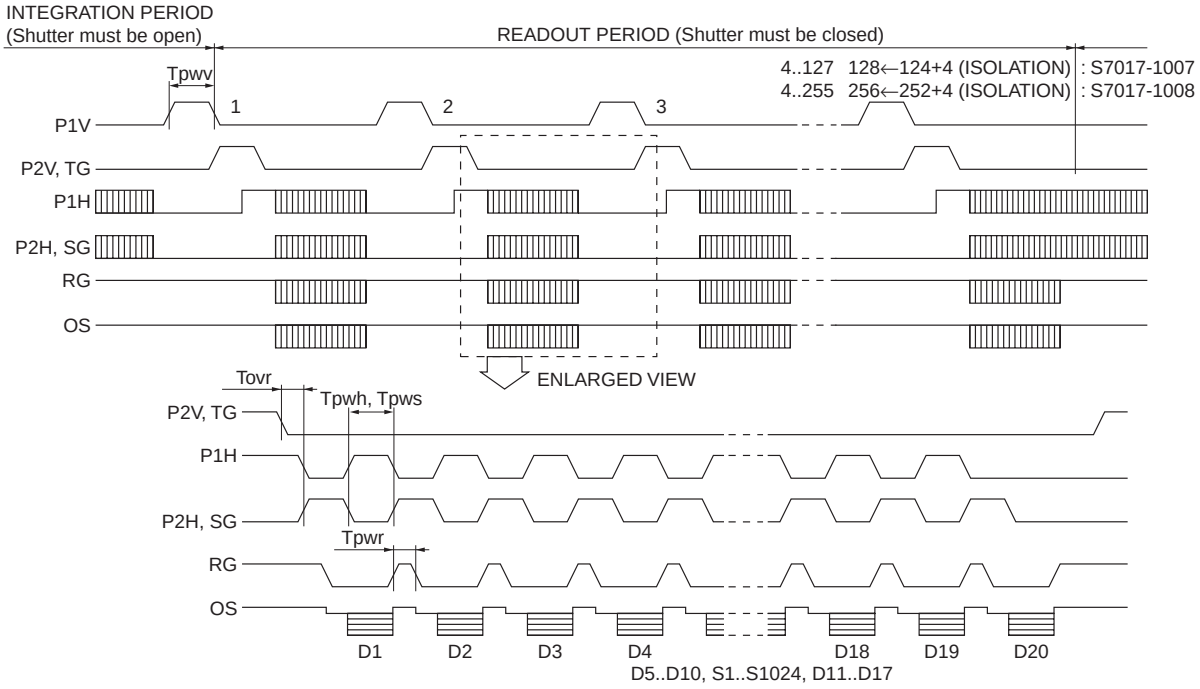
Pixel format

Left ← Horizontal Direction → Right						
Blank	Optical Black	Isolation	Effective	Isolation	Optical Black	Blank
4	4	2	1024	2	4	4

Top ← Vertical Direction → Bottom		
Isolation	Effective	Isolation
2	124 or 252	2

■ Timing chart

● Area scanning 1 (low dark current mode)



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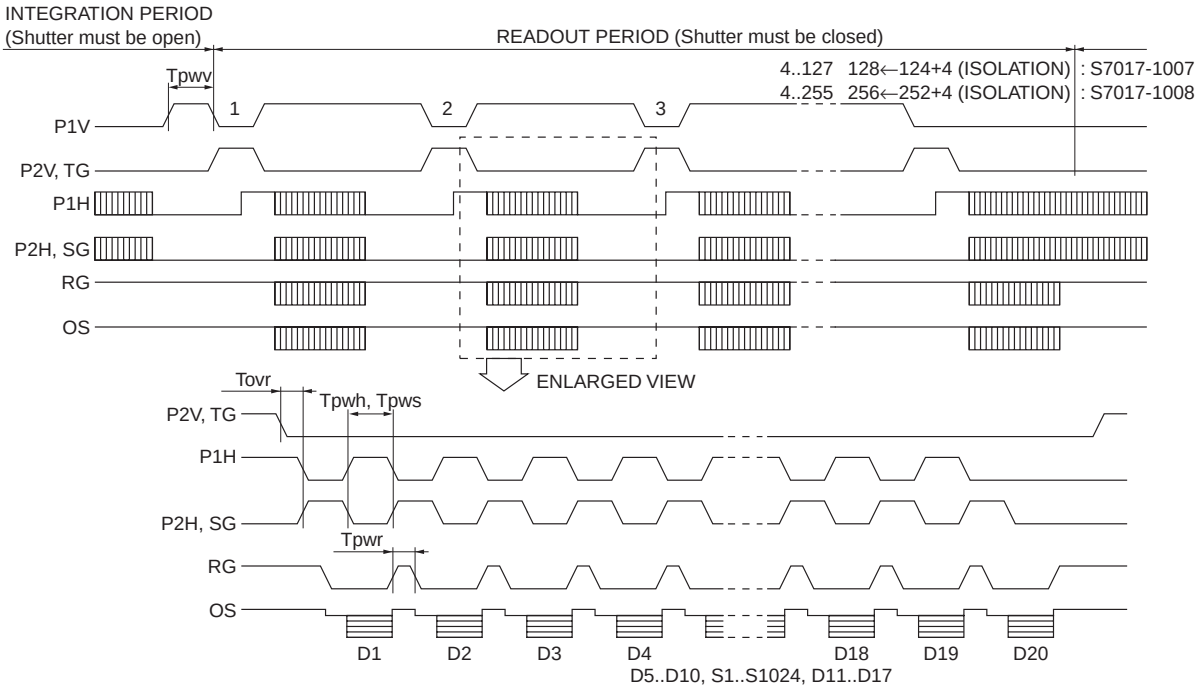
Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1V, P2V, TG	Pulse width	Tpwv	*14	6 *15	-	-	µs
	Rise and fall time	Tprv, Tpfv		200	-	-	ns
P1H, P2H	Pulse width	Tpwh	*14	250	-	-	ns
	Rise and fall time	Tprh, pfh		10	-	-	ns
	Duty ratio	-		-	50	-	%
SG	Pulse width	Tpws	-	250	-	-	ns
	Rise and fall time	Tprs, Tpfs		10	-	-	ns
	Duty ratio	-		-	50	-	%
RG	Pulse width	Tpwr	-	100	-	-	ns
	Rise and fall time	Tprr, Tpfr		5	-	-	ns
TG – P1H	Overlap time	Tovr	-	3	-	-	µs

*14: Symmetrical pulses should be overlapped at 50 % of maximum amplitude.
*15: In case of S7017-1007.

● Area scanning 2 (large full well mode)

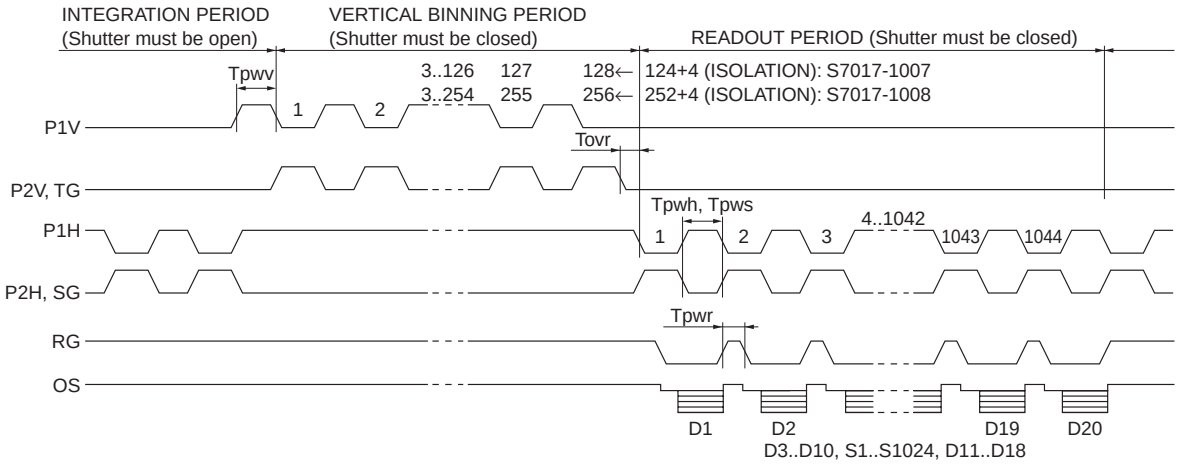


KMPDC0100EA

Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1V, P2V, TG	Pulse width	Tpwv	*16	6 *17	-	-	µs
	Rise and fall time	Tprv, Tpfv		200	-	-	ns
P1H, P2H	Pulse width	Tpwh	*16	250	-	-	ns
	Rise and fall time	Tprh, Tpfh		10	-	-	ns
	Duty ratio	-		-	50	-	%
SG	Pulse width	Tpws	-	250	-	-	ns
	Rise and fall time	Tprs, Tpfs		10	-	-	ns
	Duty ratio	-		-	50	-	%
RG	Pulse width	Tpwr	-	100	-	-	ns
	Rise and fall time	Tprr, Tpfr		5	-	-	ns
TG - P1H	Overlap time	Tovr	-	3	-	-	µs

*16: Symmetrical pulses should be overlapped at 50 % of maximum amplitude.
*17: In case of S7017-1007.

● Line binning



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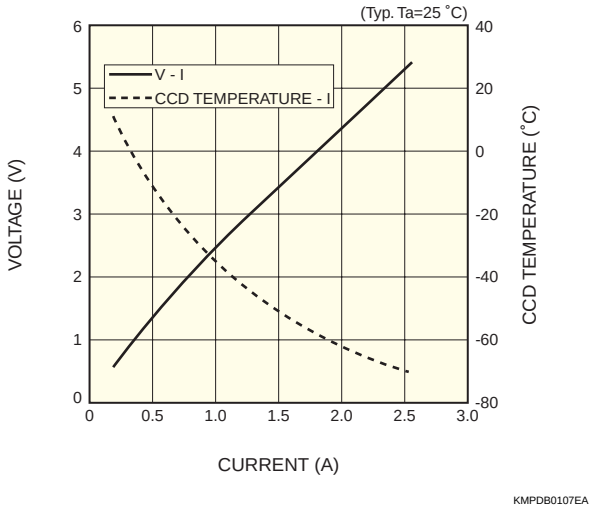
Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1V, P2V, TG	Pulse width	Tpwv	*18	6 *19	-	-	µs
	Rise and fall time	Tprv, Tpfv		200	-	-	ns
P1H, P2H	Pulse width	Tpwh	*18	250	-	-	ns
	Rise and fall time	Tprh, Tpfh		10	-	-	ns
	Duty ratio	-		-	50	-	%
SG	Pulse width	Tpws	-	250	-	-	ns
	Rise and fall time	Tprs, Tpfs		10	-	-	ns
	Duty ratio	-		-	50	-	%
RG	Pulse width	Tpwr	-	100	-	-	ns
	Rise and fall time	Tprr, Tpfr		5	-	-	ns
TG – P1H	Overlap time	Tovr	-	3	-	-	µs

*18: Symmetrical pulses should be overlapped at 50 % of maximum amplitude.
*19: In case of S7017-1007.

■ Specifications of built-in TE-cooler

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal resistance	Rint	Ta=27 °C	-	1.6	-	Ω
Maximum current *20	Imax	Th *21=27 °C ΔT *22=ΔTmax	-	-	4.4	A
Maximum voltage	Vmax	Th*21=27 °C ΔT=ΔTmax I=Imax	-	-	7.4	V
Maximum heat absorption *23	Qmax	Tc *24=Th *21=27 °C I=Imax	-	-	3.0	W
Maximum temperature at hot side	-		-	-	50	°C
CCD temperature	-	Ta=25 °C	-	-70	-50	°C

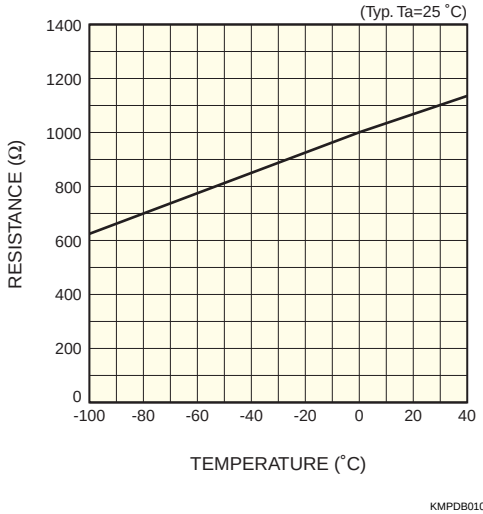
*20: If the current is greater than Imax, the heat absorption begins to decrease due to the Joule heat. It should be noted that this value is not a damage threshold. To protect the thermoelectric cooler (Peltier element) and maintain stable operation, the supply current should be less than 60 % of this maximum current.
*21: Temperature at hot side of thermoelectric cooler.
*22: ΔT=Th - Tc
*23: This is a theoretical heat absorption level that offsets the temperature difference in the Peltier element when the maximum current is supplied to the unit.
*24: Temperature at cool side of thermoelectric cooler.



KMPDB0107EA

■ Specifications of built-in temperature sensors

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resistance at cool side	Rc	T=0 °C	-	1,000	-	Ω
Temperature coefficient of resistance at cool side	-	-	-	0.00375	-	Ω/Ω
Resistance at hot side	Rh	T=0 °C	-	1,000	-	Ω
Temperature coefficient of resistance at hot side	-	-	-	0.00385	-	Ω/Ω



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■ Precaution for use (electrostatic countermeasures)

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

■ Element cooling/heating temperature incline rate

Element cooling/heating temperature incline rate should be set at less than 5 K/min.

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