



DP80C51

Pipelined High Performance 8-bit Microcontroller ver 4.01

OVERVIEW

DP80C51 is an **ultra high performance, speed optimized** soft core of a single-chip 8-bit embedded controller dedicated for operation with **fast** (typically on-chip) and **slow** (off-chip) **memories**. The core has been designed with a special concern for **performance to power consumption** ratio. This ratio is extended by an advanced power management unit **PMU**.

DP80C51 soft core is 100% binary and **pin compatible** with the industry standard 8051 8-bit microcontroller. There are two configurations of the DP80C51: **Harward**, where external data and program buses are separated, and **von Neumann**, with common program and external data bus. DP80C51 has Pipelined RISC architecture up to **10 times faster** compared to standard architecture and executes **85-200 million instructions** per second. This performance can also be exploited to great advantage in **low power** applications where the core can be clocked over ten times more slower than the original implementation for no performance penalty.

DP80C51 is delivered with **fully automated testbench** and **complete set of tests** allowing easy package validation at each stage of SoC design flow.

CPU FEATURES

- 100% pin compatible with industry standard 8051
- 100% software compatible with industry standard 8051
- Pipelined RISC architecture enables to execute instructions up to 10 times faster compared to standard 8051
- 24 times faster multiplication
- 12 times faster addition
- Up to 256 bytes of internal (on-chip) Data Memory
- Up to 64K bytes of internal (on-chip) or external (off-chip) Program Memory
- Up to 64K bytes of external (off-chip) Data Memory
- User programmable Program Memory Wait States solution for wide range of memories speed
- User programmable External Data Memory Wait States solution for wide range of memories speed
- Dedicated signal for Program Memory writes.
- Interface for additional Special Function Registers

- Fully synthesizable, static synchronous design with positive edge clocking and no internal tri-states
- Scan test ready
- **2.0 GHz virtual** clock frequency in a 0.25u technological process

PERIPHERALS

- DoCD™ debug unit
 - Processor execution control
 - Run
 - Halt
 - Step into instruction
 - Skip instruction
 - Read-write all processor contents
 - Program Counter (PC)
 - Program Memory
 - Internal (direct) Data Memory
 - Special Function Registers (SFRs)
 - External Data Memory
 - Code execution breakpoints
 - one real-time PC breakpoint
 - unlimited number of real-time OPCODE breakpoints
 - Hardware execution watch-point
 - one at Internal (direct) Data Memory
 - one at Special Function Registers (SFRs)
 - one at External Data Memory
 - Hardware watch-points activated at a certain address by any write into memory
 - Hardware watch-points activated at a certain address by any read from memory
 - Hardware watch-points activated at a certain address by write into memory a required data
 - Hardware watch-points activated at a certain address by read from memory a required data
 - Unlimited number of software watch-points
 - Internal (direct) Data Memory
 - Special Function Registers (SFRs)
 - External Data Memory
 - Unlimited number of software breakpoints
 - Program Memory(PC)
 - Automatic adjustment of debug data transfer speed rate between HAD and Silicon
 - JTAG Communication interface
- Power Management Unit
 - Power management mode
 - Switchback feature
 - Stop mode
- Interrupt Controller
 - 2 priority levels
 - 2 external interrupt sources
 - 3 interrupt sources from peripherals
- Four 8-bit I/O Ports
 - Bit addressable data direction for each line
 - Read/write of single line and 8-bit group
- Two 16-bit timer/counters
 - Timers clocked by internal source
 - Auto reload 8-bit timers
 - Externally gated event counters
- Full-duplex serial port

- Synchronous mode, fixed baud rate
- 8-bit asynchronous mode, fixed baud rate
- 9-bit asynchronous mode, fixed baud rate
- 9-bit asynchronous mode, variable baud rate

CONFIGURATION

The following parameters of the DP80C51 core can be easily adjusted to requirements of dedicated application and technology. Configuration of the core can be prepared by effortlessly changing appropriate constants in package file. There is no need to change any parts of the code.

- Internal Program Memory
 - synchronous
 - asynchronous
- Internal Program ROM
 - Memory size
 - 0 - 64kB
- Internal Program RAM
 - Memory size
 - 0 - 64kB
- Interrupts
 - subroutines location
- Power Management Mode
 - used
 - unused
- Stop mode
 - used
 - unused
- DoCD™ debug unit
 - used
 - unused

Besides mentioned above parameters all available peripherals and external interrupts can be excluded from the core by changing appropriate constants in package file.

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DELIVERABLES

- ◆ Source code:
 - ◇ VHDL Source Code or/and
 - ◇ VERILOG Source Code or/and
 - ◇ Encrypted, or plain text EDIF netlist
- ◆ VHDL & VERILOG test bench environment
 - ◇ NCSim automatic simulation macros
 - ◇ ModelSim automatic simulation macros
 - ◇ Active-HDL automatic simulation macros
 - ◇ Tests with reference responses
- ◆ Technical documentation
 - ◇ Installation notes
 - ◇ HDL core specification
 - ◇ Datasheet
- ◆ Synthesis scripts
- ◆ Example application
- ◆ Technical support
 - ◇ IP Core implementation support
 - ◇ 3 months maintenance
 - Delivery the IP Core updates, minor and major versions changes
 - Delivery the documentation updates
 - Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods without royalty fees make using of IP Core easy and simply.

Single Design license allows using IP Core in single FPGA bitstream and ASIC implementation. It also permits FPGA prototyping before ASIC production.

Unlimited Designs license allows using IP Core in unlimited number of FPGA bitstreams and ASIC implementations.

In all cases number of IP Core instantiations within a design, and number of manufactured chips are unlimited. There is no time of use limitations.

- Single Design license for
 - VHDL, Verilog source code called HDL Source
 - Encrypted, or plain text EDIF called Netlist
- Unlimited Designs license for
 - HDL Source
 - Netlist
- Upgrade from
 - Netlist to HDL Source
 - Single Design to Unlimited Designs

DESIGN FEATURES

- ◆ **PROGRAM MEMORY:**

The DP80C51 soft core is dedicated for operation with Internal and External Program Memory. Internal Program Memory can be implemented as:

 - ROM located in address range between $0x0000 \div (ROM_{size}-1)$
 - RAM located in address range between $(RAM_{size}-1) \div 0xFFFF$

External Program Memory can be implemented as ROM or RAM located in address range between $ROM_{size} \div RAM_{size}$.
- ◆ **INTERNAL DATA MEMORY:**

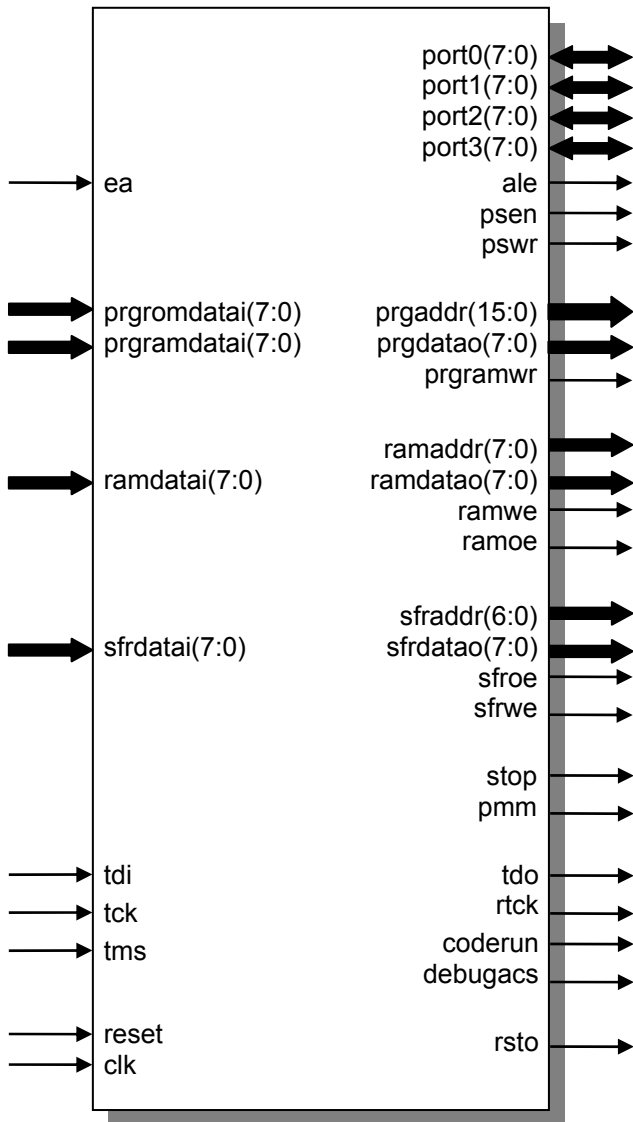
The DP80C51 can address Internal Data Memory of up to 256 bytes The Internal Data Memory can be implemented as Single-Port synchronous RAM.
- ◆ **EXTERNAL DATA MEMORY:**

The DP80C51 soft core can address up to 64 kB of External Data Memory.
- ◆ **USER SPECIAL FUNCTION REGISTERS:**

Up to 104 External (user) Special Function Registers (ESFRs) may be added to the DP80C51 design. ESFRs are memory mapped into Direct Memory between addresses 0x80 and 0xFF in the same manner as core SFRs and may occupy any address that is not occupied by a core SFR.
- ◆ **WAIT STATES SUPPORT:**

The DP80C51 soft core is dedicated for operation with wide range of Program and Data memories. Slow Program and External Data memory may assert a memory WAIT signal to hold up CPU activity for required period of time.

SYMBOL



PINS DESCRIPTION

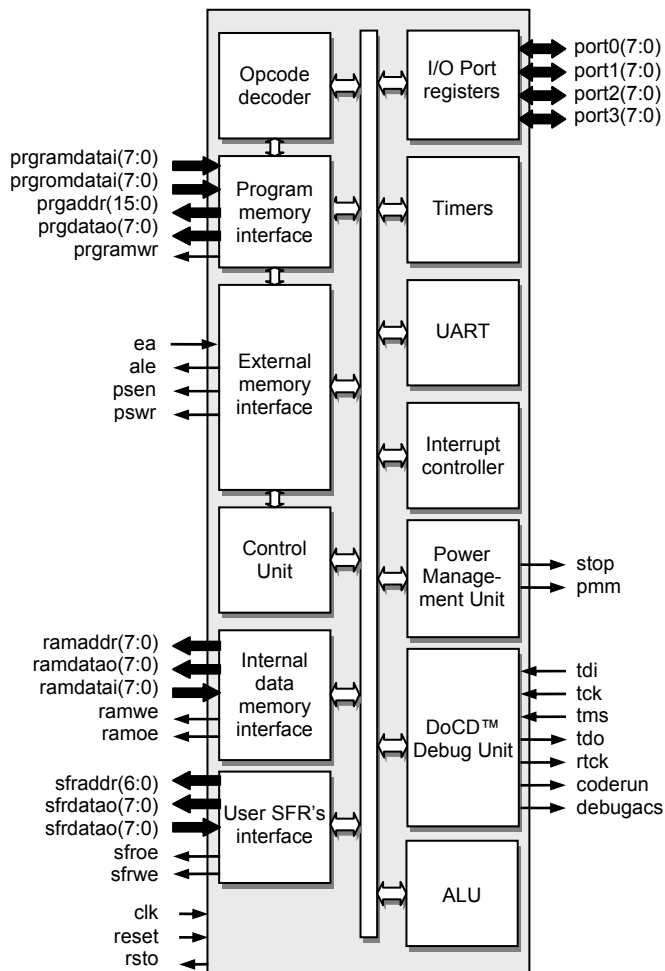
PIN	TYPE	DESCRIPTION
clk	input	Global clock
reset	input	Global reset input
port0[7:0]	bidir	I/O Port 0, multifunctional Data/LSB address of external memory
port1[7:0]	bidir	I/O Port 1
port2[7:0]	bidir	I/O Port 2, multifunctional MSB address of external memory
port3[0]	bidir	I/O Port 3.0 Serial receiver input/output port
port3[1]	bidir	I/O Port 3.1 Serial transmitter output port
port3[2]	bidir	I/O Port 3.2, multifunctional Interrupt 0 input/timer 0 gate
port3[3]	bidir	I/O Port 3.3, multifunctional Interrupt 1 input/timer 1 gate
port3[4]	bidir	I/O Port 3.4, multifunctional Timer 0 external clock line

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PIN	TYPE	DESCRIPTION
port3[5]	bidir	I/O Port 3.5, multifunctional Timer 1 external clock line
port3[6]	bidir	I/O Port 3.6 External Data Memory write
port3[7]	bidir	I/O Port 3.7 External Data Memory read
ea	input	Enable all external program memory
prgromdatai[7:0]	input	Data bus from int. RAM prog. memory
prgramdatai[7:0]	input	Data bus from int. ROM prog. memory
ramdatai[7:0]	input	Data bus from internal data memory
sfrdatai[7:0]	input	Data bus from user SFR's
tdi	input	DoCD™ TAP data input
tck	input	DoCD™ TAP clock input
tms	input	DoCD™ TAP mode select input
rsto	output	Reset output
prgaddr[15:0]	output	Internal program memory address bus
prgdatao[7:0]	output	Data bus for internal program memory
prgramwr	output	Internal program memory write
ale	output	Address Latch Enable
psen	output	Program Store (memory) read Enable
pswr	output	Program Store (memory) Write
ramaddr[7:0]	output	Internal Data Memory address bus
ramdatao[7:0]	output	Data bus for internal data memory
ramoe	output	Internal data memory output enable
ramwe	output	Internal data memory write enable
sfraddr[6:0]	output	Address bus for user SFR's
sfrdatao[7:0]	output	Data bus for user SFR's
sfro	output	User SFR's read enable
sfrwe	output	User SFR's write enable
tdo	output	DoCD™ TAP data output
rtck	output	DoCD™ return clock line
debugacs	output	DoCD™ accessing data
coderun	output	CPU is executing an instruction
pmm	output	Power management mode indicator
stop	output	Stop mode indicator

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BLOCK DIAGRAM



UNITS SUMMARY

ALU – Arithmetic Logic Unit performs the arithmetic and logic operations during execution of an instruction. It contains accumulator (ACC), Program Status Word (PSW), (B) registers and related logic such as arithmetic unit, multiplier and divider.

Opcode Decoder – Performs an instruction opcode decoding and the control functions for all other blocks.

Control Unit – Performs the core synchronization and data flow control. This module is directly connected to Opcode Decoder and manages execution of all microcontroller tasks.

Program Memory Interface – Contains Program Counter (PC) and related logic. It performs the instructions code fetching. Program Memory can be also written. This feature allows usage of a small boot loader loading new program into RAM, EPROM or FLASH

EEPROM storage via UART, SPI, I2C or DoCD™ module.

External Memory Interface - Contains memory access related registers such as Data Page High (DPH), Data Page Low (DPL). It performs the external Program and Data Memory addressing and data transfers. Program fetch cycle length can be programmed by user. This feature is called Program Memory Wait States, and allows core to work with different speed program memories.

Internal Data Memory Interface – Internal Data Memory interface controls access into the internal 256 bytes memory. It contains 8-bit Stack Pointer (SP) register and related logic.

User SFRs Interface – Special Function Registers interface controls access to the special registers. It contains standard and used defined registers and related logic. User defined external devices can be quickly accessed (read, written, modified) using all direct addressing mode instructions.

Interrupt Controller – Interrupt control module is responsible for the interrupt manage system for the external and internal interrupt sources. It contains interrupt related registers such as Interrupt Enable (IE), Interrupt Priority (IP) and (TCON) registers. Note that external pins of this module are connected to appropriate pins of P3 port.

Timers – System timers module. Contains two 16 bits configurable timers: Timer 0 (TH0, TL0), Timer 1 (TH1, TL1) and Timers Mode (TMOD) registers. In the timer mode, timer registers are incremented every 12 CLK periods when appropriate timer is enabled. In the counter mode the timer registers are incremented every falling transition on their corresponding input pins (T0, T1), if gates are opened (GATE0, GATE1). T0, T1 input pins are sampled every CLK period. It can be used as clock sources for UARTs. Note that external pins of this module are connected to appropriate pins of P3 port.

UART0 – Universal Asynchronous Receiver & Transmitter module is full duplex, meaning it can transmit and receive concurrently. Includes Serial Configuration register (SCON), serial receiver and transmitter buffer (SBUF) registers. Its receiver is double-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register. Writing to

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SBUF0 loads the transmit register, and reading SBUF0 reads a physically separate receive register. Works in 3 asynchronous and 1 synchronous modes. UART0 can be synchronized by Timer 1. Note that external pins of this module are connected to appropriate pins of P3 port.

Ports - Block contains 8051's general purpose I/O ports. Each of port's pin can be read/write as a single bit or as a 8-bit bus P0, P1, P2, P3. The P0, P2, P3 are multifunctional ports. When used with External memory P0 works as a multiplexed Data/LSB address to memory, and P2 works as a MSB address to external memory, P3.6 is a write signal and P3.7 is a read signal. Functionality of port is the same as in legacy 80C51 microcontroller.

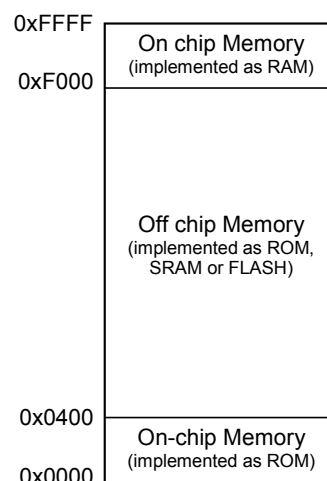
Power Management Unit – Block contains advanced power saving mechanisms with switchback feature, allowing external clock control logic to stop clocking (Stop mode) or run core in lower clock frequency (Power Management Mode) to significantly reduce power consumption. Switchback feature allows UARTs, and interrupts to be processed in full speed mode if enabled. It is very desired when microcontroller is planned to use in portable and power critical applications.

DoCD™ Debug Unit – it's a real-time hardware debugger provides debugging capability of a whole SoC system. In contrast to other on-chip debuggers DoCD™ provides non-intrusive debugging of running application. It can halt, run, step into or skip an instruction, read/write any contents of microcontroller including all registers, internal, external, program memories, all SFRs including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware breakpoint is executed if any write/read occurred at particular address with certain data pattern or without pattern. Two additional pins CODERUN, DEBUGACS indicate the state of the debugger and CPU. CODERUN is active when CPU is executing an instruction. DEBUGACS pin is active when any access is performed by DoCD™ debugger. The DoCD™ system includes **JTAG interface** and complete set of tools to communicate and work with core in real time debugging. It is built as scalable unit and some features can be turned off to save silicon and reduce power consumption. A special care on power consumption has been

taken, and when debugger is not used it is automatically switched in power save mode. Finally whole debugger is turned off when debug option is no longer used.

PROGRAM CODE SPACE IMPLEMENTATION

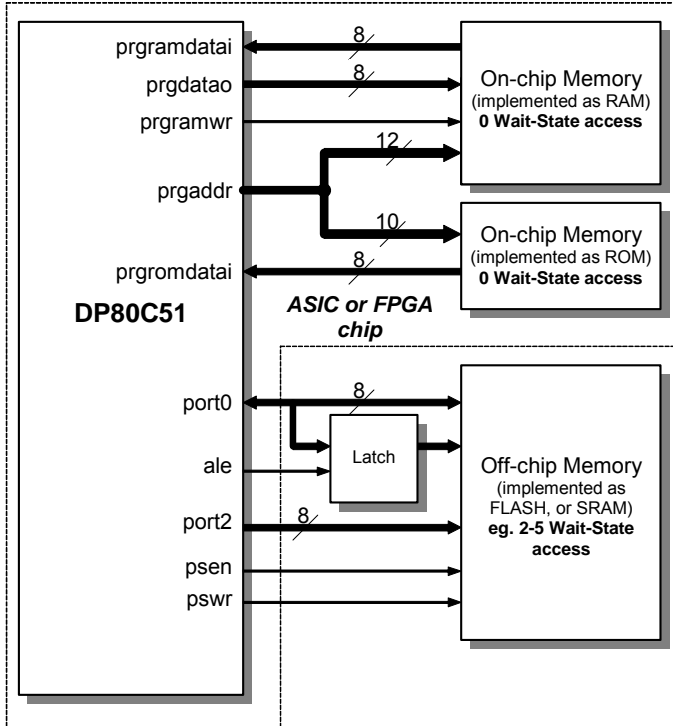
The figure below shows an example Program Memory space implementation in systems with DP80C51 Microcontroller core. The On-chip Program Memory located in address space between 0kB and 1kB is typically used for BOOT code with system initialization functions. This part of the code is typically implemented as ROM. The On-chip Program Memory located in address space between 60kB and 64kB is typically used for timing critical part of the code e.g. interrupt subroutines, arithmetic functions etc. This part of the code is typically implemented as RAM and can be loaded by the BOOT code during initialization phase from Off-chip memory or through RS232 interface from external device. From the two mentioned above spaces program code is executed without wait-states and can achieve a top performance up to 200 million instructions per second (many instructions executed in one clock cycle). The Off-chip Program Memory located in address space between 1kB and 60kB is typically used for main code and constants. This part of the code is usually implemented as ROM, SRAM or FLASH device. Because of relatively long access time the program code executed from mentioned above devices must be fetched with additional Wait-States. Number of required Wait-States depends on memory access time and DP80C51 clock frequency.



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In most cases the proper number of Wait-States cycles is between 2-5. The READY pin can be also dynamically modulated e.g. by SDRAM controller.

The figure below shows a typical Program Memories connections in system with DP80C51 Microcontroller core.



The described above implementation should be treated as an example. All Program Memory spaces are fully configurable. For timing-critical applications whole program code can be implemented as on-chip ROM and (or) RAM and executed without Wait-States, but for some other applications whole program code can be implemented as off-chip ROM or FLASH and executed with required number Wait-State cycles.

PERFORMANCE

The following tables give a survey about the Core area and performance in Programmable Logic Devices after Place & Route (CPU features and peripherals have been included):

Device	Speed grade	F _{max}
FLEX10KE	-1	57 MHz
ACEX1K	-1	57 MHz
APEX20K	-1	50 MHz
APEX20KE	-1	66 MHz
APEX20KC	-7	78 MHz
APEX-II	-7	76 MHz
MERCURY	-5	100 MHz
CYCLONE	-6	91 MHz
CYCLONE-II	-6	93 MHz

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STRATIX	-5	90 MHz
STRATIX-II	-3	160 MHz

Core performance in ALTERA® devices

For a user the most important is application speed improvement. The most commonly used arithmetic functions and their improvement are shown in table below. Improvement was computed as {80C51 clock periods} divided by {DP80C51 clock periods} required to execute an identical function for code executed from internal (first column) and external (second column) program memory. More details are available in core documentation.

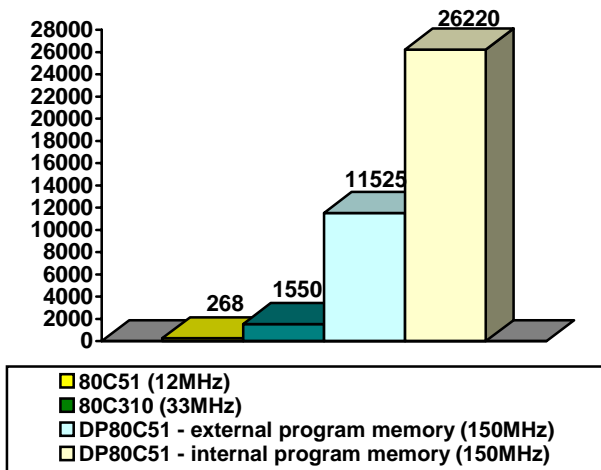
Function	Improvement	
8-bit addition (immediate data)	9,00	3,00
8-bit addition (direct addressing)	9,00	3,00
8-bit addition (indirect addressing)	9,00	3,60
8-bit addition (register addressing)	12,00	4,00
8-bit subtraction (immediate data)	9,00	3,00
8-bit subtraction (direct addressing)	9,00	3,00
8-bit subtraction (indirect addressing)	9,00	3,60
8-bit subtraction (register addressing)	12,00	4,00
8-bit multiplication	16,00	6,00
8-bit division	9,60	4,80
16-bit addition	12,00	4,00
16-bit subtraction	12,00	4,00
16-bit multiplication	13,60	5,47
32-bit addition	12,00	4,00
32-bit subtraction	12,00	4,00
32-bit multiplication	12,60	4,89
Average speed improvement:	11,12	4,03

Dhrystone Benchmark Version 2.1 was used to measure Core performance. The following table gives a survey about the DP80C51 performance in terms of Dhrystone/sec and VAX MIPS rating for testing code executed from external (1) and internal (2) program memory.

Device	Target	Clock frequency	Dhry/sec (VAX MIPS)
80C51	-	12 MHz	268 (0.153)
80C310	-	33 MHz	1550 (0.882)
DP80C51 ¹	STRATIX-II	150 MHz	11525 (6,563)
DP80C51 ²	STRATIX-II	150 MHz	26220 (14,924)

Core performance in terms of Dhrystones

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Area utilized by the each unit of DP80C51 core in vendor specific technologies is summarized in table below.

Component	Area	
	[LC]	[FFs]
CPU*	1670	310
Interrupt Controller	150	40
Power Management Unit	10	5
I/O ports	100	35
Timers	160	50
UART0	210	60
Total area	2300	500

*CPU – consisted of ALU, Opcode Decoder, Control Unit, Program & Internal & External Memory Interfaces, User SFRs Interface

Core components area utilization in all technologies except STRATIX-II

Component	Area	
	[LC]	[FFs]
CPU*	1305	310
Interrupt Controller	115	40
Power Management Unit	10	5
I/O ports	75	35
Timers	125	50
UART0	160	60
Total area	1790	500

*CPU – consisted of ALU, Opcode Decoder, Control Unit, Program & Internal & External Memory Interfaces, User SFRs Interface

Core components area utilization in STRATIX-II

The main features of each DP80C51 family member have been summarized in table below. It gives a briefly member characterization helping user to select the most suitable IP Core for its application. User can specify its own peripheral set (including listed below and the others) and requests the core modifications.

Design	Architecture speed grade			Program Memory space			Stack space size	Internal Data Memory space	External Data Memory space	External Data / Program Memory Wait States	Power Management Unit	Interface for additional SFRs	Interrupt sources	Interrupt levels	Data Pointers	Timer/Counters	UART	I/O Ports	Compare/Capture	Watchdog	Master I ² C Bus Controller	Slave I ² C Bus Controller	SPI	Fixed Point Coprocessor	Floating Point Coprocessor
	on-chip RAM	on-chip ROM	off-chip																						
DP8051CPU	10	64k	64k	64k	256	256	16M	✓	✓	✓	2	2	1	-	-	-	-	-	-	-	-	-	-	-	-
DP8051	10	64k	64k	64k	256	256	16M	✓	✓	✓	5	2	1	2	1	4	-	-	-	-	-	-	-	-	-
DP8051XP	10	64k	64k	64k	256	256	16M	✓	✓	✓	15	2	2	3	2	4	✓	✓	✓	✓	✓	✓	✓	✓	✓

DP8051 family of Pipelined High Performance Microcontroller Cores

The main features of each DP80390 family member have been summarized in table below. It gives a briefly member characterization helping user to select the most suitable IP Core for its application. User can specify its own peripheral set (including listed below and the others) and requests the core modifications.

Design	Architecture speed grade			Program Memory space			Stack space size	Internal Data Memory space	External Data Memory space	External Data / Program Memory Wait States	Power Management Unit	Interface for additional SFRs	Interrupt sources	Interrupt levels	Data Pointers	Timer/Counters	UART	I/O Ports	Compare/Capture	Watchdog	Master I ² C Bus Controller	Slave I ² C Bus Controller	SPI	Fixed Point Coprocessor	Floating Point Coprocessor
	on-chip RAM	on-chip ROM	off-chip																						
DP80390CPU	10	64k	64k	8M	256	256	16M	✓	✓	✓	2	2	1	-	-	-	-	-	-	-	-	-	-	-	-
DP80390	10	64k	64k	8M	256	256	16M	✓	✓	✓	5	2	1	2	1	4	-	-	-	-	-	-	-	-	-
DP80390XP	10	64k	64k	8M	256	256	16M	✓	✓	✓	15	2	2	3	2	4	✓	✓	✓	✓	✓	✓	✓	✓	✓

DP80390 family of Pipelined High Performance Microcontroller Cores

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